**A METHOD TO FORM VERY HIGH MOBILITY VERTICAL CHANNEL TRANSISTOR BY SELECTIVE DEPOSITION OF SiGe OR MULTI-QUANTUM WELLS (MQWs)**


## ABSTRACT

A method of fabricating a vertical channel transistor, comprising the following steps. A semiconductor substrate having an upper surface is provided. A high doped N-type lower epitaxial silicon layer is formed on the semiconductor substrate. A low doped P-type middle epitaxial silicon layer is formed on the lower epitaxial silicon layer. A high doped N-type upper epitaxial silicon layer is formed on the middle epitaxial silicon layer. The lower, middle, and upper epitaxial silicon layers are etched to form a epitaxial layer stack defined by isolation trenches. Oxide is formed within the isolation trenches. The oxide is etched to form a gate trench within one of the isolation trenches exposing a sidewall of the epitaxial layer stack facing the gate trench. Multi-quantum wells or a stained-layer super lattice is formed on the exposed epitaxial layer stack sidewall. A gate dielectric layer is formed on the multi-quantum wells or the stained-layer super lattice and within the gate trench. A gate conductor layer is formed on the gate dielectric layer, filling the gate trench.


Fig. 3