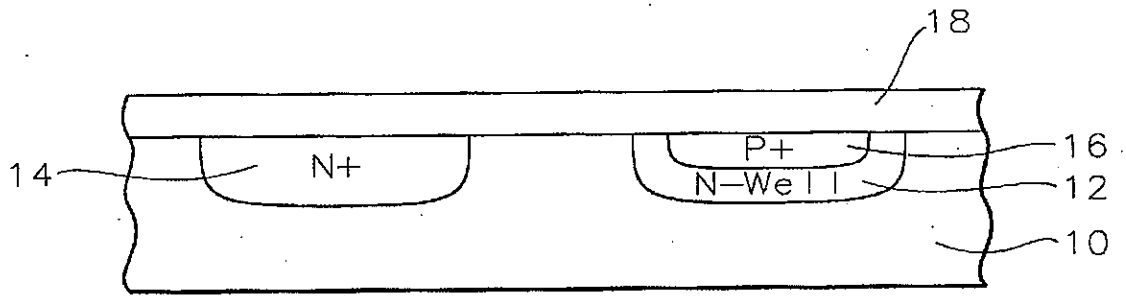


FIG. 1

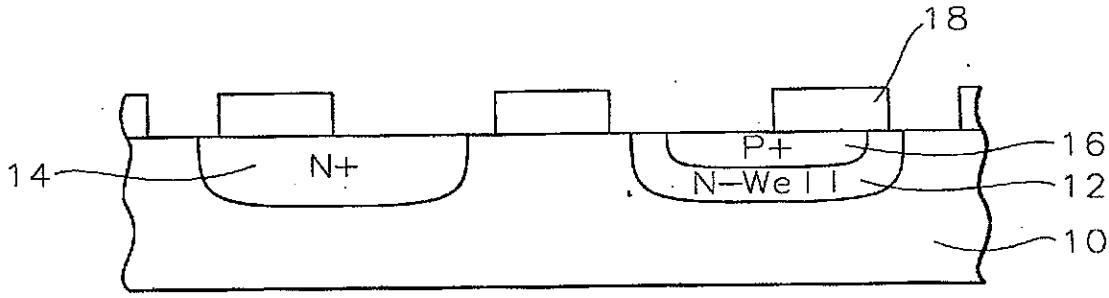


FIG. 2

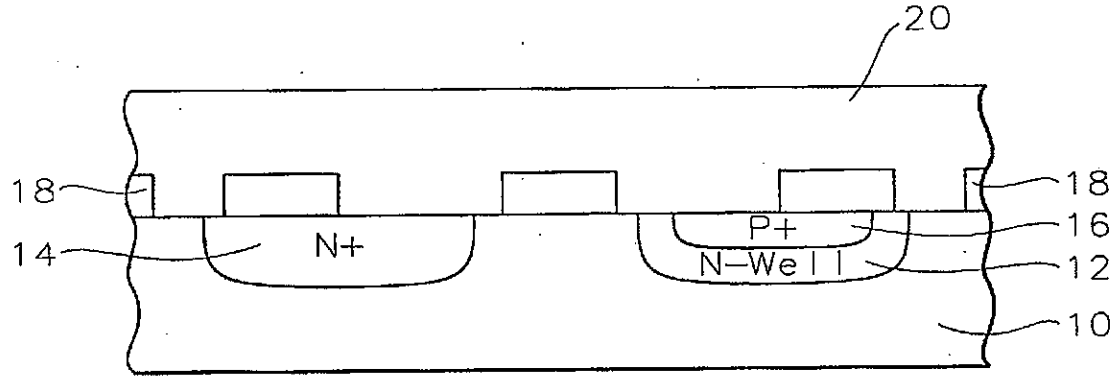


FIG. 3

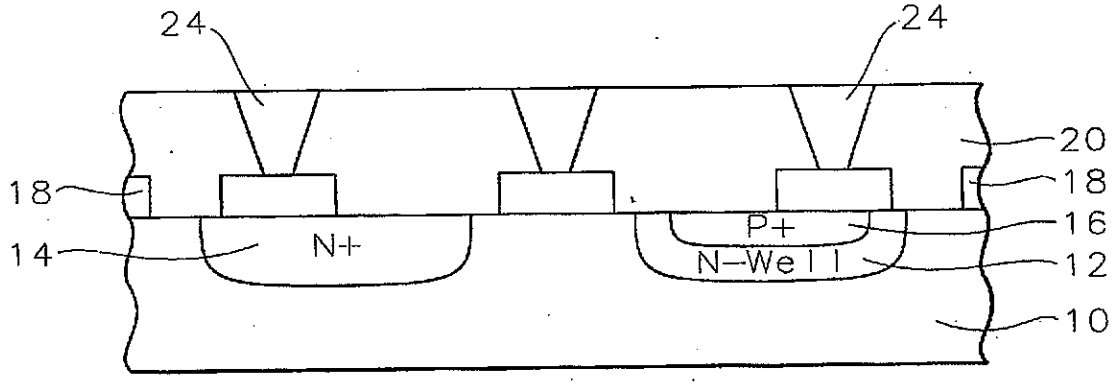


FIG. 4

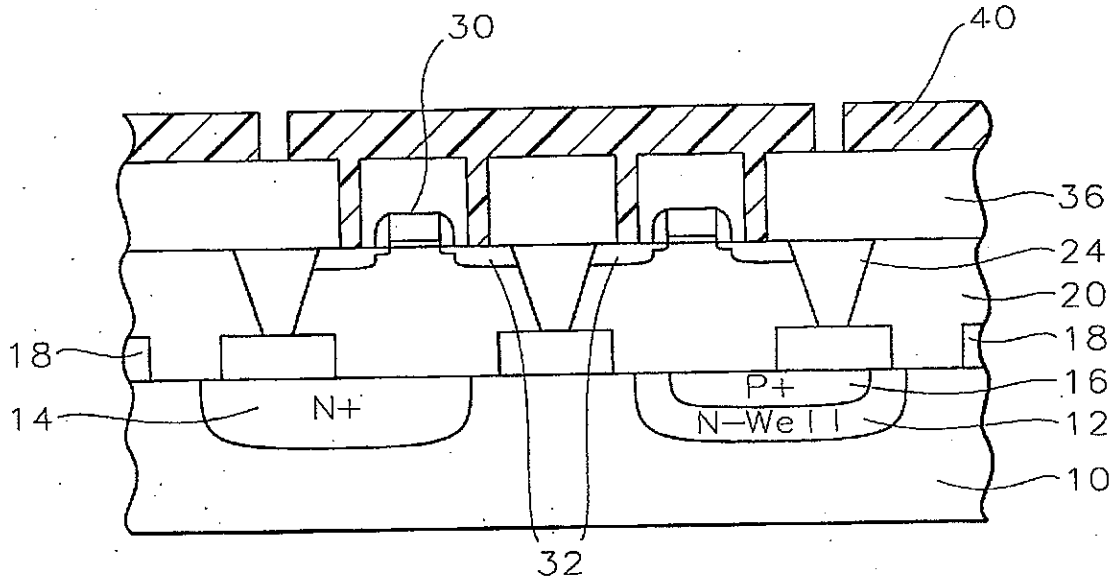

30
40
36
24
20
18
18
16
P+
14
N+
N-Well
12
10
32

FIG. 7

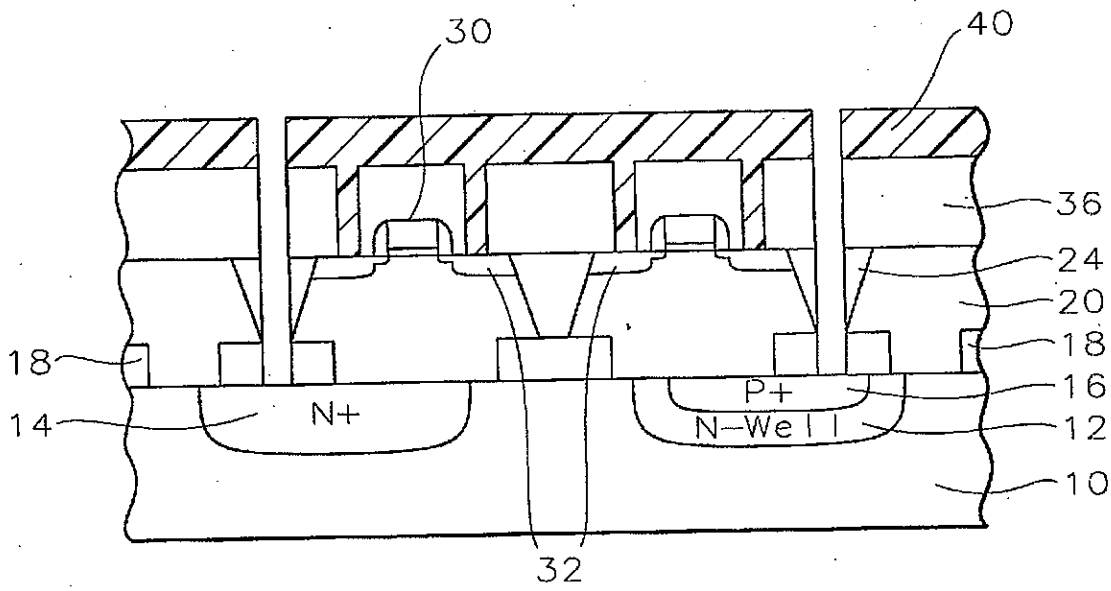

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36
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18
16
P+
14
N+
N-Well
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10
32

FIG. 8

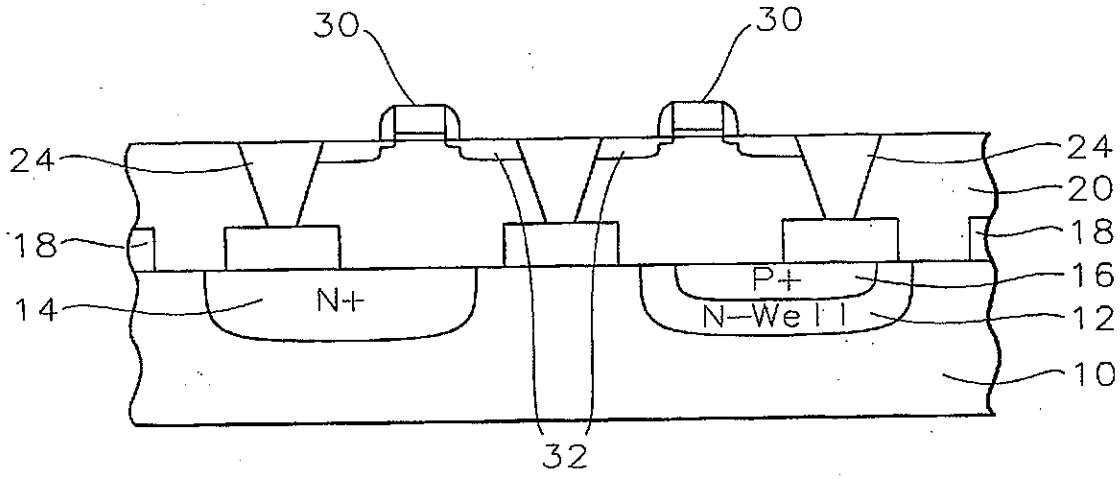

30
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24
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18
P+
16
14
N+
N–Well
12
10
32

FIG. 5

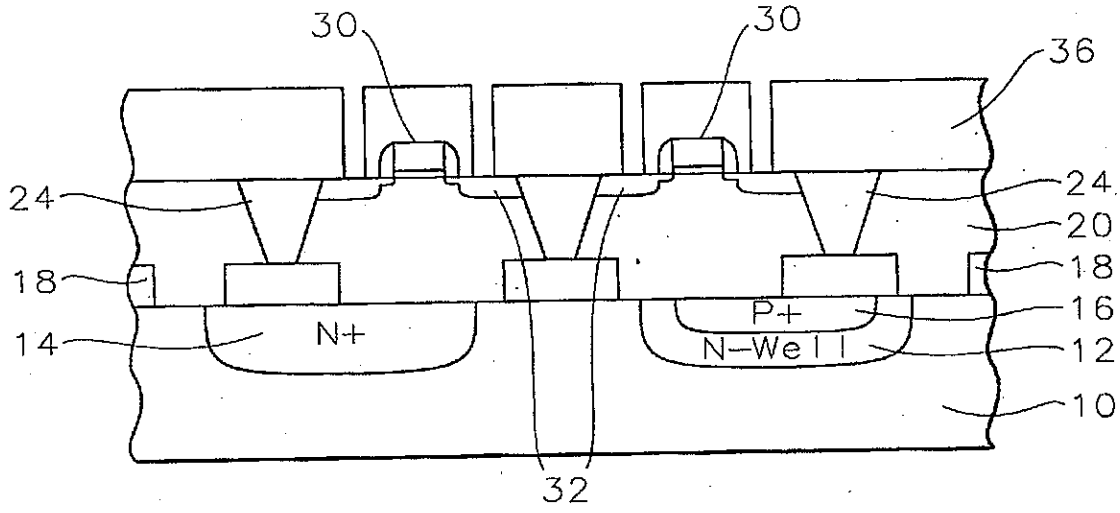

30
30
36
24
24
20
18
18
P+
16
14
N+
N–Well
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10
32

FIG. 6

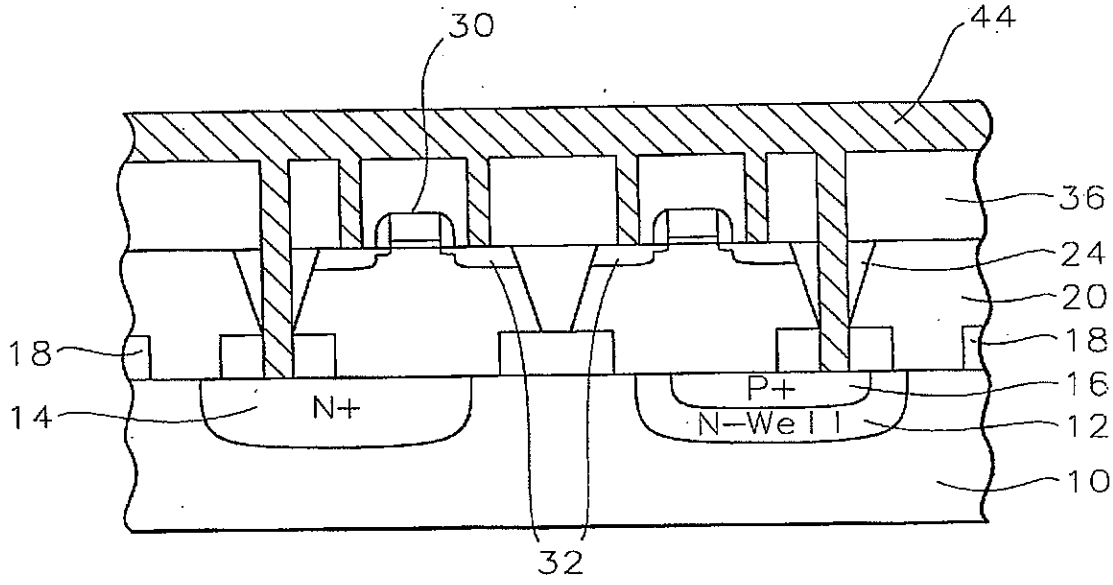

30
44
36
24
20
18
18
16
12
10
32
N+
P+
N-Well
14

FIG. 9

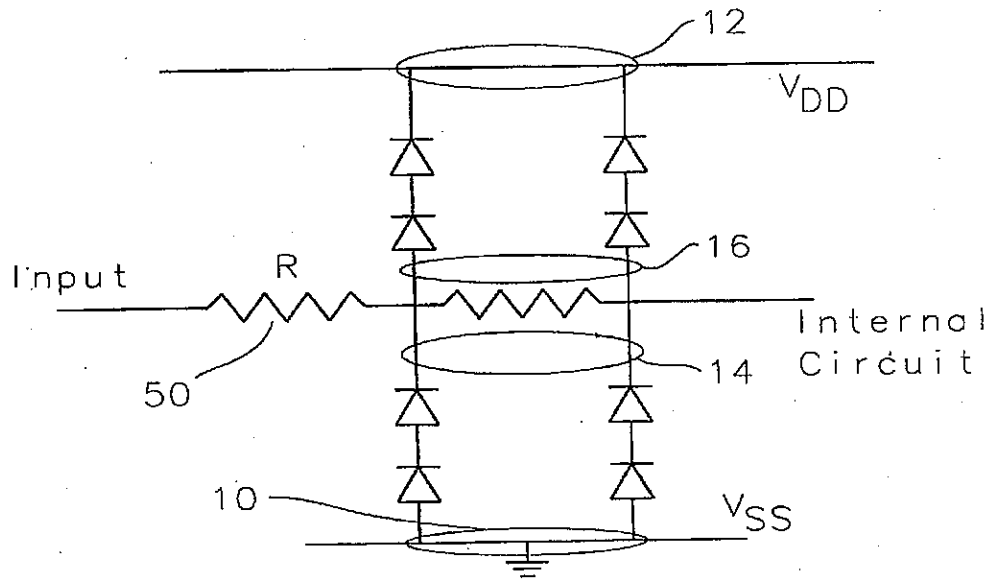

12
V_{DD}
16
Input
R
Internal
Circuit
14
50
10
V_{SS}

FIG. 10