METHODS AND APPARATUS FOR MEASURING ANALYTES USING LARGE SCALE FET ARRAYS

Field of the Disclosure

[0001] The present disclosure is directed generally to inventive methods and apparatus relating to detection and measurement of one or more analytes via electronic sensors.

Background

[0002] Electronic devices and components have found numerous applications in chemistry and biology (more generally, "life sciences"), especially for detection and measurement of various aspects of chemical reactions and substance composition. One such electronic device is referred to as an ion-sensitive field effect transistor, often denoted in the relevant literature as ISFET (or pHFET). ISFETs conventionally have been explored, primarily in the academic and research community, to facilitate measurement of the hydrogen ion concentration of a solution (commonly denoted as "pH").

[0003] More specifically, an ISFET is an impedance transformation device that operates in a manner similar to that of a MOSFET (Metal Oxide Semiconductor Field Effect Transistor), and is particularly configured to selectively measure ion activity in a solution (e.g., hydrogen ions in the solution are the "analyte"). A detailed theory of operation of an ISFET is given in "Thirty years of ISFETOLOGY: what happened in the past 30 years and what may happen in the next 30 years," P. Bergveld, *Sens. Actuators,* 88 (2003), pp. 1–20, which publication is hereby incorporated herein by reference.

[0004] Fig. 1 illustrates a cross-section of a p-type (p-channel) ISFET 50 fabricated using a conventional CMOS (Complimentary Metal Oxide Semiconductor) process. P-type ISFET fabrication is based on a p-type silicon substrate 52, in which an n-type well 54 forming a transistor "body" is formed. Highly doped p-type (p+) regions S and D, constituting a source 56 and a drain 58 of the ISFET, are formed within the n-type well 54. A highly doped n-type (n+) region B is also formed within the n-type well to provide a conductive body (or "bulk") connection 62 to the n-type well. An oxide layer 65 is disposed above the source, drain and body connection regions, through which openings are made to provide electrical connections (via electrical conductors) to these regions; for

example, metal contact 66 serves as a conductor to provide an electrical connection to the drain 58, and metal contact 68 serves as a conductor to provide a common connection to the source 56 and n-type well 54, via the highly conductive body connection 62. A polysilicon gate 64 is formed above the oxide layer at a location above a region 60 of the n-type well 54, between the source 56 and the drain 58. Because it is disposed between the polysilicon gate 64 and the transistor body (i.e., the n-type well), the oxide layer 65 often is referred to as the "gate oxide."

[0005] Like a MOSFET, the operation of an ISFET is based on the modulation of charge concentration caused by a MOS (Metal-Oxide-Semiconductor) capacitance constituted by the polysilicon gate 64, the gate oxide 65 and the region 60 of the n-type well 54 between the source and the drain. When a negative voltage is applied across the gate and source regions ($V_{GS} < 0$ Volts), a "p-channel" 63 is created at the interface of the region 60 and the gate oxide 65 by depleteing this area of electrons. This p-channel 63 extends between the source and the drain, and and electric current is conducted through the p-channel when the gate-source potential V_{GS} is negative enough to attract holes from the source into the channel. The gate-source potential at which the channel 63 begins to conduct current is referred to as the transistor's threshold voltage V_{TH} (the transistor conducts when V_{GS} has an absolute value greater than the threshold voltage V_{TH}). The source is so named because it is the source of the charge carriers (holes for a p-channel) that flow through the channel 63; similarly, the drain is where the charge carriers leave the channel 63.

[0006] In the ISFET 50 of Fig. 1, the n-type well 54 (transistor body), via the body connection 62, is forced to be biased at a same potential as the source 56 (i.e., $V_{SB} = 0$ Volts), as seen by the metal contact 68 connected to both the source 56 and the body connection 62. This connection prevents forward biasing of the p+ source region and the n-type well, and thereby facilitates confinement of charge carriers to the area of the region 60 in which the channel 63 may be formed. Any potential difference between the source 56 and the body/n-type well 54 (a non-zero source-to-body voltage V_{SB}) affects the threshold voltage V_{TH} of the ISFET according to a nonlinear relationship, and is commonly referred to as the "body effect," which in many applications is undesirable.

[0007] As also shown in Fig. 1, the polysilicon gate 64 of the ISFET 50 is coupled to multiple metal layers disposed within one or more additional oxide layers 75 disposed

above the gate oxide 65 to form a "floating gate" structure 70. The floating gate structure is so named because it is electrically isolated from other conductors associated with the ISFET; namely, it is sandwiched between the gate oxide 65 and a passivation layer 72. In the ISFET 50, the passivation layer 72 constitutes an ion-sensitive membrane that gives rise to the ion-sensitivity of the device; i.e., the presence of ions in an "analyte solution" 74 (a solution containing ions of interest) in contact with the passivation layer 72, particularly in a sensitive area 78 above the floating gate structure 70, alters the electrical characteristics of the ISFET so as to modulate a current flowing through the p-channel 63 between the source 56 and the drain 58. The passivation layer 72 may comprise any one of a variety of different materials to facilitate sensitivity to particular ions; for example, passivation layers comprising silicon nitride or silicon oxynitride generally provide sensitivity to hydrogen ion concentration (pH) in the analyte solution 74, whereas passivation layers comprising polyvinyl chloride containing valinomycin provide sensitivity to potassium ion concentration in the analyte solution (materials suitable for passivation layers and sensitive to other ions such as sodium, silver, iron, bromine, iodine, calcium, and nitrate, for example, are known).

[0008] With respect to ion sensitivity, an electric potential difference, commonly referred to as a "surface potential," arises at the solid/liquid interface of the passivation layer 72 and the analyte solution 74 as a function of the ion concentration in the sensitive area 78 due to a chemical reaction (e.g., usually involving the dissociation of oxide surface groups by the ions in the analyte solution in proximity to the sensitive area 78). This surface potential in turn affects the threshold voltage V_{TH} of the ISFET; thus, it is the threshold voltage V_{TH} of the ISFET that varies with changes in ion concentration in the analyte solution 74 in proximity to the sensitive area 78.

[0009] Fig. 2 illustrates an electric circuit representation of the p-channel ISFET 50 shown in Fig. 1. With reference again to Fig. 1, a reference electrode 76 (a conventional Ag/AgCl electrode) in the analyte solution 74 determines the electric potential of the bulk of the analyte solution itself and is analogous to the gate terminal of a conventional MOSFET, as shown in Fig. 2. In a linear or non-saturated operating region of the ISFET, the drain current I_D is given as:

$$I_D = \beta\left(V_{GS} - V_{TH} - \tfrac{1}{2}V_{DS}\right)V_{DS}, \qquad (1)$$

[0010] where V_{DS} is the voltage between the drain and the source, and β is a transconductance parameter (in units of Amps/Volts^2) given by:

$$\beta = \mu C_{ox}\left(\frac{W}{L}\right), \qquad (2)$$

[0011] where μ represents the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, and the ratio W/L is the width to length ratio of the channel 63. If the reference electrode 76 provides an electrical reference or ground ($V_G = 0$ Volts), and the drain current I_D and the drain-to-source voltage V_{DS} are kept constant, variations of the source voltage V_S of the ISFET directly track variations of the threshold voltage V_{TH}, according to Eq. (1); this may be observed by rearranging Eq. (1) as:

$$V_S = -V_{TH} - \left(\frac{I_D}{\beta V_{DS}} + \frac{V_{DS}}{2}\right). \qquad (3)$$

[0012] Since the threshold voltage V_{TH} of the ISFET is sensitive to ion concentration as discussed above, according to Eq. (3) the source voltage V_S provides a signal that is directly related to the ion concentration in the analyte solution 74 in proximity to the sensitive area 78 of the ISFET. In exemplary conventional ISFETs employing a silicon nitride or silicon oxynitride passivation layer 72 for pH-sensitivity, a threshold voltage sensitivities ΔV_{TH} (i.e., a change in threshold voltage with change in pH of the analyte solution) of approximately 30 mV/pH to 50 mV/pH have been observed (with a theoretical maximum sensitivity of 59.2 mV/pH at 298 degrees Kelvin).

[0013] Prior research efforts to fabricate ISFETs for pH measurements based on conventional CMOS processing techniques typically have aimed to achieve high signal linearity over a pH range from 1-14. Using an exemplary threshold sensitivity of approximately 50 mV/pH, and considering Eq. (3) above, this requires a linear operating range of approximately 700 mV for the source voltage V_S. As discussed above in connection with Fig. 1, the threshold voltage V_{TH} of ISFETs (as well as MOSFETs) is affected by any voltage V_{SB} between the source and the body (n-type well 54). More specifically, the threshold voltage V_{TH} is a nonlinear function of a nonzero source-to-body voltage V_{SB}. Accordingly, so as to avoid compromising linearity due to a difference between the source and body voltage potentials (i.e., to mitigate the "body effect"), as shown in Fig. 1 the source 56 and body connection 62 of the ISFET 50 often are coupled to

a common potential via the metal contact 68. This body-source coupling also is shown in the electric circuit representation of the ISFET 50 shown in Fig 2.

[0014] Previous efforts to fabricate two-dimensional arrays of ISFETs based on the ISFET design of Fig. 1 have resulted in a maximum of 256 ISFET sensor elements, or "pixels," in an array (i.e., a 16 pixel by 16 pixel array). Exemplary research in ISFET array fabrication are reported in the publications "A large transistor-based sensor array chip for direct extracellular imaging," M.J. Milgrew, M.O. Riehle, and D.R.S. Cumming, *Sensors and Actuators, B: Chemical*, 111-112, (2005), pp. 347-353, and "The development of scalable sensor arrays using standard CMOS technology," M.J. Milgrew, P.A. Hammond, and D.R.S. Cumming, *Sensors and Actuators, B: Chemical*, 103, (2004), pp. 37-42, which publications are incorporated herein by reference and collectively referred to hereafter as "Milgrew et al." Other research efforts relating to the realization of ISFET arrays are reported in the publications "A very large integrated pH-ISFET sensor array chip compatible with standard CMOS processes," T. C. W. Yeow, M. R. Haskard, D. E. Mulcahy, H. I. Seo and D. H. Kwon, *Sensors and Actuators B: Chemical*, 44, (1997), pp. 434-440 and "Fabrication of a two-dimensional pH image sensor using a charge transfer technique," Hizawa, T., Sawada, K., Takao, H., Ishida, M., *Sensors and Actuators, B: Chemical* 117 (2), 2006, pp. 509-515, which publications also are incorporated herein by reference.

[0015] Fig. 3 illustrates one column 85_j of a two-dimensional ISFET array according to the design of Milgrew et al. The column 85_j includes sixteen (16) pixels 80_1 through 80_{16} and, as discussed further below in connection with Fig. 7, a complete two-dimensional array includes sixteen (16) such columns 85_j (j = 1, 2, 3,....16) arranged side by side. As shown in Fig. 3, a given column 85_j includes a current source $I_{SOURCEj}$ that is shared by all pixels of the column, and ISFET bias/readout circuitry 82_j (including current sink I_{SINKj}) that is also shared by all pixels of the column. Each ISFET pixel 80_1 through 80_{16} includes a p-channel ISFET 50 having an electrically coupled source and body (as shown in Figs. 1 and 2), plus two switches S1 and S2 that are responsive to one of sixteen row select signals ($RSEL_1$ through $RSEL_{16}$, and their complements). As discussed below in connection with Fig. 7, a row select signal and its complement are generated simultaneously to "enable" or select a given pixel of the column 85_j, and such signal pairs are generated in some sequence to successively enable different pixels of the column one at a time.

[0016] As shown in Fig. 3, the switch S2 of each pixel 80 in the design of Milgrew et al. is implemented as a conventional n-channel MOSFET that couples the current source $I_{SOURCEj}$ to the source of the ISFET 50 upon receipt of the corresponding row select signal. The switch S1 of each pixel 80 is implemented as a transmission gate, i.e., a CMOS pair including an n-channel MOSFET and a p-channel MOSFET, that couples the source of the ISFET 50 to the bias/readout circuitry 82_j upon receipt of the corresponding row select signal and its complement. An example of the switch $S1_1$ of the pixel 80_1 is shown in Fig. 4, in which the p-channel MOSFET of the transmission gate is indicated as $S1_{1P}$ and the n-channel MOSFET is indicated as $S1_{1N}$. In the design of Milgrew et al., a transmission gate is employed for the switch S1 of each pixel so that, for an enabled pixel, any ISFET source voltage within the power supply range V_{DD} to V_{SS} may be applied to the bias/readout circuitry 82_j and output by the column as the signal V_{Sj}. From the foregoing, it should be appreciated that each pixel 80 in the ISFET sensor array design of Milgrew et al. includes four transistors, i.e., a p-channel ISFET, a CMOS-pair transmission gate including an n-channel MOSFET and a p-channel MOSFET for switch S1, and an n-channel MOSFET for switch S2.

[0017] As also shown in Fig. 3, the bias/readout circuitry 82_j employs a source-drain follower configuration in the form of a Kelvin bridge to maintain a constant drain-source voltage V_{DSj} and isolate the measurement of the source voltage V_{Sj} from the constant drain current $I_{SOURCEj}$ for the ISFET of an enabled pixel in the column 85_j. To this end, the bias/readout circuitry 82_j includes two operational amplifiers A1 and A2, a current sink I_{SINKj}, and a resistor R_{SDj}. The voltage developed across the resistor R_{SDj} due to the current I_{SINKj} flowing through the resistor is forced by the operational amplifiers to appear across the drain and source of the ISFET of an enabled pixel as a constant drain-source voltage V_{DSj}. Thus, with reference again to Eq. (3), due to the constant V_{DSj} and the constant $I_{SOURCEj}$, the source voltage V_{Sj} of the ISFET of the enabled pixel provides a signal corresponding to the ISFETs threshold voltage V_{TH}, and hence a measurement of pH in proximity to the ISFETs sensitive area (see Fig. 1). The wide dynamic range for the source voltage V_{Sj} provided by the transmission gate S1 ensures that a full range of pH values from 1-14 may be measured, and the source-body connection of each ISFET ensures sufficient linearity of the ISFETs threshold voltage over the full pH measurement range.

[0018] In the column design of Milgrew et al. shown in Fig. 3, it should be appreciated that for the Kelvin bridge configuration of the column bias/readout circuitry 82_j to function properly, a p-channel ISFET 50 as shown in Fig. 1 must be employed in each pixel; more specifically, an alternative implementation based on the Kelvin bridge configuration is not possible using an n-channel ISFET. With reference again to Fig. 1, for an n-channel ISFET based on a conventional CMOS process, the n-type well 54 would not be required, and highly doped n-type regions for the drain and source would be formed directly in the p-type silicon substrate 52 (which would constitute the transistor body). For n-channel FET devices, the transistor body typically is coupled to electrical ground. Given the requirement that the source and body of an ISFET in the design of Milgrew et al. are electrically coupled together to mitigate nonlinear performance due to the body effect, this would result in the source of an n-channel ISFET also being connected to electrical ground (i.e., $V_S = V_B = 0$ Volts), thereby precluding any useful output signal from an enabled pixel. Accordingly, the column design of Milgrew et al. shown in Fig. 3 requires p-channel ISFETs for proper operation.

[0019] It should also be appreciated that in the column design of Milgrew et al. shown in Fig. 3, the two n-channel MOSFETs required to implement the switches S1 and S2 in each pixel cannot be formed in the n-type well 54 shown in Fig. 1, in which the p-channel ISFET for the pixel is formed; rather, the n-channel MOSFETs are formed directly in the p-type silicon substrate 52, beyond the confines of the n-type well 54 for the ISFET. Fig. 5 is a diagram similar to Fig. 1, illustrating a wider cross-section of a portion of the p-type silicon substrate 52 corresponding to one pixel 80 of the column 85j shown in Fig. 3, in which the n-type well 54 containing the drain 58, source 56 and body connection 62 of the ISFET 50 is shown alongside a first n-channel MOSFET corresponding to the switch S2 and a second n-channel MOSFET $S1_{1N}$ constituting one of the two transistors of the transmission gate $S1_1$ shown in Fig. 4.

[0020] Furthermore, in the design of Milgrew et al., the p-channel MOSFET required to implement the transmission gate S1 in each pixel (e.g., see $S1_{1P}$ in Fig. 4) cannot be formed in the same n-type well in which the p-channel ISFET 50 for the pixel is formed. In particular, because the body and source of the p-channel ISFET are electrically coupled together, implementing the p-channel MOSFET $S1_{1P}$ in the same n-well as the p-channel ISFET 50 would lead to unpredictable operation of the transmission gate, or preclude

operation entirely. Accordingly, two separate n-type wells are required to implement each pixel in the design of Milgrew et al. Fig. 6 is a diagram similar to Fig. 5, showing a cross-section of another portion of the p-type silicon substrate 52 corresponding to one pixel 80, in which the n-type well 54 corresponding to the ISFET 50 is shown alongside a second n-type well 55 in which is formed the p-channel MOSFET $S1_{1P}$ constituting one of the two transistors of the transmission gate $S1_1$ shown in Fig. 4. It should be appreciated that the drawings in Figs. 5 and 6 are not to scale and may not exactly represent the actual layout of a particular pixel in the design of Milgrew et al.; rather these figures are conceptual in nature and are provided primarily to illustrate the requirements of multiple n-wells, and separate n-channel MOSFETs fabricated outside of the n-wells, in the design of Milgrew et al.

[0021] The array design of Milgrew et al. was implemented using a 0.35 micrometer (μm) conventional CMOS fabrication process. In this process, various design rules dictate minimum separation distances between features. For example, according to the 0.35 μm CMOS design rules, with reference to Fig. 6, a distance "a" between neighboring n-wells must be at least three (3) micrometers. A distance "a/2" also is indicated in Fig. 6 to the left of the n-well 54 and to the right of the n-well 55 to indicate the minimum distance required to separate the pixel 80 shown in Fig. 6 from neighboring pixels in other columns to the left and right, respectively. Additionally, according to the 0.35 μm CMOS design rules, a distance "b" shown in Fig. 6 representing the width in cross-section of the n-type well 54 and a distance "c" representing the width in cross-section of the n-type well 55 are each on the order of approximately 3 μm to 4 μm (within the n-type well, an allowance of 1.2 μm is made between the edge of the n-well and each of the source and drain, and the source and drain themselves have a width on the order of 0.7 μm). Accordingly, a total distance "d" shown in Fig. 6 representing the width of the pixel 80 in cross-section is on the order of approximately 12 μm to 14 μm. In one implementation, Milgrew et al. report an array based on the column/pixel design shown in Fig. 3 comprising geometrically square pixels each having a dimension of 12.8 μm by 12.8 μm.

[0022] In sum, the ISFET pixel design of Milgrew et al. is aimed at ensuring accurate hydrogen ion concentration measurements over a pH range of 1-14. To ensure measurement linearity, the source and body of each pixel's ISFET are electrically coupled together. To ensure a full range of pH measurements, a transmission gate S1 is employed in

each pixel to transmit the source voltage of an enabled pixel. Thus, each pixel of Milgrew's array requires four transistors (p-channel ISFET, p-channel MOSFET, and two n-channel MOSFETs) and two separate n-wells (Fig. 6). Based on a 0.35 micrometer conventional CMOS fabrication process and the corresponding design rules, the pixels of such an array have a minimum size appreciably greater than 10 μm, i.e., on the order of approximately 12 μm to 14 μm.

[0023] Fig. 7 illustrates a complete two-dimensional pixel array 95 according to the design of Milgrew et al., together with accompanying row and column decoder circuitry and measurement readout circuitry. The array 95 includes sixteen columns 85_1 through 85_{16} of pixels, each column having sixteen pixels as discussed above in connection with Fig. 3 (i.e., a 16 pixel by 16 pixel array). A row decoder 92 provides sixteen pairs of complementary row select signals, wherein each pair of row select signals simultaneously enables one pixel in each column 85_1 through 85_{16} to provide a set of column output signals from the array 95 based on the respective source voltages V_{S1} through V_{S16} of the enabled row of ISFETs. The row decoder 92 is implemented as a conventional four-to-sixteen decoder (i.e., a four-bit binary input $ROW_1 - ROW_4$ to select one of 2^4 outputs). The set of column output signals V_{S1} through V_{S16} for an enabled row of the array is applied to switching logic 96, which includes sixteen transmission gates S1 through S16 (one transmission gate for each output signal). As above, each transmission gate of the switching logic 96 is implemented using a p-channel MOSFET and an n-channel MOSFET to ensure a sufficient dynamic range for each of the output signals V_{S1} through V_{S16}. The column decoder 94, like the row decoder 92, is implemented as a conventional four-to-sixteen decoder and is controlled via the four-bit binary input $COL_1 - COL_4$ to enable one of the transmission gates S1 through S16 of the switching logic 96 at any given time, so as to provide a single output signal V_S from the switching logic 96. This output signal V_S is applied to a 10-bit analog to digital converter (ADC) 98 to provide a digital representation $D_1 - D_{10}$ of the output signal V_S corresponding to a given pixel of the array.

[0024] As noted earlier, individual ISFETs and arrays of ISFETs similar to those discussed above have been employed as sensing devices in a variety of applications involving chemistry and biology. In particular, ISFETs have been employed as pH sensors in various processes involving nucleic acids such as DNA. Some examples of employing ISFETs in various life-science related applications are given in the following publications,

each of which is incorporated herein by reference: Massimo Barbaro, Annalisa Bonfiglio, Luigi Raffo, Andrea Alessandrini, Paolo Facci and Imrich Barák, "Fully electronic DNA hybridization detection by a standard CMOS biochip," *Sensors and Actuators B: Chemical*, Volume 118, Issues 1-2, 2006, pp. 41-46; Toshinari Sakurai and Yuzuru Husimi, "Real-time monitoring of DNA polymerase reactions by a micro ISFET pH sensor," *Anal. Chem.*, *64*(17), 1992, pp 1996 – 1997; S. Purushothaman, C. Toumazou, J. Georgiou, "Towards fast solid state DNA sequencing," *Circuits and Systems,* vol.4, 2002, pp. IV-169 to IV-172; S. Purushothaman, C. Toumazou, C.P. Ou, "Protons and single nucleotide polymorphism detection: A simple use for the Ion Sensitive Field Effect Transistor," *Sensors and Actuators B*: *Chemical*, Vol. 114, no. 2, 2006, pp. 964-968; A.L. Simonian, A.W. Flounders, J.R. Wild, "FET-Based Biosensors for The Direct Detection of Organophosphate Neurotoxins," *Electroanalysis*, Vol. 16, No. 22, 2004, pp. 1896-1906; C. Toumazou, S. Purushothaman, "Sensing Apparatus and Method," United States Patent Application 2004-0134798, published July 15, 2004; and T.W. Koo, S. Chan, X. Su, Z. Jingwu, M. Yamakawa, V.M. Dubin, "Sensor Arrays and Nucleic Acid Sequencing Applications," United States Patent Application 2006-0199193, published September 7, 2006.

[0025] In general, the development of rapid and sensitive nucleic acid sequencing methods utilizing automated DNA sequencers has significantly advanced the understanding of biology. The term "sequencing" refers to the determination of a primary structure (or primary sequence) of an unbranched biopolymer, which results in a symbolic linear depiction known as a "sequence" that succinctly summarizes much of the atomic-level structure of the sequenced molecule. "DNA sequencing" particularly refers to the process of determining the nucleotide order of a given DNA fragment. Analysis of entire genomes of viruses, bacteria, fungi, animals and plants is now possible, but such analysis generally is limited due to the cost and throughput of sequencing. More specifically, present conventional sequencing methods are limited in terms of the accuracy of the sequence, the length of individual templates that can be sequenced, the cost of the sequence, and the rate of sequence determination.

[0026] Despite improvements in sample preparation and sequencing technologies, none of the present conventional sequencing strategies, including those to date that may involve ISFETs, has provided the cost reductions required to increase throughput to levels required for analysis of large numbers of individual human genomes. It is necessary to sequence a

large number of individual genomes to understand the genetic basis of disease and aging. In addition, a large number of cancers will need to be sequenced to understand the somatic changes underlying cancer. Some recent efforts have made significant gains in both the ability to prepare genomes for sequencing and to sequence large numbers of templates simultaneously. However, these and other efforts are still limited by the relatively large size of the reaction volumes needed to prepare templates that are detectable by these systems, as well as the need for special nucleotide analogues, and complex enzymatic or fluorescent methods to read out the bases.

Summary

[0027] Applicants have recognized and appreciated that large arrays of ISFETs may be particularly configured and employed to facilitate DNA sequencing techniques based on monitoring changes in chemical processes relating to DNA synthesis. More generally, Applicants have recognized and appreciated that large arrays of chemically-sensitive FETs may be employed to detect and measure concentrations/levels of a variety of analytes (e.g., hydrogen ions, other ions, non-ionic molecules or compounds, binding events, etc.) in a host of chemical and/or biological processes (chemical reactions, cell cultures, neural activity, nucleic acid sequencing, etc.) in which valuable information may be obtained based on such analyte measurements.

[0028] Accordingly, various embodiments of the present disclosure is directed generally to inventive methods and apparatus relating to large scale FET arrays for measuring one or more analytes. In the various embodiments disclosed herein, FET arrays include multiple "chemFETs," or chemically-sensitive field-effect transistors, that act as chemical sensors. An ISFET, as discussed above, is a particular type of chemFET that is configured for ion detection, and ISFETs may be employed in various embodiments disclosed herein. Other types of chemFETs contemplated by the present disclosure include ENFETs, which are configured for sensing of specific enzymes. It should be appreciated, however, that the present disclosure is not limited to ISFETs and ENFETs, but more generally relates to any FET that is configured for some type of chemical sensitivity.

[0029] According to yet other embodiments, the present disclosure is directed generally to inventive methods and apparatus relating to the delivery to the above-described large scale chemFET arrays of appropriate chemical samples to evoke corresponding responses.

The chemical samples may comprise (liquid) analyte samples in small reaction volumes, to facilitate high speed, high-density determination of chemical (e.g., ion or other constituent) concentration or other measurements on the analyte.

[0030] For example, some embodiments are directed to a "very large scale" two-dimensional chemFET sensor array (e.g., greater than 256k sensors), in which one or more chemFET-containing elements or "pixels" constituting the sensors of such an array are configured to monitor one or more independent chemical reactions or events occurring in proximity to the pixels of the array. In some exemplary implementations, the array may be coupled to one or more microfluidics structures that form one or more reaction chambers, or "wells" or "microwells," over individual sensors or groups of sensors of the array, and apparatus which delivers analyte samples to the wells and removes them from the wells between measurements. Even when microwells are not employed, the sensor array may be coupled to one or more microfluidics structures for the delivery of one or more analytes to the pixels and for removal of analyte(s) between measurements. Accordingly, inventive aspects of this disclosure, which are desired to be protected, include the various microfluidic structures which may be employed to flow reagents/analytes to and from the wells or pixels, the methods of manufacture of the array of wells, methods and structures for coupling the wells with the pixels of the array, and methods and apparatus for loading the wells with DNA-bearing beads when the apparatus is used for DNA sequencing or related analysis.

[0031] A unique reference electrode and its coupling to the flow cell are also shown.

[0032] In various embodiments, an analyte of particular interest is hydrogen ions, and large scale ISFET arrays according to the present disclosure are specifically configured to measure pH. In other embodiments, the chemical reactions being monitored may relate to DNA synthesis processes, or other chemical and/or biological processes, and chemFET arrays may be specifically configured to measure pH or one or more other analytes that provide relevant information relating to a particular chemical process of interest. In various aspects, the chemFET arrays are fabricated using conventional CMOS processing technologies, and are particularly configured to facilitate the rapid acquisition of data from the entire array (scanning all of the pixels to obtain corresponding pixel output signals).

[0033] With respect to analyte detection and measurement, it should be appreciated that in various embodiments discussed in greater detail below, one or more analytes measured

by a chemFET array according to the present disclosure may include any of a variety of chemical substances that provide relevant information regarding a chemical process or chemical processes of interest (e.g., binding of multiple nucleic acid strands, binding of an antibody to an antigen, etc.). In some aspects, the ability to measure levels or concentrations of one or more analytes, in addition to merely detecting the presence of an analyte, provides valuable information in connection with the chemical process or processes. In other aspects, mere detection of the presence of an analyte or analytes of interest may provide valuable information.

[0034] A chemFET array according to various inventive embodiments of the present disclosure may be configured for sensitivity to any one or more of a variety of analytes/chemical substances. In one embodiment, one or more chemFETs of an array may be particularly configured for sensitivity to one or more analytes representing one or more binding events (e.g., associated with a nucleic acid sequencing process), and in other embodiments different chemFETs of a given array may be configured for sensitivity to different analytes. For example, in one embodiment, one or more sensors (pixels) of the array may include a first type of chemFET configured to be chemically sensitive to a first analyte, and one or more other sensors of the array may include a second type of chemFET configured to be chemically sensitive to a second analyte different from the first analyte. In one exemplary implementation, the first analyte may represent a first binding event associated with a nucleic acid sequencing process, and the second analyte may represent a second binding event associated with the nucleic acid sequencing process. Of course, it should be appreciated that more than two different types of chemFETs may be employed in any given array to detect and/or measure different types of analytes/binding events. In general, it should be appreciated in any of the embodiments of sensor arrays discussed herein that a given sensor array may be "homogeneous" and include chemFETs of substantially similar or identical types to detect and/or measure a same type of analyte (e.g., pH or other ion concentration), or a sensor array may be "heterogeneous" and include chemFETs of different types to detect and/or measure different analytes.

[0035] In yet other aspects, Applicants have specifically improved upon the ISFET array design of Milgrew et al. discussed above in connection with Figs. 1-7, as well as other conventional ISFET array designs, so as to significantly reduce pixel size, and thereby increase the number of pixels of a chemFET array for a given semiconductor die size (i.e.,

increase pixel density). In various embodiments, this increase in pixel density is accomplished while at the same time increasing the signal-to-noise ratio (SNR) of output signals corresponding to respective measurements relating to monitored chemical processes, and the speed with which such output signals may be read from the array. In particular, Applicants have recognized and appreciated that by relaxing requirements for chemFET linearity and focusing on a more limited measurement output signal range (e.g., output signals corresponding to a pH range of from approximately 7 to 9 rather than 1 to 14), individual pixel complexity and size may be significantly reduced, thereby facilitating the realization of very large scale dense chemFET arrays. Applicants have also recognized and appreciated that alternative less complex approaches to pixel selection in an chemFET array (e.g., alternatives to the row and column decoder approach employed in the design of Milgrew et al. as shown in Fig. 7, whose complexity scales with array size) facilitate rapid acquisition of data from significantly large and dense arrays.

[0036] With respect to chemFET array fabrication, Applicants have further recognized and appreciated that various techniques employed in a conventional CMOS fabrication process, as well as various post-fabrication processing steps (wafer handling, cleaning, dicing, packaging, etc.), may in some instances adversely affect performance of the resulting chemFET array. For example, with reference again to Fig. 1, one potential issue relates to trapped charge that may be induced in the gate oxide 65 during etching of metals associated with the floating gate structure 70, and how such trapped charge may affect chemFET threshold voltage V_{TH}. Another potential issue relates to the density/porosity of the chemFET passivation layer (e.g., see ISFET passivation layer 72 in Fig. 1) resulting from low-temperature material deposition processes commonly employed in aluminum metal-based CMOS fabrication. While such low-temperature processes generally provide an adequate passivation layer for conventional CMOS devices, they may result in a somewhat low-density and porous passivation layer which may be potentially problematic for chemFETs in contact with an analyte solution; in particular, a low-density porous passivation layer over time may absorb and become saturated with analytes or other substances in the solution, which may in turn cause an undesirable time-varying drift in the chemFETs threshold voltage V_{TH}. This phenomenon in turn impedes accurate measurements of one or more particular analytes of interest. In view of the foregoing, other inventive embodiments disclosed herein relate to methods and apparatus which mitigate

potentially adverse effects on chemFET performance that may arise from various aspects of fabrication and post-fabrication processing/handling of chemFET arrays.

[0037] Accordingly, one embodiment of the present invention is directed to an apparatus, comprising an array of CMOS-fabricated sensors, each sensor comprising one chemically-sensitive field effect transistor (chemFET) and occupying an area on a surface of the array of ten micrometers by ten micrometers or less.

[0038] Another embodiment is directed to a sensor array, comprising a two-dimensional array of electronic sensors including at least 512 rows and at least 512 columns of the electronic sensors, each sensor comprising one chemically-sensitive field effect transistor (chemFET) configured to provide at least one output signal representing a presence and/or concentration of an analyte proximate to a surface of the two-dimensional array.

[0039] Another embodiment is directed to an apparatus, comprising an array of CMOS-fabricated sensors, each sensor comprising one chemically-sensitive field effect transistor (chemFET). The array of CMOS-fabricated sensors includes more than 256 sensors, and a collection of chemFET output signals from all chemFETs of the array constitutes a frame of data. The apparatus further comprises control circuitry coupled to the array and configured to generate at least one array output signal to provide multiple frames of data from the array at a frame rate of at least 1 frame per second. In one aspect, the frame rate may be at least 10 frames per second. In another aspect, the frame rate may be at least 20 frames per second. In yet other aspects, the frame rate may be at least 30, 40, 50, 70 or up to 100 frames per second.

[0040] Another embodiment is directed to an apparatus, comprising an array of CMOS-fabricated sensors, each sensor comprising a chemically-sensitive field effect transistor (chemFET). The chemFET comprises a floating gate structure, and a source and a drain having a first semiconductor type and fabricated in a region having a second semiconductor type, wherein there is no electrical conductor that electrically connects the region having the second semiconductor type to either the source or the drain.

[0041] Another embodiment is directed to an apparatus, comprising an array of electronic sensors, each sensor consisting of three field effect transistors (FETs) including one chemically-sensitive field effect transistor (chemFET).

[0042] Another embodiment is directed to an apparatus, comprising an array of electronic sensors, each sensor comprising three or fewer field effect transistors (FETs), wherein the three or fewer FETs includes one chemically-sensitive field effect transistor (chemFET).

[0043] Another embodiment is directed to an apparatus, comprising an array of electronic sensors, each sensor comprising a plurality of field effect transistors (FETs) including one chemically-sensitive field effect transistor (chemFET), and a plurality of electrical conductors electrically connected to the plurality of FETs, wherein the plurality of FETs are arranged such that the plurality of electrical conductors includes no more than four conductors traversing an area occupied by each sensor and interconnecting multiple sensors of the array.

[0044] Another embodiment is directed to an apparatus, comprising an array of CMOS-fabricated sensors, each sensor comprising a plurality of field effect transistors (FETs) including one chemically-sensitive field effect transistor (chemFET), wherein all of the FETs in each sensor are of a same channel type and implemented in a single semiconductor region of an array substrate.

[0045] Another embodiment is directed to a sensor array, comprising a plurality of electronic sensors arranged in a plurality of rows and a plurality of columns. Each sensor comprises one chemically-sensitive field effect transistor (chemFET) configured to provide at least one output signal representing a presence and/or a concentration of an analyte proximate to a surface of the array. For each column of the plurality of columns, the array further comprises column circuitry configured to provide a constant drain current and a constant drain-to-source voltage to respective chemFETs in the column, the column circuitry including two operational amplifiers and a diode-connected FET arranged in a Kelvin bridge configuration with the respective chemFETs to provide the constant drain-to-source voltage.

[0046] Another embodiment is directed to a sensor array, comprising a plurality of electronic sensors arranged in a plurality of rows and a plurality of columns. Each sensor comprises one chemically-sensitive field effect transistor (chemFET) configured to provide at least one output signal representing a concentration of ions in an analyte proximate to a surface of the array. The array further comprises at least one row select shift register to

enable respective rows of the plurality of rows, and at least one column select shift register to acquire chemFET output signals from respective columns of the plurality of columns.

[0047] Another embodiment is directed to an apparatus, comprising an array of CMOS-fabricated sensors, each sensor comprising a chemically-sensitive field effect transistor (chemFET). The chemFET comprises a floating gate structure, and a source and a drain having a first semiconductor type and fabricated in a region having a second semiconductor type, wherein there is no electrical conductor that electrically connects the region having the second semiconductor type to either the source or the drain. The array includes a two-dimensional array of at least 512 rows and at least 512 columns of the CMOS-fabricated sensors. Each sensor consists of three field effect transistors (FETs) including the chemFET, and each sensor includes a plurality of electrical conductors electrically connected to the three FETs. The three FETs are arranged such that the plurality of electrical conductors includes no more than four conductors traversing an area occupied by each sensor and interconnecting multiple sensors of the array. All of the FETs in each sensor are of a same channel type and implemented in a single semiconductor region of an array substrate. A collection of chemFET output signals from all chemFETs of the array constitutes a frame of data. The apparatus further comprises control circuitry coupled to the array and configured to generate at least one array output signal to provide multiple frames of data from the array at a frame rate of at least 20 frames per second.

[0048] Another embodiment is directed to a method for processing an array of CMOS-fabricated sensors, each sensor comprising a chemically-sensitive field effect transistor (chemFET). The method comprises: A) dicing a semiconductor wafer including the array to form at least one diced portion including the array; and B) performing a forming gas anneal on the at least one diced portion.

[0049] Another embodiment is directed to a method for processing an array of CMOS-fabricated sensors. Each sensor comprises a chemically-sensitive field effect transistor (chemFET) having a chemically-sensitive passivation layer of silicon nitride and/or silicon oxynitride deposited via plasma enhanced chemical vapor deposition (PECVD). The method comprises: A) depositing at least one additional passivation material on the chemically-sensitive passivation layer so as to reduce a porosity and/or increase a density of the passivation layer.

[0050] In another aspect, the invention provides a method for sequencing a nucleic acid comprising disposing a plurality of template nucleic acids into a plurality of reaction chambers, wherein the plurality of reaction chambers is in contact with a chemical-sensitive field effect transistor (chemFET) array comprising at least one chemFET for each reaction chamber, and wherein each of the template nucleic acids is hybridized to a sequencing primer and is bound to a polymerase, synthesizing a new nucleic acid strand by incorporating one or more known nucleotide triphosphates sequentially at the 3' end of the sequencing primer, detecting the incorporation of the one or more known nucleotide triphosphates by a change in current at the at least one chemFET.

[0051] In another aspect, the invention provides a method for sequencing a nucleic acid comprising disposing a plurality of template nucleic acids into a plurality of reaction chambers, wherein the plurality of reaction chambers is in contact with a chemical-sensitive field effect transistor (chemFET) array comprising at least one chemFET for each reaction chamber, and wherein each of the template nucleic acids is hybridized to a sequencing primer and is bound to a polymerase, synthesizing a new nucleic acid strand by incorporating one or more known nucleotide triphosphates sequentially at the 3' end of the sequencing primer, detecting the incorporation of the one or more known nucleotide triphosphates by a change in current at the at least one chemFET, wherein the chemFET array is any of the foregoing arrays.

[0052] In another aspect, the invention provides a method for sequencing a nucleic acid comprising disposing a plurality of template nucleic acids into a plurality of reaction chambers, wherein the plurality of reaction chambers is in contact with an chemical-sensitive field effect transistor (chemFET) array comprising at least one chemFET for each reaction chamber, and wherein each of the template nucleic acids is hybridized to a sequencing primer and is bound to a polymerase, synthesizing a new nucleic acid strand by incorporating one or more known nucleotide triphosphates sequentially at the 3' end of the sequencing primer, detecting the incorporation of the one or more known nucleotide triphosphates by the generation of sequencing reaction byproduct, wherein (a) the chemFET array comprises more than 256 sensors, or (b) a center-to-center distance between adjacent reaction chambers (or "pitch") is 1-10 μm.

[0053] Various embodiments apply equally to the methods disclosed herein and they are recited once for brevity. In some embodiments, the center-to-center distance between adjacent reaction chambers is about 2-9 μm, about 2 μm, about 5 μm, or about 9 μm. In some embodiments, the chemFET array comprises more than 256 sensors (and optionally more than 256 corresponding reaction chambers (or wells), more than 10^3 sensors (and optionally more than 10^3 corresponding reaction chambers), more than 10^4 sensors (and optionally more than 10^4 corresponding reaction chambers), more than 10^5 sensors (and optionally more than 10^5 corresponding reaction chambers), or more than 10^6 sensors (and optionally more than 10^6 corresponding reaction chambers). In some embodiments, the chemFET array comprises at least 512 rows and at least 512 columns of sensors.

[0054] In some embodiments, the sequencing reaction byproduct is inorganic pyrophosphate (PPi). In some embodiments, PPi is measured directly. In some embodiments, the PPi is measured in the absence of a PPi receptor. In some embodiments, the sequencing reaction byproduct is hydrogen ions. In some embodiments, the sequencing reaction byproduct is inorganic phosphate (Pi). In still other embodiments, the chemFET detects changes in any combination of the byproducts, optionally in combination with other parameters, as described herein.

[0055] In another aspect, the invention provides a method for sequencing a nucleic acid comprising disposing a plurality of template nucleic acids into a plurality of reaction chambers, wherein the plurality of reaction chambers is in contact with an chemical-sensitive field effect transistor (chemFET) array comprising at least one chemFET for each reaction chamber, and wherein each of the template nucleic acids is hybridized to a sequencing primer and is bound to a polymerase, synthesizing a new nucleic acid strand by incorporating one or more known nucleotide triphosphates sequentially at the 3' end of the sequencing primer, directly detecting release of inorganic pyrophosphate (PPi) as an indicator of incorporation of the one or more known nucleotide triphosphates.

[0056] In some embodiments, the PPi is directly detected by binding to a PPi receptor immobilized on the chemFET. In some embodiments, the PPi is directly detected by the chemFET in the absence of a PPi receptor.

[0057] In another aspect, the invention provides a method for sequencing nucleic acids comprising fragmenting a template nucleic acid to generate a plurality of fragmented

nucleic acids, attaching one strand from each of the plurality of fragmented nucleic acids individually to beads to generate a plurality of beads each having a single stranded fragmented nucleic acid attached thereto, delivering the plurality of beads having a single stranded fragmented nucleic acid attached thereto to a chemFET array having a separate reaction chamber for each sensor in the area, and wherein only one bead is situated in each reaction chamber, and performing a sequencing reaction simultaneously in the plurality of chambers.

[0058] In another aspect, the invention provides an apparatus comprising a chemical-sensitive field effect transistor (chemFET) having disposed on its surface a PPi receptor.

[0059] In some embodiments, the PPi selective receptor is Compound 1, Compound 2, Compound 3, Compound 4, Compound 5, Compound 6, Compound 7, Compound 8, Compound 9 or Compound 10 as shown in Fig. 11B. In some embodiments, the chemFET is present in an array of chemFETs, each of which has disposed on its surface a PPi selective receptor. In some embodiments, the identical PPi selective receptors are disposed on each chemFET of the array. In some embodiments, the array comprises more than 256 sensors. In some embodiments, the array comprises at least 512 rows and at least 512 columns of sensors. In some embodiments, the chemFET is located at a bottom of a reaction chamber.

[0060] In another aspect, the invention provides an apparatus comprising a chemical-sensitive field effect transistor (chemFET) array having disposed on its surface a biological array.

[0061] The biological array may be a nucleic acid array, a protein array including but not limited to an enzyme array, an antibody array and an antibody fragment array, a cell array, and the like. The chemical array may be an organic small molecule array, or an inorganic molecule array, but it is not so limited. The chemFET array may comprise at least 5, 10, 10^2, 10^3, 10^4, 10^5, 10^6 or more sensors. The biological or chemical array may be arranged into a plurality of "cells" or spatially defined regions and each of these regions is situated over a different sensor in the chemFET array, in some embodiments.

[0062] In yet another aspect, the invention provides a method for detecting a nucleic acid comprising contacting a nucleic acid array disposed on a chemFET array with a sample, and

detecting binding of a nucleic acid from the sample to one or more regions on the nucleic acid array.

[0063] In another aspect, the invention provides a method for detecting a protein comprising contacting a protein array disposed on a chemFET array with a sample, and detecting binding of a protein from the sample to one or more regions on the protein array.

[0064] In yet another aspect, the invention provides a method for detecting a nucleic acid comprising contacting a protein array disposed on a chemFET array with a sample, and detecting binding of a nucleic acid from the sample to one or more regions on the protein array.

[0065] In another aspect, the invention provides a method for detecting an antigen comprising contacting an antibody array disposed on a chemFET array with a sample, and detecting binding of a antigen from the sample to one or more regions on the antibody array.

[0066] In another aspect, the invention provides a method for detecting an enzyme substrate or inhibitor comprising contacting an enzyme array disposed on a chemFET array with a sample, and detecting binding of an entity from the sample to one or more regions on the enzyme array.

[0067] It should be appreciated that all combinations of the foregoing concepts and additional concepts discussed in greater detail below (provided such concepts are not mutually inconsistent) are contemplated as being part of the inventive subject matter disclosed herein. In particular, all combinations of claimed subject matter appearing at the end of this disclosure are contemplated as being part of the inventive subject matter disclosed herein. It should also be appreciated that terminology explicitly employed herein that also may appear in any disclosure incorporated by reference should be accorded a meaning most consistent with the particular concepts disclosed herein.

Brief Description of the Drawings

[0068] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead being placed upon generally illustrating the various concepts discussed herein.

[0069] Fig. 1 illustrates a cross-section of a p-type (p-channel) ion-sensitive field effect transistor (ISFET) fabricated using a conventional CMOS process.

[0070] Fig. 2 illustrates an electric circuit representation of the p-channel ISFET shown in Fig. 1.

[0071] Fig. 3 illustrates one column of a two-dimensional ISFET array based on the ISFET shown in Fig. 1.

[0072] Fig. 4 illustrates a transmission gate including a p-channel MOSFET and an n-channel MOSFET that is employed in each pixel of the array column shown in Fig. 3.

[0073] Fig. 5 is a diagram similar to Fig. 1, illustrating a wider cross-section of a portion of a substrate corresponding to one pixel of the array column shown in Fig. 3, in which the ISFET is shown alongside two n-channel MOSFETs also included in the pixel.

[0074] Fig. 6 is a diagram similar to Fig. 5, illustrating a cross-section of another portion of the substrate corresponding to one pixel of the array column shown in Fig. 3, in which the ISFET is shown alongside the p-channel MOSFET of the transmission gate shown in Fig. 4.

[0075] Fig. 7 illustrates an example of a complete two-dimensional ISFET pixel array based on the column design of Fig. 3, together with accompanying row and column decoder circuitry and measurement readout circuitry.

[0076] Fig. 8 generally illustrates a nucleic acid processing system comprising a large scale chemFET array, according to one inventive embodiment of the present disclosure.

[0077] Fig. 9 illustrates one column of an chemFET array similar to that shown in Fig. 8, according to one inventive embodiment of the present disclosure.

[0078] Fig. 9A illustrates a circuit diagram for an exemplary amplifier employed in the array column shown in Fig. 9, and Fig. 9B is a graph of amplifier bias vs. bandwidth, according to one inventive embodiment of the present disclosure.

[0079] Fig. 10 illustrates a top view of a chip layout design for a pixel of the column of an chemFET array shown in Fig. 9, according to one inventive embodiment of the present disclosure.

[0080] Fig. 11A shows a composite cross-sectional view along the line I--I of the pixel shown in Fig. 10, including additional elements on the right half of Fig. 10 between the

lines II--II and III--III, illustrating a layer-by-layer view of the pixel fabrication according to one inventive embodiment of the present disclosure.

[0081] Fig. 11B provides the chemical structures of ten PPi receptors (compounds 1 through 10).

[0082] Fig. 11C is a schematic of a synthesis protocol for compound 4 from Fig. 11B.

[0083] Fig. 11D is a schematic illustrating a variety of chemistries that can be applied to the passivation layer in order to bind molecular recognition compounds (such as but not limited to PPi receptors).

[0084] Fig. 11E is a schematic of attachment of compound 10 from Fig. 11B to a metal oxide surface.

[0085] Figs. 12A through 12L provide top views of each of the fabrication layers shown in Fig. 11A, according to one inventive embodiment of the present disclosure.

[0086] Fig. 13 illustrates a block diagram of an exemplary CMOS IC chip implementation of an chemFET sensor array similar to that shown in Fig. 8, based on the column and pixel designs shown in Figs. 9-12, according to one inventive embodiment of the present disclosure.

[0087] Fig. 14 illustrates a row select shift register of the array shown in Fig. 13, according to one inventive embodiment of the present disclosure.

[0088] Fig. 15 illustrates one of two column select shift registers of the array shown in Fig. 13, according to one inventive embodiment of the present disclosure.

[0089] Fig. 16 illustrates one of two output drivers of the array shown in Fig. 13, according to one inventive embodiment of the present disclosure.

[0090] Fig. 17 illustrates a block diagram of the chemFET sensor array of Fig. 13 coupled to an array controller, according to one inventive embodiment of the present disclosure.

[0091] Fig. 18 illustrates an exemplary timing diagram for various signals provided by the array controller of Fig. 17, according to one inventive embodiment of the present disclosure.

[0092] Figs. 19-20 illustrate block diagrams of alternative CMOS IC chip implementations of chemFET sensor arrays, according to other inventive embodiments of the present disclosure.

[0093] Fig. 20A illustrates a top view of a chip layout design for a pixel of the chemFET array shown in Fig. 20, according to another inventive embodiment of the present disclosure.

[0094] Figs. 21-23 illustrate block diagrams of additional alternative CMOS IC chip implementations of chemFET sensor arrays, according to other inventive embodiments of the present disclosure.

[0095] Fig. 24 illustrates the pixel design of Fig. 9 implemented with an n-channel chemFET and accompanying n-channel MOSFETs, according to another inventive embodiment of the present disclosure.

[0096] Figs. 25-27 illustrate alternative pixel designs and associated column circuitry for chemFET arrays according to other inventive embodiments of the present disclosure.

[0097] Figs. 28A and 28B are isometric illustrations of portions of microwell arrays as employed herein, showing round wells and rectangular wells, to assist three-dimensional visualization of the array structures.

[0098] Fig. 29 is a diagrammatic depiction of a top view of one corner (i.e., the lower left corner) of the layout of a chip showing an array of individual ISFET sensors on a CMOS die.

[0099] Fig. 30 is an illustration of an example of a layout for a portion of a (typically chromium) mask for a one-sensor-per-well embodiment of the above-described sensor array, corresponding to the portion of the die shown in Fig. 29.

[00100] Fig. 31 is a corresponding layout for a mask for a 4-sensors-per-well embodiment.

[00101] Fig. 32 is an illustration of a second mask used to mask an area which surrounds the array, to build a collar or wall (or basin, using that term in the geological sense) of resist which surrounds the active array of sensors on a substrate, as shown in Fig. 33A.

[00102] Fig. 33 is an illustration of the resulting basin.

[00103] Fig. 33A is an illustration of a three-layer PCM process for making the microwell array.

[00104] Figs. 34 - 37 diagrammatically illustrate a first example of a suitable experiment apparatus incorporating a fluidic interface with the sensor array, with Fig. 35 providing a cross-section through the Fig. 34 apparatus along section line 35-35' and Fig. 36 expanding part of Fig. 35, in perspective, and Fig. 37 further expanding a portion of the structure to make the fluid flow more visible.

[00105] Fig. 38 is a diagrammatic illustration of a substrate with an etched photoresist layer beginning the formation of an example flow cell of a certain configuration.

[00106] Figs. 39 - 41 are diagrams of masks suitable for producing a first configuration of flow cell consistent with Fig. 38.

[00107] Figs. 42 - 54 and 57-58 are pairs of partly isometric, sectional views of example apparatus and enlargements, showing ways of introducing a reference electrode into, and forming, a flow cell and flow chamber, using materials such as plastic and PDMS.

[00108] Figs. 55 and 56 are schematic, cross-sectional views of two-layer glass (or plastic) arrangements for manufacturing fluidic apparatus for mounting onto a chip for use as taught herein.

[00109] Figs. 59A-59C are illustrations of the pieces for two examples of two-piece injection molded parts for forming a flow cell.

[00110] Fig. 60 is a schematic illustration, in cross-section, for introducing a stainless steel capillary tube as an electrode, into a downstream port of a flow cell such as the flow cells of Figs. 59A - 59C, or other flow cells.

[00111] Fig. 61 is a schematic illustrating the incorporation of a dNTP into a synthesized nucleic acid strand with concomitant release of inorganic pyrophosphate (PPi).

[00112] Figs. 62-70 illustrate bead loading into the microfluidic arrays of the invention.

[00113] Fig. 71A is a screen capture showing pixels with signal occurring after dATP was added (first) resulting in a 4 base extension in template 4 (see Tables 1 and 2) (left panel) and a plot of voltage versus frame (or time) for the arrowed pixels (right panel).

[00114] Fig. 71B is a screen capture showing pixels with signal occurring after dCTP was added next resulting in a 4 base extension in template 1 (see Tables 1, 2) (left panel) and a plot of voltage versus frame (or time) for the arrowed pixels (right panel).

[00115] Fig. 71C is a screen capture showing pixels with signal occurring after dGTP was added next resulting in extension of templates 1, 2 and 4 (see Tables 1, 2) (left panel) and a plot of voltage versus frame (or time) for the arrowed pixels (right panel).

[00116] Fig. 71D is a screen capture showing pixels with signal occurring after dTTP was added and run-off occurred (due the presence of all 4 dNTP) in all 4 templates (see Tables 1, 2) (left panel) and a plot of voltage versus frame (or time) for the arrowed pixels (right panel).

Detailed Description

[00117] Following below are more detailed descriptions of various concepts related to, and embodiments of, inventive methods and apparatus relating to large scale chemFET arrays for analyte measurements. It should be appreciated that various concepts introduced above and discussed in greater detail below may be implemented in any of numerous ways, as the disclosed concepts are not limited to any particular manner of implementation. Examples of specific implementations and applications are provided primarily for illustrative purposes.

[00118] Various inventive embodiments according to the present disclosure are directed at least in part to a semiconductor-based / microfluidic hybrid system that combines the power of microelectronics with the biocompatibility of a microfluidic system. In some examples below, the microelectronics portion of the hybrid system is implemented in CMOS technology for purposes of illustration. It should be appreciated, however, that the disclosure is not intended to be limiting in this respect, as other semiconductor-based technologies may be utilized to implement various aspects of the microelectronics portion of the systems discussed herein.

[00119] One embodiment disclosed herein is directed to a large sensor array (e.g., a two-dimensional array) of chemically-sensitive field effect transistors (chemFETs), wherein the individual chemFET sensor elements or "pixels" of the array are configured to detect analyte concentration changes in a host of chemical and/or biological processes (chemical

reactions, cell cultures, neural activity, nucleic acid sequencing processes, etc.) occurring in proximity to the array. Examples of chemFETs contemplated by various embodiments discussed in greater detail below include, but are not limited to, ion-sensitive field effect transistors (ISFETs) and enzyme-sensitive field effect transistors (ENFETs). In one exemplary implementation, one or more microfluidic structures is/are fabricated above the chemFET sensor array to provide for containment and/or confinement of a chemical reaction in which an analyte of interest may be produced. For example, in one implementation, the microfluidic structure(s) may be configured as one or more "wells" (e.g., small reaction chambers) disposed above one or more sensors of the array, such that the one or more sensors over which a given well is disposed detect and measure analyte concentration in the given well.

[00120] In some embodiments, such a chemFET array/microfluidics hybrid structure may be used to analyze solution(s)/material(s) of interest containing nucleic acids. For example, such structures may be employed to process nucleic acids in a multitude of ways that utilize sequencing of nucleic acids. In various aspects, such sequencing can be performed to determine the identity of a sequence of nucleic acids, for single nucleotide polymorphism detection in nucleic acid fragments, for nucleic acid expression profiling (comparing the nucleic acid expression profile between two or more states--e.g., comparing between diseased and normal tissue or comparing between untreated tissue and tissue treated with drug, enzymes, radiation or chemical treatment), for haplotyping (comparing genes or variations in genes on each of the two alleles present in a human subject), for karyotyping (diagnostically comparing one or more genes in a test tissue--typically from an embryo/fetus prior to conception to detect birth defects--with the same genes from "normal" karyotyped subjects), and for genotyping (comparing one or more genes in a first individual of a species with the same genes in other individuals of the same species). It should be appreciated, however, that while some illustrative examples of the concepts disclosed herein are applied in the context of nucleic acid processing, application of the concepts disclosed herein relating to chemFET sensor arrays is not limited to these examples.

[00121] Fig. 8 generally illustrates a nucleic acid processing system 1000 comprising a large scale chemFET array, according to one inventive embodiment of the present disclosure. In the discussion that follows, the chemFET sensors of the array are described for purposes of illustration as ISFETs configured for sensitivity to hydrogen ion

concentration. However, it should be appreciated that the present disclosure is not limited in this respect, and that in any of the embodiments discussed herein in which ISFETs are employed as an illustrative example, other types of chemFETs may be similarly employed in alternative embodiments, as discussed in further detail below. In one aspect, the system 1000 includes a semiconductor/microfluidics hybrid structure 300 comprising an ISFET sensor array 100 and a microfluidics flow cell 200. In another aspect, the flow cell 200 is configured to facilitate the sequencing of a nucleic acid template disposed in the flow cell via the controlled admission to the flow cell of a number of sequencing reagents 272 (e.g., bases dATP, dCTP, dGTP, dTTP and other reagents). As illustrated in Fig. 8, the admission of the sequencing reagents to the flow cell 200 may be accomplished via one or more valves 270 and one or more pumps 274 that are controlled by computer 260.

[00122] In the system 1000 of Fig. 8, according to one embodiment the ISFET sensor array 100 monitors pH changes occurring in different portions of the flow cell 200 due to chemical reactions between one or more of the bases constituting the sequencing reagents 272 and the nucleic acid template. In other embodiments discussed in greater detail below, the FET sensor array may be particularly configured for sensitivity to other analytes that may provide relevant information about the chemical reactions of interest. Via an array controller 250 (also under operation of the computer 260), the ISFET array may be controlled so as to acquire data relating to analyte measurements, and collected data may be processed by the computer 260 to yield meaningful information associated with the processing of the nucleic acid template. For example, in one implementation, pH change generally is proportional to the number of a particular type of base (e.g., one of dATP, dCTP, dGTP, dTTP) added to the nucleic acid template. Such a pH change may be represented by a change in output voltage of one or more ISFETs of the array 100 in proximity to the reaction(s) between a given type of base and the template. Thus, the magnitude of the voltage change in an output signal of a given pixel of the array may be used to determine the number of bases of a particular type added to the template disposed in the flow cell above the given pixel.

[00123] In one aspect, the flow cell 200 of the system 1000 shown in Fig. 8 may comprise a number of wells (not shown in Fig. 8) disposed above corresponding sensors of the ISFET array 100. A number of techniques may be used to admit the various processing materials to the wells of such a flow cell. For example, the flow cell first may be loaded with a

nucleic acid template to be sequenced by centrifuging into the wells "beads" containing the nucleic acid template; alternatively, such beads may enter the wells by gravity. In another example, instead of employing beads, the wells can be coated with a set of primer pairs, and the nucleic acid template provided to the flow cell with adapters that complement the primer pairs (immobilization materials can be added to the sensor array 100, or to individual dies as part of the chip packaging, or immediately before the processing of the nucleic acid). Other methods involving solgels may be used to immobilize a nucleic acid template near the surface of the ISFET array 100.

[00124] Once a nucleic acid template is loaded into respective wells of the flow cell 200, bridge amplification can then be performed in the wells, the product denatured, and sequencing by synthesis or ligation then performed. Other methods of amplification in the wells (with the products captured in the wells) are envisioned, including rolling circle amplification, or other strategies using isothermal or non-isothermal amplification techniques such as PCR. As illustrated in Fig. 8, reagents including bases may be admitted to the flow cell (e.g., via the computer controlled valve 270 and pumps 274) and diffuse into the wells, or reagents may be added to the flow cell by other means such as an ink jet. In yet another example, the flow cell 200 may not contain any wells, and diffusion properties of the reagents may be exploited to limit cross-talk between respective sensors of the ISFET array 100.

[00125] In sum, the flow cell 200 in the system of Fig. 8 may be configured in a variety of manners to provide one or more analytes in proximity to the ISFET array 100; for example, a nucleic acid template (DNA) may be directly attached or applied in suitable proximity to one or more pixels of the sensor array 100, or on a support material (e.g., one or more "beads") located above the sensor array. Processing reagents (e.g., enzymes) can also be placed on the sensors directly, or on one or more solid supports in proximity to the array, and the device used without wells or beads for a number of biosensor applications where the enzymes result in a sensor-detectable product (e.g., ion concentration change).

[00126] With respect to the ISFET array 100 of the system 1000 shown in Fig. 8, in one embodiment the array 100 is implemented as an integrated circuit designed and fabricated using standard CMOS processes (e.g., 0.35 micrometer process, 0.18 micrometer process), comprising all the sensors and electronics needed to monitor/measure one or more analytes.

With reference again to Fig. 1, one or more reference electrodes 76 to be employed in connection with the ISFET array 100 may be placed in the flow cell 200 (e.g., disposed in "unused" wells of the flow cell) or otherwise exposed to a reference (e.g., one or more of the sequencing reagents 172) to establish a base line against which changes in analyte concentration proximate to respective ISFETs of the array 100 are compared. The reference electrode(s) 76 may be electrically coupled to the array 100, the array controller 250 or directly to the computer 260 to facilitate analyte measurements based on voltage signals obtained from the array 100; in some implementations, the reference electrode(s) may be coupled to an electric ground or other predetermined potential, or the reference electrode voltage may be measured with respect to ground, to establish an electric reference for ISFET output signal measurements, as discussed further below.

[00127] The ISFET array 100 is not limited to any particular size, as one- or two-dimensional arrays, including as few as two to 256 pixels (e.g., 16 by 16 pixels in a two-dimensional implementation) or as many as 54 mega-pixels (e.g., 7400 by 7400 pixels in a two-dimensional implementation) or even greater may be fabricated and employed for various chemical/biological analysis purposes pursuant to the concepts disclosed herein. In one embodiment of the exemplary system shown in Fig. 8, the individual ISFET sensors of the array may be configured for sensitivity to hydrogen ions; however, it should also be appreciated that the present disclosure is not limited in this respect, as individual sensors of an ISFET sensor array may be particularly configured for sensitivity to other types of ion concentrations for a variety of applications (materials sensitive to other ions such as sodium, silver, iron, bromine, iodine, calcium, and nitrate, for example, are known).

[00128] More generally, a chemFET array according to various embodiments of the present disclosure may be configured for sensitivity to any one or more of a variety of analytes/chemical substances. In one embodiment, one or more chemFETs of an array may be particularly configured for sensitivity to one or more analytes representing one or more binding events (e.g., associated with a nucleic acid sequencing process), and in other embodiments different chemFETs of a given array may be configured for sensitivity to different analytes. For example, in one embodiment, one or more sensors (pixels) of the array may include a first type of chemFET configured to be chemically sensitive to a first analyte, and one or more other sensors of the array may include a second type of chemFET configured to be chemically sensitive to a second analyte different from the first analyte. In

one exemplary implementation, the first analyte may represent a first binding event associated with a nucleic acid sequencing process, and the second analyte may represent a second binding event associated with the nucleic acid sequencing process. Of course, it should be appreciated that more than two different types of chemFETs may be employed in any given array to detect and/or measure different types of analytes/binding events. In general, it should be appreciated in any of the embodiments of sensor arrays discussed herein that a given sensor array may be "homogeneous" and include chemFETs of substantially similar or identical types to detect and/or measure a same type of analyte (e.g., pH or other ion concentration), or a sensor array may be "heterogeneous" and include chemFETs of different types to detect and/or measure different analytes. For simplicity of discussion, again the example of an ISFET is discussed below in various embodiments of sensor arrays, but the present disclosure is not limited in this respect, and several other options for analyte sensitivity are discussed in further detail below (e.g., in connection with Fig. 11A).

[00129] In exemplary implementations based on 0.35 micrometer CMOS processing techniques (or CMOS processing techniques capable of smaller feature sizes), each pixel of the ISFET array 100 may include an ISFET and accompanying enable/select components, and may occupy an area on a surface of the array of approximately ten micrometers by ten micrometers (i.e., 100 micrometers^2) or less; stated differently, arrays having a pitch (pixel-to-pixel spacing) on the order of 10 micrometers or less may be realized. An array pitch on the order of 10 micrometers or less using a 0.35 micrometer CMOS processing technique constitutes a significant improvement in terms of size reduction with respect to prior attempts to fabricate ISFET arrays, which resulted in pixel sizes on the order of at least 12 micrometers or greater.

[00130] More specifically, in some embodiments discussed further below based on the inventive concepts disclosed herein, an array pitch of approximately nine (9) micrometers allows an ISFET array including over 256,000 pixels (i.e., a 512 by 512 array), together with associated row and column select and bias/readout electronics, to be fabricated on a 7 millimeter by 7 millimeter semiconductor die, and a similar sensor array including over four million pixels (i.e., a 2048 by 2048 array, over 4 Mega-pixels) to be fabricated on a 21 millimeter by 21 millimeter die. In other examples, an array pitch of approximately 5 micrometers allows an ISFET array including approximately 1.55 Mega-pixels (i.e., a 1348

by 1152 array) and associated electronics to be fabricated on a 9 millimeter by 9 millimeter die, and an ISFET sensor array including over 14 Mega-pixels and associated electronics on a 22 millimeter by 20 millimeter die. In yet other implementations, using a CMOS fabrication process in which feature sizes of less than 0.35 micrometers are possible (e.g., 0.18 micrometer CMOS processing techniques), ISFET sensor arrays with a pitch significantly below 5 micrometers may be fabricated (e.g., array pitch of 2.6 micrometers or pixel area of less than 8 or 9 micrometers^2), providing for significantly dense ISFET arrays. Of course, it should be appreciated that pixel sizes greater than 10 micrometers (e.g., on the order of approximately 20, 50, 100 micrometers or greater) may be implemented in various embodiments of chemFET arrays according to the present disclosure.

[00131] In other aspects of the system shown in Fig. 8, one or more array controllers 250 may be employed to operate the ISFET array 100 (e.g., selecting/enabling respective pixels of the array to obtain output signals representing analyte measurements). In various implementations, one or more components constituting one or more array controllers may be implemented together with pixel elements of the arrays themselves, on the same integrated circuit (IC) chip as the array but in a different portion of the IC chip, or off-chip. In connection with array control, analog-to-digital conversion of ISFET output signals may be performed by circuitry implemented on the same integrated circuit chip as the ISFET array, but located outside of the sensor array region (locating the analog to digital conversion circuitry outside of the sensor array region allows for smaller pitch and hence a larger number of sensors, as well as reduced noise). In various exemplary implementations discussed further below, analog-to-digital conversion can be 4-bit, 8-bit, 12-bit, 16-bit or other bit resolutions depending on the signal dynamic range required.

[00132] Having provided a general overview of the role of a chemFET (e.g., ISFET) array 100 in an exemplary system 1000 for measuring one or more analytes in connection with nucleic acid processing, following below are more detailed descriptions of exemplary chemFET arrays according to various inventive embodiments of the present disclosure that may be employed in a variety of applications including, but not limited to, nucleic acid processing. Again, for purposes of illustration, chemFET arrays according to the present disclosure are discussed below using the particular example of an ISFET array, but other types of chemFETs may be employed in alternative embodiments.

[00133] An noted above, various inventive embodiments disclosed herein specifically improve upon the ISFET array design of Milgrew et al. discussed above in connection with Figs. 1-7, as well as other prior ISFET array designs, so as to significantly reduce pixel size and array pitch, and thereby increase the number of pixels of an ISFET array for a given semiconductor die size (i.e., increase pixel density). In some implementations, an increase in pixel density is accomplished while at the same time increasing the signal-to-noise ratio (SNR) of output signals corresponding to respective measurements relating to one or more chemical properties of one or more analytes and the speed with which such output signals may be read from the array. In particular, Applicants have recognized and appreciated that by relaxing requirements for ISFET linearity and focusing on a more limited signal output/measurement range (e.g., signal outputs corresponding to a pH range of from approximately 7 to 9 rather than 1 to 14), individual pixel complexity and size may be significantly reduced, thereby facilitating the realization of very large scale dense ISFET arrays.

[00134] To this end, Fig. 9 illustrates one column 102_j of an ISFET array 100, according to one inventive embodiment of the present disclosure, in which ISFET pixel design is appreciably simplified to facilitate small pixel size. The column 102_j includes n pixels, the first and last of which are shown in Fig. 9 as the pixels 105_1 and 105_n. As discussed further below in connection with Fig. 13, a complete two-dimensional ISFET array 100 based on the column design shown in Fig. 9 includes m such columns 102_j ($j = 1, 2, 3, \ldots m$) with successive columns of pixels generally arranged side by side.

[00135] In one aspect of the embodiment shown in Fig. 9, each pixel 105_1 through 105_n of the column 102_j includes only three components, namely, an ISFET 150 (also labeled as Q1) and two MOSFET switches Q2 and Q3. The MOSFET switches Q2 and Q3 are both responsive to one of n row select signals ($\overline{\text{RowSel}_1}$ through $\overline{\text{RowSel}_n}$, logic low active) so as to enable or select a given pixel of the column 102_j. Using pixel 105_1 as an example that applies to all pixels of the column, the transistor switch Q3 couples a controllable current source 106_j via the line 112_1 to the source of the ISFET 150 upon receipt of the corresponding row select signal via the line 118_1. The transistor switch Q2 couples the source of the ISFET 150 to column bias/readout circuitry 110_j via the line 114_1 upon receipt of the corresponding row select signal. The drain of the ISFET 150 is directly coupled via

the line 116_1 to the bias/readout circuitry 110_j. Thus, only four signal lines per pixel, namely the lines 112_1, 114_1, 116_1 and 118_1, are required to operate the three components of the pixel 105_1. In an array of *m* columns, a given row select signal is applied simultaneously to one pixel of each column (e.g., at same positions in respective columns).

[00136] As illustrated in Fig. 9, the design for the column 102_j according to one embodiment is based on general principles similar to those discussed above in connection with the column design of Milgrew et al. shown Fig. 3. In particular, the ISFET of each pixel, when enabled, is configured with a constant drain current I_{Dj} and a constant drain-to-source voltage V_{DSj} to obtain an output signal V_{Sj} from an enabled pixel according to Eq. (3) above. To this end, the column 102_j includes a controllable current source 106_j, coupled to an analog circuitry positive supply voltage VDDA and responsive to a bias voltage VB1, that is shared by all pixels of the column to provide a constant drain current I_{Dj} to the ISFET of an enabled pixel. In one aspect, the current source 106_j is implemented as a current mirror including two long-channel length and high output impedance MOSFETs. The column also includes bias/readout circuitry 110_j that is also shared by all pixels of the column to provide a constant drain-to-source voltage to the ISFET of an enabled pixel. The bias/readout circuitry 110_j is based on a Kelvin Bridge configuration and includes two operational amplifiers 107A (A1) and 107B (A2) configured as buffer amplifiers and coupled to analog circuitry positive supply voltage VDDA and the analog supply voltage ground VSSA. The bias/readout circuitry also includes a controllable current sink 108_j (similar to the current source 106j) coupled to the analog ground VSSA and responsive to a bias voltage VB2, and a diode-connected MOSFET Q6. The bias voltages VB1 and VB2 are set/controlled in tandem to provide a complimentary source and sink current. The voltage developed across the diode-connected MOSFET Q6 as a result of the current drawn by the current sink 108_j is forced by the operational amplifiers to appear across the drain and source of the ISFET of an enabled pixel as a constant drain-source voltage V_{DSj}.

[00137] By employing the diode-connected MOSFET Q6 in the bias/readout circuitry 110_j of Fig. 9, rather than the resistor R_{SDj} as shown in the design of Milgrew et al. illustrated in Fig. 3, a significant advantage is provided in a CMOS fabrication process; specifically, matching resistors can be fabricated with error tolerances generally on the order of ±20%, whereas MOSFET matching in a CMOS fabrication process is on the order of ±1% or better. The degree to which the component responsible for providing a constant

ISFET drain-to-source voltage V_{DSj} can be matched from column to column significantly affects measurement accuracy (e.g., offset) from column to column. Thus, employing the MOSFET Q6 rather than a resistor appreciably mitigates measurement offsets from column-to-column. Furthermore, whereas the thermal drift characteristics of a resistor and an ISFET may be appreciably different, the thermal drift characteristics of a MOSFET and ISFET are substantially similar, if not virtually identical; hence, any thermal drift in MOSFET Q6 virtually cancels any thermal drift from ISFET Q1, resulting in greater measurement stability with changes in array temperature.

[00138] In Fig. 9, the column bias/readout circuitry 110j also includes sample/hold and buffer circuitry to provide an output signal V_{COLj} from the column. In particular, after one of the pixels 105_1 through 105_n is enabled or selected via the transistors Q2 and Q3 in each pixel, the output of the amplifier 107A (A1), i.e., a buffered V_{Sj}, is stored on a column sample and hold capacitor C_{sh} via operation of a switch (e.g., a transmission gate) responsive to a column sample and hold signal COL SH. Examples of suitable capacitances for the sample and hold capacitor include, but are not limited to, a range of from approximately 500fF to 2pF. The sampled voltage is buffered via a column output buffer amplifier 111j (BUF) and provided as the column output signal V_{COLj}. As also shown in Fig. 9, a reference voltage VREF may be applied to the buffer amplifier 111j, via a switch responsive to a control signal CAL, to facilitate characterization of column-to-column non-uniformities due to the buffer amplifier 111j and thus allow post-read data correction.

[00139] Fig. 9A illustrates an exemplary circuit diagram for one of the amplifiers 107A of the bias/readout circuitry 110j (the amplifier 107B is implemented identically), and Fig. 9B is a graph of amplifier bias vs. bandwidth for the amplifiers 107A and 107B. As shown in Fig. 9A, the amplifier 107A employs an arrangement of multiple current mirrors based on nine MOSFETs (M1 through M9) and is configured as a unity gain buffer, in which the amplifier's inputs and outputs are labeled for generality as IN+ and VOUT, respectively. The bias voltage VB4 (representing a corresponding bias current) controls the transimpedance of the amplifier and serves as a bandwidth control (i.e., increased bandwidth with increased current). With reference again to Fig. 9, due to the sample and hold capacitor C_{sh}, the output of the amplifier 107A essentially drives a filter when the sample and hold switch is closed. Accordingly, to achieve appreciably high data rates, the bias voltage VB4 may be adjusted to provide higher bias currents and increased amplifier

bandwidth. From Fig. 9B, it may be observed that in some exemplary implementations, amplifier bandwidths of at least 40 MHz and significantly greater may be realized. In some implementations, amplifier bandwidths as high as 100 MHz may be appropriate to facilitate high data acquisition rates and relatively lower pixel sample or "dwell" times (e.g., on the order of 10 to 20 microseconds).

[00140] In another aspect of the embodiment shown in Fig. 9, unlike the pixel design of Milgrew et al. shown in Fig. 3, the pixels 105_1 through 105_n do not include any transmission gates or other devices that require both n-channel and p-channel FET components; in particular, the pixels 105_1 through 105_n of this embodiment include only FET devices of a same type (i.e., only n-channel or only p-channel). For purposes of illustration, the pixels 105_1 and 105_n illustrated in Fig. 9 are shown as comprising only p-channel components, i.e., two p-channel MOSFETs Q2 and Q3 and a p-channel ISFET 150. By not employing a transmission gate to couple the source of the ISFET to the bias/readout circuitry 110_j, some dynamic range for the ISFET output signal (i.e., the ISFET source voltage V_S) may be sacrificed. However, Applicants have recognized and appreciated that by potentially foregoing some output signal dynamic range (and thereby potentially limiting measurement range for a given chemical property, such as pH), the requirement of different type FET devices (both n-channel and p-channel) in each pixel may be eliminated and the pixel component count reduced. As discussed further below in connection with Figs. 10-12, this significantly facilitates pixel size reduction. Thus, in one aspect, there is a beneficial tradeoff between reduced dynamic range and smaller pixel size.

[00141] In yet another aspect of the embodiment shown in Fig. 9, unlike the pixel design of Milgrew et al., the ISFET 150 of each pixel 105_1 through 105_n does not have its body connection tied to its source (i.e., there is no electrical conductor coupling the body connection and source of the ISFET such that they are forced to be at the same electric potential during operation). Rather, the body connections of all ISFETs of the array are tied to each other and to a body bias voltage V_{BODY}. While not shown explicitly in Fig. 9, the body connections for the MOSFETs Q2 and Q3 likewise are not tied to their respective sources, but rather to the body bias voltage V_{BODY}. In one exemplary implementation based on pixels having all p-channel components, the body bias voltage V_{BODY} is coupled to the highest voltage potential available to the array (e.g., VDDA), as discussed further below in connection with Fig. 17.

[00142] By not tying the body connection of each ISFET to its source, the possibility of some non-zero source-to-body voltage V_{SB} may give rise to the "body effect," as discussed above in connection with Fig. 1, which affects the threshold voltage V_{TH} of the ISFET according to a nonlinear relationship (and thus, according to Eq. (3), may affect measurements of chemical properties, such as pH). However, Applicants have recognized and appreciated that by focusing on a reduced ISFET output signal dynamic range, any body effect that may arise in the ISFET from a non-zero source-to-body voltage may be relatively minimal. Thus, any measurement nonlinearity that may result over the reduced dynamic range may be ignored as insignificant or taken into consideration and compensated (e.g., via array calibration and data processing techniques, as discussed further below in connection with Fig. 17). Applicants have also recognized and appreciated that by not tying each ISFET source to its body connection, all of the FETs constituting the pixel may share a common body connection, thereby further facilitating pixel size reduction, as discussed further below in connection with Figs. 10-12. Accordingly, in another aspect, there is a beneficial tradeoff between reduced linearity and smaller pixel size.

[00143] Fig. 10 illustrates a top view of a chip layout design for the pixel 105_1 shown in Fig. 9, according to one inventive embodiment of the present disclosure. Fig. 11A shows a composite cross-sectional view along the line I--I of the pixel shown in Fig. 10, including additional elements on the right half of Fig. 10 between the lines II--II and III--III, illustrating a layer-by-layer view of the pixel fabrication, and Figs. 12A through 12L provide top views of each of the fabrication layers shown in Fig. 11A (the respective images of Figs. 12A through 12L are superimposed one on top of another to create the pixel chip layout design shown in Fig. 10). In one exemplary implementation, the pixel design illustrated in Figs. 10-12 may be realized using a standard 4-metal, 2-poly, 0.35 micrometer CMOS process to provide a geometrically square pixel having a dimension "e" as shown in Fig. 10 of approximately 9 micrometers, and a dimension "f" corresponding to the ISFET sensitive area of approximately 7 micrometers.

[00144] In the top view of Fig. 10, the ISFET 150 (labeled as Q1 in Fig. 10) generally occupies the right center portion of the pixel illustration, and the respective locations of the gate, source and drain of the ISFET are indicated as $Q1_G$, $Q1_S$ and $Q1_D$. The MOSFETs Q2 and Q3 generally occupy the left center portion of the pixel illustration; the gate and source of the MOSFET Q2 are indicated as $Q2_G$ and $Q2_S$, and the gate and source of the MOSFET

Q3 are indicated as $Q3_G$ and $Q3_S$. In one aspect of the layout shown in Fig. 10, the MOSFETs Q2 and Q3 share a drain, indicated as $Q2/3_D$. In another aspect, it may be observed generally from the top view of Fig. 10 that the ISFET is formed such that its channel lies along a first axis of the pixel (e.g., parallel to the line I--I), while the MOSFETs Q2 and Q3 are formed such that their channels lie along a second axis perpendicular to the first axis. Fig. 10 also shows the four lines required to operate the pixel, namely, the line 112_1 coupled to the source of Q3, the line 114_1 coupled to the source of Q2, the line 116_1 coupled to the drain of the ISFET, and the row select line 118_1 coupled to the gates of Q2 and Q3. With reference to Fig. 9, it may be appreciated that all pixels in a given column share the lines 112, 114 and 116 (e.g., running vertically across the pixel in Fig. 10), and that all pixels in a given row share the line 118 (e.g., running horizontally across the pixel in Fig. 10); thus, based on the pixel design of Fig. 9 and the layout shown in Fig. 10, only four metal lines need to traverse each pixel.

[00145] With reference now to the cross-sectional view of Fig. 11A, highly doped p-type regions 156 and 158 (lying along the line I--I in Fig. 10) in n-well 154 constitute the source (S) and drain (D) of the ISFET, between which lies a region 160 of the n-well in which the ISFETs p-channel is formed below the ISFETs polysilicon gate 164 and a gate oxide 165. According to one aspect of the inventive embodiment shown in Figs. 10 and 11, all of the FET components of the pixel 105_1 are fabricated as p-channel FETs in the single n-type well 154 formed in a p-type semiconductor substrate 152. This is possible because, unlike the design of Milgrew et al., 1) there is no requirement for a transmission gate in the pixel; and 2) the ISFETs source is not tied to the n-well's body connection. More specifically, highly doped n-type regions 162 provide a body connection (B) to the n-well 154 and, as shown in Fig. 10, the body connection B is coupled to a metal conductor 322 around the perimeter of the pixel 105_1. However, the body connection is not directly electrically coupled to the source region 156 of the ISFET (i.e., there is no electrical conductor coupling the body connection and source such that they are forced to be at the same electric potential during operation), nor is the body connection directly electrically coupled to the gate, source or drain of any component in the pixel. Thus, the other p-channel FET components of the pixel, namely Q2 and Q3, may be fabricated in the same n-well 154.

[00146] In the composite cross-sectional view of Fig. 11A, a highly doped p-type region 159 is also visible (lying along the line I--I in Fig. 10), corresponding to the shared drain

(D) of the MOSFETs Q2 and Q3. For purposes of illustration, a polysilicon gate 166 of the MOSFET Q3 also is visible in Fig. 11A, although this gate does not lie along the line I--I in Fig. 10, but rather "behind the plane" of the cross-section along the line I--I. However, for simplicity, the respective sources of the MOSFETs Q2 and Q3 shown in Fig. 10, as well as the gate of Q2, are not visible in Fig. 11A, as they lie along the same axis (i.e., perpendicular to the plane of the figure) as the shared drain (if shown in Fig. 11A, these elements would unduly complicate the composite cross-sectional view of Fig. 11A).

[00147] Above the substrate, gate oxide, and polysilicon layers shown in Fig. 11A, a number of additional layers are provided to establish electrical connections to the various pixel components, including alternating metal layers and oxide layers through which conductive vias are formed. Pursuant to the 4-Metal CMOS process, these layers are labeled in Fig. 11A as "Contact," "Metal1," "Via1," "Metal2," "Via2," "Metal3," "Via3," and "Metal4." To facilitate an understanding particularly of the ISFET electrical connections, the composite cross-sectional view of Fig. 11A shows additional elements of the pixel fabrication on the right side of the top view of Fig. 10 between the lines II--II and III--III. With respect to the ISFET electrical connections, the topmost metal layer 304 corresponds to the ISFETs sensitive area 178, above which is disposed an analyte-sensitive passivation layer 172. The topmost metal layer 304, together with the ISFET polysilicon gate 164 and the intervening conductors 306, 308, 312, 316, 320, 326 and 338, form the ISFETs "floating gate" structure 170, in a manner similar to that discussed above in connection with a conventional ISFET design shown in Fig. 1. An electrical connection to the ISFETs drain is provided by the conductors 340, 328, 318, 314 and 310 coupled to the line 116_1. The ISFETs source is coupled to the shared drain of the MOSFETs Q2 and Q3 via the conductors 334 and 336 and the conductor 324 (which lies along the line I—I in Fig. 10). The body connections 162 to the n-well 154 are electrically coupled to a metal conductor 322 around the perimeter of the pixel on the "Metal1" layer via the conductors 330 and 332.

[00148] As indicated above, Figs. 12A through 12L provide top views of each of the fabrication layers shown in Fig. 11A (the respective images of Figs. 12A through 12L are superimposed one on top of another to create the pixel chip layout design shown in Fig. 10). In Fig. 12, the correspondence between the lettered top views of respective layers and the cross-sectional view of Fig. 11A is as follows: A) n-type well 154; B) Implant; C)

Diffusion; D) polysilicon gates 164 (ISFET) and 166 (MOSFETs Q2 and Q3); E) contacts; F) Metal1; G) Via1; H) Metal2; I) Via2; J) Metal3; K) Via3; L) Metal4 (top electrode contacting ISFET gate). The various reference numerals indicated in Figs. 12A through 12L correspond to the identical features that are present in the composite cross-sectional view of Fig. 11A.

[00149] Thus, the pixel chip layout design shown in Figs. 10, 11, and 12A through 12L illustrates that, according to one embodiment, FET devices of a same type may be employed for all components of the pixel, and that all components may be implemented in a single well. This dramatically reduces the area required for the pixel, thereby facilitating increased pixel density in a given area.

[00150] In one exemplary implementation, the gate oxide 165 for the ISFET may be fabricated to have a thickness on the order of approximately 75 Angstroms, giving rise to a gate oxide capacitance per unit area C_{ox} of 4.5 fF/μm^2. Additionally, the polysilicon gate 164 may be fabricated with dimensions corresponding to a channel width W of 1.2 μm and a channel length L of from 0.35 to 0.6 μm (i.e., W/L ranging from approximately 2 to 3.5), and the doping of the region 160 may be selected such that the carrier mobility for the p-channel is 190 cm^2/V·s (i.e., 1.9E10 μm^2/V·s). From Eq. (2) above, this results in an ISFET transconductance parameter β on the order of approximately 170 to 300 μA/V^2. In other aspects of this exemplary implementation, the analog supply voltage VDDA is 3.3 Volts, and VB1 and VB2 are biased so as to provide a constant ISFET drain current I_{Dj} on the order of 5 μA (in some implementations, VB1 and VB2 may be adjusted to provide drain currents from approximately 1 μA to 20 μA). Additionally, the MOSFET Q6 (see bias/readout circuitry 110j in Fig. 9) is sized to have a channel width to length ratio (e.g., W/L of approximately 50) such that the voltage across Q6, given I_{Dj} of 5 μA, is 800 mV (i.e., V_{DSj} = 800 mV). From Eq. (3), based on these exemplary parameters, this provides for pixel output voltages V_{Sj} over a range of approximately 0.5 to 2.5 Volts for ISFET threshold voltage changes over a range of approximately 0 to 2 Volts.

[00151] With respect to the analyte-sensitive passivation layer 172 shown in Fig. 11A, in exemplary CMOS implementations the passivation layer may be significantly sensitive to hydrogen ion concentration and may include silicon nitride (Si_3N_4) and/or silicon oxynitride (Si_2N_2O). In conventional CMOS processes, a passivation layer may be formed by one or

more successive depositions of these materials, and is employed generally to treat or coat devices so as to protect against contamination and increase electrical stability. The material properties of silicon nitride and silicon oxynitride are such that a passivation layer comprising these materials provides scratch protection and serves as a significant barrier to the diffusion of water and sodium, which can cause device metallization to corrode and/or device operation to become unstable. A passivation layer including silicon nitride and/or silicon oxynitride also provides ion-sensitivity in ISFET devices, in that the passivation layer contains surface groups that may donate or accept protons from an analyte solution with which they are in contact, thereby altering the surface potential and the device threshold voltage V_{TH}, as discussed above in connection with Fig. 1.

[00152] For CMOS processes involving aluminum as the metal (which has a melting point of approximately 650 degrees Celsius), a silicon nitride and/or silicon oxynitride passivation layer generally is formed via plasma-enhanced chemical vapor deposition (PECVD), in which a glow discharge at 250-350 degrees Celsius ionizes the constituent gases that form silicon nitride or silicon oxynitride, creating active species that react at the wafer surface to form a laminate of the respective materials. In one exemplary process, a passivation layer having a thickness on the order of approximately 1.0 to 1.5 μm may be formed by an initial deposition of a thin layer of silicon oxynitride (on the order of 0.2 to 0.4 μm) followed by a slighting thicker deposition of silicon oxynitride (on the order of 0.5 μm) and a final deposition of silicon nitride (on the order of 0.5 μm). Because of the low deposition temperature involved in the PECVD process, the aluminum metallization is not adversely affected.

[00153] However, Applicants have recognized and appreciated that while a low-temperature PECVD process provides adequate passivation for conventional CMOS devices, the low-temperature process results in a generally low-density and somewhat porous passivation layer, which in some cases may adversely affect ISFET threshold voltage stability. In particular, during ISFET device operation, a low-density porous passivation layer over time may absorb and become saturated with ions from the solution, which may in turn cause an undesirable time-varying drift in the ISFETs threshold voltage V_{TH}, making accurate measurements challenging.

[00154] In view of the foregoing, in one embodiment a CMOS process that uses tungsten metal instead of aluminum may be employed to fabricate ISFET arrays according to the present disclosure. The high melting temperature of Tungsten (above 3400 degrees Celsius) permits the use of a higher temperature low pressure chemical vapor deposition (LPCVD) process (e.g., approximately 700 to 800 degrees Celsius) for a silicon nitride or silicon oxynitride passivation layer. The LPCVD process typically results in significantly more dense and less porous films for the passivation layer, thereby mitigating the potentially adverse effects of ion absorption from the analyte solution leading to ISFET threshold voltage drift.

[00155] In yet another embodiment in which an aluminum-based CMOS process is employed to fabricate ISFET arrays according to the present disclosure, the passivation layer 172 shown in Fig. 11A may comprise additional depositions and/or materials beyond those typically employed in a conventional CMOS process. For example, the passivation layer 172 may include initial low-temperature plasma-assisted depositions (PECVD) of silicon nitride and/or silicon oxynitride as discussed above; for purposes of the present discussion, these conventional depositions are illustrated in Fig. 11A as a first portion 172A of the passivation layer 172. In one embodiment, following the first portion 172A, one or more additional passivation materials are disposed to form at least a second portion 172B to increase density and reduce porosity of (and absorption by) the overall passivation layer 172. While one additional portion 172B is shown primarily for purposes of illustration in Fig. 11A, it should be appreciated that the disclosure is not limited in this respect, as the overall passivation layer 172 may comprise two or more constituent portions, in which each portion may comprise one or more layers/depositions of same or different materials, and respective portions may be configured similarly or differently.

[00156] Examples of materials suitable for the second portion 172B (or other additional portions) of the passivation layer 172 for particular sensitivity to hydrogen ions include, but are not limited to, silicon nitride, silicon oxynitride, aluminum oxide (Al_2O_3), tantalum oxide (Ta_3O_5), tin oxide (SnO_2) and silicon dioxide (SiO_2). In one aspect, the second portion 172B (or other additional portions) may be deposited via a variety of relatively low-temperature processes including, but not limited to, RF sputtering, DC magnetron sputtering, thermal or e-beam evaporation, and ion-assisted depositions. In another aspect, a pre-sputtering etch process may be employed, prior to deposition of the second portion

172B, to remove any native oxide residing on the first portion 172A (alternatively, a reducing environment, such as an elevated temperature hydrogen environment, may be employed to remove native oxide residing on the first portion 172A). In yet another aspect, a thickness of the second portion 172B may be on the order of approximately 0.04 μm to 0.06 μm (400 to 600 Angstroms) and a thickness of the first portion may be on the order of 1.0 to 1.5 μm, as discussed above. In some exemplary implementations, the first portion 172A may include multiple layers of silicon oxynitride and silicon nitride having a combined thickness of 1.0 to 1.5 μm, and the second portion 172B may include a single layer of either aluminum oxide or tantalum oxide having a thickness of approximately 400 to 600 Angstroms. Again, it should be appreciated that the foregoing exemplary thicknesses are provided primarily for purposes of illustration, and that the disclosure is not limited in these respects.

[00157] Thus it is to be understood that the chemFET arrays described herein may be used to detect various analytes and, by doing so, may monitor a variety of reactions and/or interactions. It is also to be understood that the emphasis on hydrogen ion detection (in the form of a pH change) is for the sake of convenience and brevity and that other analytes (including other ions) can be substituted for hydrogen in these descriptions.

[00158] The chemFETs, including ISFETs, described herein are capable of detecting any analyte that is itself capable of inducing a change in electric field. The analyte need not be charged in order to be detected by the sensor. For example, depending on the embodiment, the analyte may be positively charged (i.e., a cation), negatively charged (i.e., an anion), zwitterionic (i.e., capable of having two equal and opposite charges but overall neutral), and polar yet neutral. This list is not intended as exhaustive as other analyte classes as well as species within each class will be readily contemplated by those of ordinary skill in the art based on the disclosure provided herein.

[00159] In the broadest sense of the invention, passivation layer may or may not be coated and the analyte may or may not interact with the passivation layer. As an example, the passivation layer may be comprised of silicon nitride and the analyte may be something other than hydrogen ions. As a specific example, the passivation layer may be comprised of silicon nitride and the analyte may be inorganic pyrophosphate (PPi). In these instances,

PPi is detected directly (i.e., in the absence of PPi receptors attached to the passivation layer either directly or indirectly).

[00160] If the analyte being detected is hydrogen (or alternatively hydroxide), then it is preferable to use weak buffers so that changes in either ionic species can be detected at the passivation layer. If the analyte being detected is something other than hydrogen (or hydroxide) but there is some possibility of a pH change in the solution during the reaction or detection step, then it is preferable to use a strong buffer so that changes in pH do not interfere with the detection of the analyte. A buffer is an ionic molecule that resists changes in pH. Buffers are able to neutralize acids or bases added to or generated in a solution, resulting in no effective pH change in the solution. It is to be understood that any buffer is suitable provided it has a pKa in the desired range. A suitable buffer is one that functions in about the pH range of 6 to 9, and more preferably 6.5 to 8.5. The strength of a buffer is a relative term since it depends on the nature, strength and concentration of the acid or base added to or generated in the solution of interest. A weak buffer is a buffer that allows detection (and therefore is not able to otherwise control) pH changes of about at least +/- 0.005, 0.01, 0.015, 0.02, 0.03, 0.04, 0.05, 0.10, 0.15, 0.20, 0.25, 0.30, 0.35, 0.45, 0.50, or more. In some embodiments, the pH change is on the order of about 0.005 (e.g., per nucleotide incorporation) and is preferably an increase in pH. A strong buffer is a buffer that controls pH changes of about at least +/- 0.005, 0.01, 0.015, 0.02, 0.03, 0.04, 0.05, 0.10, 0.15, 0.20, 0.25, 0.30, 0.35, 0.45, 0.50, or more. Buffer strength can be varied by varying the concentration of the buffer species itself. Thus low concentration buffers can be low strength buffers. Examples include those having less than 1 mM (e.g., 50-100 μM) buffer species. A non-limiting example of a weak buffer suitable for the sequencing reactions described herein wherein pH change is the readout is 0.1 mM Tris or Tricine. Examples of suitable weak buffers are provided in the Examples and are also known in the art. Higher concentration buffers can be stronger buffers. Examples include those having 1-25 mM buffer species. A non-limiting example of a strong buffer suitable for the sequencing reactions described herein wherein PPi is read directly is 1, 5 or 25 mM (or more) Tris or Tricine. One of ordinary skill in the art will be able to determine the optimal buffer for use in the reactions and detection methods encompassed by the invention.

[00161] In some embodiments, the passivation layer and/or the molecules coated thereon dictate the analyte specificity of the array readout.

[00162] Detection of hydrogen ions (in the form of pH) can be carried out using a passivation layer made of silicon nitride (Si_3N_4), silicon oxynitride (Si_2N_2O), silicon oxide (SiO_2), aluminum oxide (Al_2O_3), tantalum pentoxide (Ta_2O_5), tin oxide or stannic oxide (SnO_2), and the like.

[00163] The passivation layer can also detect other ion species directly including but not limited to calcium, potassium, sodium, iodide, magnesium, chloride, lithium, lead, silver, cadmium, nitrate, phosphate, dihydrogen phosphate, and the like.

[00164] In some embodiments, the passivation layer is coated with a receptor for the analyte of interest. The receptor binds selectively to the analyte of interest. As used herein, a receptor that binds selectively to an analyte is a molecule that binds preferentially to that analyte (i.e., its binding affinity for that analyte is greater than its binding affinity for any other analyte). Its binding affinity for the analyte of interest may be 2-fold, 3-fold, 4-fold, 5-fold, 6-fold, 7-fold, 8-fold, 9-fold, 10-fold, 15-fold, 20-fold, 25-fold, 30-fold, 40-fold, 50-fold, 100-fold or more than its binding affinity for any other analyte. In addition to its relative binding affinity, the receptor must also have an absolute binding affinity that is sufficiently high to efficiently bind the analyte of interest (i.e., it must have a sufficient sensitivity). Receptors having binding affinities in the picomolar to micromolar range are suitable. Preferably such interaction are reversible.

[00165] The receptor may be of any nature (e.g., chemical, nucleic acid, peptide, lipid, combinations thereof and the like). The analyte too may be of any nature provided there exists a receptor that binds to it selectively and in some instances specifically. It is to be understood however that the invention further contemplates detection of analytes in the absence of a receptor. An example of this is the detection of PPi and Pi by the passivation layer in the absence of PPi or Pi receptors.

[00166] In one aspect, the invention contemplates receptors that are ionophores. As used herein, an ionophore is a molecule that binds selectively to an ionic species, whether anion or cation. In the context of the invention, the ionophore is the receptor and the ion to which it binds is the analyte. Ionophores of the invention include art-recognized carrier ionophores (i.e., small lipid-soluble molecules that bind to a particular ion) derived from microorganisms. Various ionophores are commercially available from sources such as Calbiochem.

[00167] Detection of some ions can be accomplished through using the passivation layer itself or through the use of receptors coated onto the passivation layer. For example, potassium can be detected selectively using the polysiloxane, valinomycin, or salinomycin; sodium can be detected selectively using monensin, nystatin, or SQI-Pr; calcium can be detected selectively using ionomycin, calcimycine (A23187), or CA 1001 (ETH 1001).

[00168] Receptors able to bind more than one ion can also be used in some instances. For example, beauvericin can be used to detect calcium and/or barium ions, nigericin can be used to detect potassium, hydrogen and/or lead ions, and gramicidin can be used to detect hydrogen, sodium and/or potassium ions. One of ordinary skill in the art will recognize that these compounds can be used in applications in which single ion specificity is not required or in which it is unlikely (or impossible) that other ions which the compounds bind will be present or generated.

[00169] In other embodiments, including but not limited to nucleic acid sequencing applications, receptors that bind selectively to inorganic pyrophosphate (PPi) can be used. Examples of PPi receptors include those compounds shown in Fig. 11B (compounds 1-10). Compound 1 is described in Angew Chem Int Ed 2004 43:4777-4780 and US 2005/0119497 A1 and is referred to as p-naphthyl-bis[(bis(2-pyridylmethyl)amino)methyl]phenol. Compound 2 is described in J Am Chem Soc 2003 125:7752-7753 and US 2005/0119497 A1 and is referred to as p-(p-nitrophenylazo)-bis[(bis(2-pyridylmethyl-1)amino)methyl]phenol (or its dinuclear Zn complex). Compound 3 is described in Sensors and Actuators B 1995 29:324-327. Compound 4 is described in Angew Chem Int Ed 2002 41(20):3811-3814. Compound 5 is described in WO 2007/002204 and is referred to therein as bis-Zn^{2+} -dipicolylamine (Zn^{2+}-DPA). Synthesis schemes for compounds 1 and 2 are shown provided in US 2005/0119497 A1. An exemplary synthesis for compound 4 is shown in Fig. 11C. Attachment of compound 10 to a metal oxide surface is shown in Fig. 11E.

[00170] As another example, receptors for neurotoxins are described in Simonian Electroanalysis 2004, 16: 1896-1906.

[00171] Receptors may be attached to the passivation layer covalently or non-covalently. Covalent attachment of a receptor to the passivation layer may be direct or indirect (e.g., through a linker). Fig. 11D illustrates the use of silanol chemistry to covalently bind

receptors to the passivation layer. Receptors may be immobilized on the passivation layer using for example aliphatic primary amines (bottom left panel) or aryl isothiocyanates (bottom right panel). In these and other embodiments, the passivation layer which itself may be comprised of silicon nitride, aluminum oxide, silicon oxide, tantalum pentoxide, or the like, is bonded to a silanation layer via its reactive surface groups. For greater detail on silanol chemistry for covalent attachment to the FET surface, reference can be made to at least the following publications: for silicon nitride, see Sensors and Actuators B 1995 29:324-327, Jpn J Appl Phys 1999 38:3912-3917 and Langmuir 2005 21:395-402; for silicon oxide, see Protein Sci 1995 4:2532-2544 and Am Biotechnol Lab 2002 20(7):16-18; and for aluminum oxide, see Colloids and Surfaces 1992 63:1-9, Sensors and Accuators B 2003 89:40-47, and Bioconjugate Chem 1997 8:424-433. The receptor is then conjugated to the silanation layer reactive groups. This latter binding can occur directly or indirectly through the use of a bifunctional linker, as illustrated in Fig. 11D. A bifunctional linker is a compound having at least two reactive groups to which two entities may be bound. In some instances, the reactive groups are located at opposite ends of the linker. In some embodiments, the bifunctional linker is a universal bifunctional linker such as that shown in Fig. 11D. A universal linker is a linker that can be used to link a variety of entities. It should be understood that the chemistries shown in Fig. 11D are meant to be illustrative and not limiting.

[00172] The bifunctional linker may be a homo-bifunctional linker or a hetero-bifunctional linker, depending upon the nature of the molecules to be conjugated. Homo-bifunctional linkers have two identical reactive groups. Hetero-bifunctional linkers are have two different reactive groups. Various types of commercially available linkers are reactive with one or more of the following groups: primary amines, secondary amines, sulphydryls, carboxyls, carbonyls and carbohydrates. Examples of amine-specific linkers are bis(sulfosuccinimidyl) suberate, bis[2-(succinimidooxycarbonyloxy)ethyl] sulfone, disuccinimidyl suberate, disuccinimidyl tartarate, dimethyl adipimate·2 HCl, dimethyl pimelimidate·2 HCl, dimethyl suberimidate·2 HCl, and ethylene glycolbis-[succinimidyl-[succinate]]. Linkers reactive with sulfhydryl groups include bismaleimidohexane, 1,4-di-[3'-(2'-pyridyldithio)-propionamido)] butane, 1-[p-azidosalicylamido]-4-[iodoacetamido] butane, and N-[4-(p-azidosalicylamido) butyl]-3'-[2'-pyridyldithio] propionamide. Linkers preferentially reactive with carbohydrates include azidobenzoyl

hydrazine. Linkers preferentially reactive with carboxyl groups include 4-[p-azidosalicylamido] butylamine.

[00173] Heterobifunctional linkers that react with amines and sulfhydryls include N-succinimidyl-3-[2-pyridyldithio] propionate, succinimidyl [4-iodoacetyl]aminobenzoate, succinimidyl 4-[N-maleimidomethyl] cyclohexane-1- carboxylate, m-maleimidobenzoyl-N-hydroxysuccinimide ester, sulfosuccinimidyl 6-[3-[2-pyridyldithio]propionamido]hexanoate, and sulfosuccinimidyl 4-[N-maleimidomethyl] cyclohexane-1-carboxylate. Heterobifunctional linkers that react with carboxyl and amine groups include 1-ethyl-3-[3-dimethylaminopropyl]-carbodiimide hydrochloride. Heterobifunctional linkers that react with carbohydrates and sulfhydryls include 4-[N-maleimidomethyl]-cyclohexane-1-carboxylhydrazide·2 HCl, 4-(4-N-maleimidophenyl)-butyric acid hydrazide·2 HCl, and 3-[2-pyridyldithio] propionyl hydrazide.

[00174] Alternatively, receptors may be non-covalently coated onto the passivation layer. Non-covalent deposition of the receptor to the passivation layer may involve the use of a polymer matrix. The polymer may be naturally occurring or non-naturally occurring and may be of any type including but not limited to nucleic acid (e.g., DNA, RNA, PNA, LNA, and the like, or mimics, derivatives, or combinations thereof), amino acid (e.g., peptides, proteins (native or denatured), and the like, or mimics, derivatives, or combinations thereof, lipids, polysaccharides, and functionalized block copolymers. The receptor may be adsorbed onto and/or entrapped within the polymer matrix.

[00175] Alternatively, the receptor may be covalently conjugated or crosslinked to the polymer (e.g., it may be "grafted" onto a functionalized polymer).

[00176] An example of a suitable peptide polymer is poly-lysine (e.g., poly-L-lysine). Examples of other polymers include block copolymers that comprise polyethylene glycol (PEG), polyamides, polycarbonates, polyalkylenes, polyalkylene glycols, polyalkylene oxides, polyalkylene terepthalates, polyvinyl alcohols, polyvinyl ethers, polyvinyl esters, polyvinyl halides, polyvinylpyrrolidone, polyglycolides, polysiloxanes, polyurethanes, alkyl cellulose, hydroxyalkyl celluloses, cellulose ethers, cellulose esters, nitrocelluloses, polymers of acrylic and methacrylic esters, methyl cellulose, ethyl cellulose, hydroxypropyl cellulose, hydroxypropyl methyl cellulose, hydroxybutyl methyl cellulose, cellulose acetate,

cellulose propionate, cellulose acetate butyrate, cellulose acetate phthalate, carboxylethyl cellulose, cellulose triacetate, cellulose sulphate sodium salt, poly(methyl methacrylate), poly(ethyl methacrylate), poly(butylmethacrylate), poly(isobutyl methacrylate), poly(hexylmethacrylate), poly(isodecyl methacrylate), poly(lauryl methacrylate), poly(phenyl methacrylate), poly(methyl acrylate), poly(isopropyl acrylate), poly(isobutyl acrylate), poly(octadecyl acrylate), polyethylene, polypropylene, poly(ethylene glycol), poly(ethylene oxide), poly(ethylene terephthalate), poly(vinyl alcohols), polyvinyl acetate, polyvinyl chloride, polystyrene, polyhyaluronic acids, casein, gelatin, glutin, polyanhydrides, polyacrylic acid, alginate, chitosan, poly(methyl methacrylates), poly(ethyl methacrylates), poly(butylmethacrylate), poly(isobutyl methacrylate), poly(hexylmethacrylate), poly(isodecyl methacrylate), poly(lauryl methacrylate), poly(phenyl methacrylate), poly(methyl acrylate), poly(isopropyl acrylate), poly(isobutyl acrylate), and poly(octadecyl acrylate), poly(lactide-glycolide), copolyoxalates, polycaprolactones, polyesteramides, polyorthoesters, polyhydroxybutyric acid, polyanhydrides, poly (styrene-b-isobutylene-b-styrene) (SIBS) block copolymer, ethylene vinyl acetate, poly(meth)acrylic acid, polymers of lactic acid and glycolic acid, polyanhydrides, poly(ortho)esters, polyurethanes, poly(butic acid), poly(valeric acid), and poly(lactide-cocaprolactone), and natural polymers such as alginate and other polysaccharides including dextran and cellulose, collagen, albumin and other hydrophilic proteins, zein and other prolamines and hydrophobic proteins, copolymers and mixtures thereof, and chemical derivatives thereof including substitutions and/or additions of chemical groups, for example, alkyl, alkylene, hydroxylations, oxidations, and other modifications routinely made by those skilled in the art.

[00177] Another issue that relates to ISFET threshold voltage stability and/or predictability involves trapped charge that may accumulate on metal layers of CMOS-fabricated devices as a result of various processing activities during or following array fabrication (e.g., back-end-of-line processing such as plasma metal etching, wafer cleaning, dicing, packaging, handling, etc.). In particular, with reference to Fig. 11A, trapped charge may in some instances accumulate on one or more of the various conductors 304, 306, 308, 312, 316, 320, 326, 338, and 164 constituting the ISFETs floating gate structure 170. This phenomenon also is referred to in the relevant literature as the "antenna effect."

[00178] One opportunity for trapped charge to accumulate includes plasma etching of the topmost metal layer 304. Applicants have recognized and appreciated that other opportunities for charge to accumulate on one or more conductors of the floating gate structure includes wafer dicing, during which the abrasive process of a dicing saw cutting through a wafer generates static electricity, and/or various post-processing wafer handling/packaging steps, where automated machinery that handles/transports wafers may be sources of electrostatic discharge (ESD) to conductors of the floating gate structure. If there is no connection to the silicon substrate (or other semi-conductor substrate) to provide an electrical path to bleed off such charge accumulation, charge may build up to the point of causing undesirable changes or damage to the gate oxide 165 (e.g., charge injection into the oxide, or low-level oxide breakdown to the underlying substrate). Trapped charge in the gate oxide or at the gate oxide-semiconductor interface in turn can cause undesirable and/or unpredictable variations in ISFET operation and performance.

[00179] In view of the foregoing, other inventive embodiments of the present disclosure are directed to methods and apparatus for improving ISFET performance by reducing trapped charge or mitigating the antenna effect. In one embodiment, trapped charge may be reduced after a sensor array has been fabricated, while in other embodiments the fabrication process itself may be modified to reduce trapped charge that could be induced by some conventional process steps. In yet other embodiments, both "during fabrication" and "post fabrication" techniques may be employed in combination to reduce trapped charge and thereby improve ISFET performance.

[00180] With respect to alterations to the fabrication process itself to reduce trapped charge, in one embodiment the thickness of the gate oxide 165 shown in Fig. 11A may be particularly selected so as to facilitate bleeding of accumulated charge to the substrate; in particular, a thinner gate oxide may allow a sufficient amount of built-up charge to pass through the gate oxide to the substrate below without becoming trapped. In another embodiment based on this concept, a pixel may be designed to include an additional "sacrificial" device, i.e., another transistor having a thinner gate oxide than the gate oxide 165 of the ISFET. The floating gate structure of the ISFET may then be coupled to the gate of the sacrificial device such that it serves as a "charge bleed-off transistor." Of course, it should be appreciated that some trade-offs for including such a sacrificial device include an increase in pixel size and complexity.

[00181] In another embodiment, the topmost metal layer 304 of the ISFETs floating gate structure 170 shown in Fig. 11A may be capped with a dielectric prior to plasma etching to mitigate trapped charge. As discussed above, charge accumulated on the floating gate structure may in some cases be coupled from the plasma being used for metal etching. Typically, a photoresist is applied over the metal to be etched and then patterned based on the desired geometry for the underlying metal. In one exemplary implementation, a capping dielectric layer (e.g., an oxide) may be deposited over the metal to be etched, prior to the application of the photoresist, to provide an additional barrier on the metal surface against charge from the plasma etching process. In one aspect, the capping dielectric layer may remain behind and form a portion of the passivation layer 172.

[00182] In yet another embodiment, the metal etch process for the topmost metal layer 304 may be modified to include wet chemistry or ion-beam milling rather than plasma etching. For example, the metal layer 304 could be etched using an aqueous chemistry selective to the underlying dielectric (e.g., see http://www.transene.com/aluminum.html, hereby incorporated herein by reference). Another alternative approach employs ion-milling rather than plasma etching for the metal layer 304. Ion-milling is commonly used to etch materials that cannot be readily removed using conventional plasma or wet chemistries. The ion-milling process does not employ an oscillating electric field as does a plasma, so that charge build-up does not occur in the metal layer(s). Yet another metal etch alternative involves optimizing the plasma conditions so as to reduce the etch rate (i.e. less power density).

[00183] In yet another embodiment, architecture changes may be made to the metal layer to facilitate complete electrical isolation during definition of the floating gate. In one aspect, designing the metal stack-up so that the large area ISFET floating gate is not connected to anything during its final definition may require a subsequent metal layer serving as a "jumper" to realize the electrical connection to the floating gate of the transistor. This "jumper" connection scheme prevents charge flow from the large floating gate to the transistor. This method may be implemented as follows (M = metal layer): i) M1 contacting Poly gate electrode; ii) M2 contacting M1; iii) M3 defines floating gate and separately connects to M2 with isolated island; iv) M4 jumper, having very small area being etched over the isolated islands and connections to floating gate M3, connects the M3 floating gate to the M1/M2/M3 stack connected to the Poly gate immediately over the

transistor active area; and v) M3 to M4 interlayer dielectric is removed only over the floating gate so as to expose the bare M3 floating gate. In the method outlined immediately above, step v) need not be done, as the ISFET architecture according to some embodiments discussed above leaves the M4 passivation in place over the M4 floating gate. In one aspect, removal may nonetheless improve ISFET performance in other ways (i.e. sensitivity). In any case, the final chemically-sensitive passivation layer may be a thin sputter-deposited ion-sensitive metal-oxide layer. It should be appreciated that the over-layer jumpered architecture discussed above may be implemented in the standard CMOS fabrication flow to allow any of the first three metal layers to be used as the floating gates (i.e. M1, M2 or M3).

[00184] With respect to post-fabrication processes to reduce trapped charge, in one embodiment a "forming gas anneal" may be employed as a post-fabrication process to mitigate potentially adverse effects of trapped charge. In a forming gas anneal, CMOS-fabricated ISFET devices are heated in a hydrogen and nitrogen gas mixture. The hydrogen gas in the mixture diffuses into the gate oxide 165 and neutralizes certain forms of trapped charges. In one aspect, the forming gas anneal need not necessarily remove all gate oxide damage that may result from trapped charges; rather, in some cases, a partial neutralization of some trapped charge is sufficient to significantly improve ISFET performance. In exemplary annealing processes according to the present disclosure, ISFETs may be heated for approximately 30 to 60 minutes at approximately 400 to 425 degrees Celsius in a hydrogen/nitrogen mixture that includes 10% to 15% hydrogen. In one particular implementation, annealing at 425 degrees Celsius at 30 minutes in a hydrogen/nitrogen mixture that includes 10% hydrogen is observed to be particularly effective at improving ISFET performance. For aluminum CMOS processes, the temperature of the anneal should be kept at or below 450 degrees Celsius to avoid damaging the aluminum metallurgy. In another aspect of an annealing process according to the present disclosure, the forming gas anneal is performed after wafers of fabricated ISFET arrays are diced, so as to ensure that damage due to trapped charge induced by the dicing process itself, and/or other pre-dicing processing steps (e.g., plasma etching of metals) may be effectively ameliorated.

[00185] In yet other processes for mitigating potentially adverse effects of trapped charge according to embodiments of the present disclosure, a variety of "electrostatic discharge (ESD)-sensitive protocols" may be adopted during any of a variety of wafer post-fabrication

handling/packaging steps. For example, in one exemplary process, anti-static dicing tape may be employed to hold wafer substrates in place (e.g., during the dicing process). Also, although high-resistivity (e.g., 10 MΩ) deionized water conventionally is employed in connection with cooling of dicing saws, according to one embodiment of the present disclosure less resistive/more conductive water may be employed for this purpose to facilitate charge conduction via the water; for example, deionized water may be treated with carbon dioxide to lower resistivity and improve conduction of charge arising from the dicing process. Furthermore, conductive and grounded die-ejection tools may be used during various wafer dicing/handling/packaging steps, again to provide effective conduction paths for charge generated during any of these steps, and thereby reduce opportunities for charge to accumulate on one or more conductors of the floating gate structure of respective ISFETs of an array.

[00186] In yet another embodiment involving a post-fabrication process to reduce trapped charge, the gate oxide region of an ISFET may be irradiated with UV radiation. With reference again to Fig. 11A, in one exemplary implementation based on this embodiment, an optional hole or window 302 is included during fabrication of an ISFET array in the top metal layer 304 of each pixel of the array, proximate to the ISFET floating gate structure. This window is intended to allow UV radiation, when generated, to enter the ISFETs gate region; in particular, the various layers of the pixel 105_{i}, as shown in Figs. 11 and 12 A-L, are configured such that UV radiation entering the window 302 may impinge in an essentially unobstructed manner upon the area proximate to the polysilicon gate 164 and the gate oxide 165.

[00187] To facilitate a UV irradiation process to reduce trapped charge, Applicants have recognized and appreciated that materials other than silicon nitride and silicon oxynitride generally need to be employed in the passivation layer 172 shown in Fig. 11A, as silicon nitride and silicon oxynitride significantly absorb UV radiation. In view of the foregoing, these materials need to be substituted with others that are appreciably transparent to UV radiation, examples of which include, but are not limited to, phososilicate glass (PSG) and boron-doped phososilicate glass (BPSG). PSG and BPSG, however, are not impervious to hydrogen and hydroxyl ions; accordingly, to be employed in a passivation layer of an ISFET designed for pH sensitivity, PSG and BPSG may be used together with an ion-impervious material that is also significantly transparent to UV radiation, such as aluminum

oxide (Al_2O_3), to form the passivation layer. For example, with reference again to Fig. 11A, PSG or BPSG may be employed as a substitute for silicon nitride or silicon oxynitride in the first portion 172A of the passivation layer 172, and a thin layer (e.g., 400 to 600 Angstroms) of aluminum oxide may be employed in the second portion 172B of the passivation layer 172 (e.g., the aluminum oxide may be deposited using a post-CMOS lift-off lithography process).

[00188] In another aspect of an embodiment involving UV irradiation, each ISFET of a sensor array must be appropriately biased during a UV irradiation process to facilitate reduction of trapped charge. In particular, high energy photons from the UV irradiation, impinging upon the bulk silicon region 160 in which the ISFET conducting channel is formed, create electron-hole pairs which facilitate neutralization of trapped charge in the gate oxide as current flows through the ISFETs conducting channel. To this end, an array controller, discussed further below in connection with Fig. 17, generates appropriate signals for biasing the ISFETs of the array during a UV irradiation process. In particular, with reference again to Fig. 9, each of the signals $\overline{\text{RowSel}_1}$ through $\overline{\text{RowSel}_n}$ is generated so as to enable/select (i.e., turn on) all rows of the sensor array at the same time and thereby couple all of the ISFETs of the array to respective controllable current sources 106_j in each column. With all pixels of each column simultaneously selected, the current from the current source 106_j of a given column is shared by all pixels of the column. The column amplifiers 107A and 107B are disabled by removing the bias voltage VB4, and at the same time the output of the amplifier 107B, connected to the drain of each ISFET in a given column, is grounded via a switch responsive to a control signal "UV." Also, the common body voltage V_{BODY} for all ISFETs of the array is coupled to electrical ground (i.e., V_{BODY} = 0 Volts) (as discussed above, during normal operation of the array, the body bias voltage V_{BODY} is coupled to the highest voltage potential available to the array, e.g., VDDA). In one exemplary procedure, the bias voltage VB1 for all of the controllable current sources 106_j is set such that each pixel's ISFET conducts approximately 1 μA of current. With the ISFET array thusly biased, the array then is irradiated with a sufficient dose of UV radiation (e.g., from an EPROM eraser generating approximately 20 milliWatts/cm^2 of radiation at a distance of approximately one inch from the array for approximately 1 hour). After irradiation, the array may be allowed to rest and stabilize over several hours before use for measurements of chemical properties such as ion concentration.

[00189] Fig. 13 illustrates a block diagram of an exemplary CMOS IC chip implementation of an ISFET sensor array 100 based on the column and pixel designs discussed above in connection with Figs. 9-12, according to one embodiment of the present disclosure. In one aspect of this embodiment, the array 100 includes 512 columns 102_1 through 102_{512} with corresponding column bias/readout circuitry 110_1 through 110_{512} (one for each column, as shown in Fig. 9), wherein each column includes 512 geometrically square pixels 105_1 through 105_{512}, each having a size of approximately 9 micrometers by 9 micrometers (i.e., the array is 512 columns by 512 rows). In another aspect, the entire array (including pixels together with associated row and column select circuitry and column bias/readout circuitry) may be fabricated on a semiconductor die as an application specific integrated circuit (ASIC) having dimensions of approximately 7 millimeters by 7 millimeters. While an array of 512 by 512 pixels is shown in the embodiment of Fig. 13, it should be appreciated that arrays may be implemented with different numbers of rows and columns and different pixel sizes according to other embodiments, as discussed further below in connection with Figs. 19-23.

[00190] Also, as discussed above, it should be appreciated that arrays according to various embodiments of the present invention may be fabricated according to conventional CMOS fabrications techniques, as well as modified CMOS fabrication techniques (e.g., to facilitate realization of various functional aspects of the chemFET arrays discussed herein, such as additional deposition of passivation materials, process steps to mitigate trapped charge, etc.) and other semiconductor fabrication techniques beyond those conventionally employed in CMOS fabrication. Additionally, various lithography techniques may be employed as part of an array fabrication process. For example, in one exemplary implementation, a lithography technique may be employed in which appropriately designed blocks are "stitched" together by overlapping the edges of a step and repeat lithography exposures on a wafer substrate by approximately 0.2 micrometers. In a single exposure, the maximum die size typically is approximately 21 millimeters by 21 millimeters. By selectively exposing different blocks (sides, top & bottoms, core, etc.) very large chips can be defined on a wafer (up to a maximum, in the extreme, of one chip per wafer, commonly referred to as "wafer scale integration").

[00191] In one aspect of the array 100 shown in Fig. 13, the first and last two columns 102_1, 102_2, 102_{511} and 102_{512}, as well as the first two pixels 105_1 and 105_2 and the last two

pixels 105_{511} and 105_{512} of each of the columns 102_3 through 102_{510} (e.g., two rows and columns of pixels around a perimeter of the array) may be configured as "reference" or "dummy" pixels 103. With reference to Fig. 11A, for the dummy pixels of an array, the topmost metal layer 304 of each dummy pixel's ISFET (coupled ultimately to the ISFETs polysilicon gate 164) is tied to the same metal layer of other dummy pixels and is made accessible as a terminal of the chip, which in turn may be coupled to a reference voltage VREF. As discussed above in connection with Fig. 9, the reference voltage VREF also may be applied to the bias/readout circuitry of respective columns of the array. In some exemplary implementations discussed further below, preliminary test/evaluation data may be acquired from the array based on applying the reference voltage VREF and selecting and reading out dummy pixels, and/or reading out columns based on the direct application of VREF to respective column buffers (e.g., via the CAL signal), to facilitate offset determination (e.g., pixel-to-pixel and column-to-column variances) and array calibration.

[00192] In Fig. 13, various power supply and bias voltages required for array operation (as discussed above in connection with Fig. 9) are provided to the array via electrical connections (e.g., pins, metal pads) and labeled for simplicity in block 195 as "supply and bias connections." The array 100 of Fig. 13 also includes a row select shift register 192, two sets of column select shift registers $194_{1,2}$ and two output drivers 198_1 and 198_2 to provide two parallel output signals from the array, Vout1 and Vout2, representing sensor measurements. The various power supply and bias voltages, control signals for the row and column shift registers, and control signals for the column bias/readout circuitry shown in Fig. 13 are provided by an array controller, as discussed further below in connection with Fig. 17, which also reads the output signals Vout1 and Vout2 (and other optional status/diagnostic signals) from the array 100. In another aspect of the array embodiment shown in Fig. 13, configuring the array such that multiple regions (e.g., multiple columns) of the array may be read at the same time via multiple parallel array outputs (e.g., Vout1 and Vout2) facilitates increased data acquisition rates, as discussed further below in connection with Figs. 17 and 18. While Fig. 13 illustrates an array having two column select registers and parallel output signals Vout1 and Vout2 to acquire data simultaneously from two columns at a time, it should be appreciated that, in other embodiments, arrays according to the present disclosure may be configured to have only one measurement signal output, or more than two measurement signal outputs; in particular, as discussed further

below in connection with Figs. 19-23, more dense arrays according to other inventive embodiments may be configured to have four our more parallel measurement signal outputs and simultaneously enable different regions of the array to provide data via the four our more outputs.

[00193] Fig. 14 illustrates the row select shift register 192, Fig. 15 illustrates one of the column select shift registers 194_2 and Fig. 16 illustrates one of the output drivers 198_2 of the array 100 shown in Fig. 13, according to one exemplary implementation. As shown in Figs. 14 and 15, the row and column select shift registers are implemented as a series of D-type flip-flops coupled to a digital circuitry positive supply voltage VDDD and a digital supply ground VSSD. In the row and column shift registers, a data signal is applied to a D-input of first flip-flop in each series and a clock signal is applied simultaneously to a clock input of all of the flip-flops in the series. For each flip-flop, a "Q" output reproduces the state of the D-input upon a transition (e.g., falling edge) of the clock signal. With reference to Fig. 14, the row select shift register 192 includes 512 D-type flip-flops, in which a first flip-flop 193 receives a vertical data signal DV and all flip-flops receive a vertical clock signal CV. A "Q" output of the first flip-flop 193 provides the first row select signal $RowSel_1$ and is coupled to the D-input of the next flip-flop in the series. The Q outputs of successive flip-flops are coupled to the D-inputs of the next flip-flop in the series and provide the row select signals $RowSel_2$ through $RowSel_{512}$ with successive falling edge transitions of the vertical clock signal CV, as discussed further below in connection with Fig. 18. The last row select signal $RowSel_{512}$ also may be taken as an optional output of the array 100 as the signal LSTV (Last STage Vertical), which provides an indication (e.g., for diagnostic purposes) that the last row of the array has been selected. While not shown explicitly in Fig. 14, each of the row select signals $RowSel_1$ through $RowSel_{512}$ is applied to a corresponding inverter, the output of which is used to enable a given pixel in each column (as illustrated in Fig. 9 by the signals $\overline{RowSel_1}$ through $\overline{RowSel_n}$).

[00194] Regarding the column select shift registers 194_1 and 194_2, these are implemented in a manner similar to that of the row select shift registers, with each column select shift register comprising 256 series-connected flip-flops and responsible for enabling readout from either the odd columns of the array or the even columns of the array. For example, Fig. 15 illustrates the column select shift register 194_2, which is configured to enable

readout from all of the even numbered columns of the array in succession via the column select signals $ColSel_2$, $ColSel_4$,....$ColSel_{512}$, whereas another column select shift register 194_1 is configured to enable readout from all of the odd numbered columns of the array in succession (via column select signals $ColSel_1$, $ColSel_3$,....Col Sel_{511}). Both column select shift registers are controlled simultaneously by the horizontal data signal DH and the horizontal clock signal CH to provide the respective column select signals, as discussed further below in connection with Fig. 18. As shown in Fig. 15, the last column select signal $ColSel_{512}$ also may be taken as an optional output of the array 100 as the signal LSTH (Last STage Horizontal), which provides an indication (e.g., for diagnostic purposes) that the last column of the array has been selected.

[00195] With reference again for the moment to Fig. 7, Applicants have recognized and appreciated that an implementation for array row and column selection based on shift registers, as discussed above in connection with Figs. 13-15, is a significant improvement to the row and column decoder approach employed in various prior art ISFET array designs, including the design of Milgrew et al. shown in Fig. 7. In particular, regarding the row decoder 92 and the column decoder 94 shown in Fig. 7, the complexity of implementing these components in an integrated circuit array design increases dramatically as the size of the array is increased, as additional inputs to both decoders are required. For example, an array having 512 rows and columns as discussed above in connection with Fig. 13 would require nine inputs ($2^9 = 512$) per row and column decoder if such a scheme were employed for row and column selection; similarly, arrays having 7400 rows and 7400 columns, as discussed below in connection with other embodiments, would require 13 inputs ($2^{13} = 8192$) per row and column decoder. In contrast, the row and column select shift registers shown in Figs. 14 and 15 require no additional input signals as array size is increased, but rather additional D-type flip-flops (which are routinely implemented in a CMOS process). Thus, the shift register implementations shown in Figs. 14 and 15 provide an easily scalable solution to array row and column selection.

[00196] In the embodiment of Fig. 13, the "odd" column select shift register 194_1 provides odd column select signals to an "odd" output driver 198_1 and the even column select shift register 194_2 provides even column select signals to an "even" output driver 198_2. Both output drivers are configured similarly, and an example of the even output driver 198_2 is shown in Fig. 16. In particular, Fig. 16 shows that respective even column

output signals V_{COL2}, V_{COL4},...V_{COL512} (refer to Fig. 9 for the generic column signal output V_{COLj}) are applied to corresponding switches 191_2, 191_4,...191_{512}, responsive to the even column select signals $ColSel_2$, $ColSel_4$,....$ColSel_{512}$ provided by the column select register 194_2, to successively couple the even column output signals to the input of a buffer amplifier 199 (BUF) via a bus 175. In Fig. 16, the buffer amplifier 199 receives power from an output buffer positive supply voltage VDDO and an output buffer supply ground VSSO, and is responsive to an output buffer bias voltage VBO0 to set a corresponding bias current for the buffer output. Given the high impedance input of the buffer amplifier 199, a current sink 197 responsive to a bias voltage VB3 is coupled to the bus 175 to provide an appropriate drive current (e.g., on the order of approximately 100 μA) for the output of the column output buffer (see the buffer amplifier 111j of Fig. 9) of a selected column. The buffer amplifier 199 provides the output signal Vout2 based on the selected even column of the array; at the same time, with reference to Fig. 13, a corresponding buffer amplifier of the "odd" output driver 198_1 provides the output signal Vout1 based on a selected odd column of the array.

[00197] In one exemplary implementation, the switches of both the even and odd output drivers 198_1 and 198_2 (e.g., the switches 191_2, 191_4, ...191_{512} shown in Fig. 16) may be implemented as CMOS-pair transmission gates (including an n-channel MOSFET and a p-channel MOSFET; see Fig. 4), and inverters may be employed so that each column select signal and its complement may be applied to a given transmission gate switch 191 to enable switching. Each switch 191 has a series resistance when enabled or "on" to couple a corresponding column output signal to the bus 175; likewise, each switch adds a capacitance to the bus 175 when the switch is off. A larger switch reduces series resistance and allows a higher drive current for the bus 175, which generally allows the bus 175 to settle more quickly; on the other hand, a larger switch increases capacitance of the bus 175 when the switch is off, which in turn increases the settling time of the bus 175. Hence, there is a trade-off between switch series resistance and capacitance in connection with switch size.

[00198] The ability of the bus 175 to settle quickly following enabling of successive switches in turn facilitates rapid data acquisition from the array. To this end, in some embodiments the switches 191 of the output drivers 198_1 and 198_2 are particularly configured to significantly reduce the settling time of the bus 175. Both the n-channel and

the p-channel MOSFETs of a given switch add to the capacitance of the bus 175; however, n-channel MOSFETs generally have better frequency response and current drive capabilities than their p-channel counterparts. In view of the foregoing, Applicants have recognized and appreciated that some of the superior characteristics of n-channel MOSFETs may be exploited to improve settling time of the bus 175 by implementing "asymmetric" switches in which respective sizes for the n-channel MOSFET and p-channel MOSFET of a given switch are different.

[00199] For example, in one embodiment, with reference to Fig. 16, the current sink 197 may be configured such that the bus 175 is normally "pulled down" when all switches 191_2, 191_4, ...191_{512} are open or off (not conducting). Given a somewhat limited expected signal dynamic range for the column output signals based on ISFET measurements, when a given switch is enabled or on (conducting), in many instances most of the conduction is done by the n-channel MOSFET of the CMOS-pair constituting the switch. Accordingly, in one aspect of this embodiment, the n-channel MOSFET and the p-channel MOSFET of each switch 191 are sized differently; namely, in one exemplary implementation, the n-channel MOSFET is sized to be significantly larger than the p-channel MOSFET. More specifically, considering equally-sized n-channel and p-channel MOSFETs as a point of reference, in one implementation the n-channel MOSFET may be increased to be about 2 to 2.5 times larger, and the p-channel MOSFET may be decreased in size to be about 8 to 10 times smaller, such that the n-channel MOSFET is approximately 20 times larger than the p-channel MOSFET. Due to the significant decrease is size of the p-channel MOSFET and the relatively modest increase in size of the n-channel MOSFET, the overall capacitance of the switch in the off state is notably reduced, and there is a corresponding notable reduction in capacitance for the bus 175; at the same time, due to the larger n-channel MOSFET, there is a significant increase in current drive capability, frequency response and transconductance of the switch, which in turn results in a significant reduction in settling time of the bus 175.

[00200] While the example above describes asymmetric switches 191 for the output drivers 198_1 and 198_2 in which the n-channel MOSFET is larger than the p-channel MOSFET, it should be appreciated that in another embodiment, the converse may be implemented, namely, asymmetric switches in which the p-channel MOSFET is larger than the n-channel MOSFET. In one aspect of this embodiment, with reference again to Fig. 16,

the current sink 197 may alternatively serve as a source of current to appropriately drive the output of the column output buffer (see the buffer amplifier 111j of Fig. 9) of a selected column, and be configured such that the bus 175 is normally "pulled up" when all switches 191_2, 191_4, ...191_{512} are open or off (not conducting). In this situation, most of the switch conduction may be accomplished by the p-channel MOSFET of the CMOS-pair constituting the switch. Benefits of reduced switch capacitance (and hence reduced bus capacitance) may be realized in this embodiment, although the overall beneficial effect of reduced settling time for the bus 175 may be somewhat less than that described previously above, due to the lower frequency response of p-channel MOSFETs as compared to n-channel MOSFETs. Nevertheless, asymmetric switches based on larger p-channel MOSFETs may still facilitate a notable reduction in bus settling time, and may also provide for circuit implementations in which the column output buffer amplifier (111j of Fig. 9) may be a body-tied source follower with appreciably increased gain.

[00201] In yet another embodiment directed to facilitating rapid settling of the bus 175 shown in Fig. 16, it may be appreciated that fewer switches 191 coupled to the bus 175 results in a smaller bus capacitance. With this in mind, and with reference again to Fig. 13, in yet another embodiment, more than two output drivers 198_1 and 198_2 may be employed in the ISFET array 100 such that each output driver handles a smaller number of columns of the array. For example, rather than having all even columns handled by one driver and all odd columns handled by another driver, the array may include four column select registers $194_{1,2,3,4}$ and four corresponding output drivers $198_{1,2,3,4}$ such that each output driver handles one-fourth of the total columns of the array, rather than one-half of the columns. In such an implementation, each output driver would accordingly have half the number of switches 191 as compared with the embodiment discussed above in connection with Fig. 16, and the bus 175 of each output driver would have a corresponding lower capacitance, thereby improving bus settling time. While four output drivers are discussed for purposes of illustration in this example, it should be appreciated that the present disclosure is not limited in this respect, and virtually any number of output drivers greater than two may be employed to improve bus settling time in the scenario described above. Other array embodiments in which more than two output drivers are employed to facilitate rapid data acquisition from the array are discussed in greater detail below (e.g., in connection with Figs. 19-23).

[00202] In one aspect of the array design discussed above in connection with Figs. 13-16, separate analog supply voltage connections (for VDDA, VSSA), digital supply voltage connections (for VDDD, VSSD) and output buffer supply voltage connections (for VDDO, VSSO) are provided on the array to facilitate noise isolation and reduce signal cross-talk amongst various array components, thereby increasing the signal-to-noise ratio (SNR) of the output signals Vout1 and Vout2. In one exemplary implementation, the positive supply voltages VDDA, VDDD and VDDO each may be approximately 3.3 Volts. In another aspect, these voltages respectively may be provided "off chip" by one or more programmable voltage sources, as discussed further below in connection with Fig. 17.

[00203] Fig. 17 illustrates a block diagram of the sensor array 100 of Fig. 13 coupled to an array controller 250, according to one inventive embodiment of the present disclosure. In various exemplary implementations, the array controller 250 may be fabricated as a "stand alone" controller, or as a computer compatible "card" forming part of a computer 260, as discussed above in connection with Fig. 8. In one aspect, the functions of the array controller 250 may be controlled by the computer 260 through an interface block 252 (e.g., serial interface, via USB port or PCI bus, Ethernet connection, etc.), as shown in Fig. 17. In one embodiment, the array controller 250 is fabricated as a printed circuit board into which the array 100 plugs, similar to a conventional IC chip (e.g., the array 100 is configured as an ASIC that plugs into the array controller). In one aspect of such an embodiment, all or portions of the array controller 250 may be implemented as a field programmable gate array (FPGA) configured to perform various array controller functions described in further detail below.

[00204] Generally, the array controller 250 provides various supply voltages and bias voltages to the array 100, as well as various signals relating to row and column selection, sampling of pixel outputs and data acquisition. In particular, the array controller 250 reads the two analog output signals Vout1 (odd columns) and Vout2 (even columns) including multiplexed respective pixel voltage signals from the array 100 and then digitizes these respective pixel signals to provide measurement data to the computer 260, which in turn may store and/or process the data. In some implementations, the array controller 250 also may be configured to perform or facilitate various array calibration and diagnostic functions, and an optional array UV irradiation treatment as discussed above in connection with Fig. 11A.

[00205] As illustrated in Fig. 17, the array controller 250 generally provides to the array 100 the analog supply voltage and ground (VDDA, VSSA), the digital supply voltage and ground (VDDD, VSSD), and the buffer output supply voltage and ground (VDDO, VSSO). In one exemplary implementation, each of the supply voltages VDDA, VDDD and VDDO is approximately 3.3 Volts. As discussed above, in one aspect each of these power supply voltages is provided to the array 100 via separate conducting paths to facilitate noise isolation. In another aspect, these supply voltages may originate from respective power supplies/regulators, or one or more of these supply voltages may originate from a common source in a power supply 258 of the array controller 250. The power supply 258 also may provide the various bias voltages required for array operation (e.g., VB1, VB2, VB3, VB4, VBO0, V_{BODY}) and the reference voltage VREF used for array diagnostics and calibration. In another aspect, the power supply 258 includes one or more digital-to-analog converters (DACs) that may be controlled by the computer 260 to allow any or all of the bias voltages, reference voltage, and supply voltages to be changed under software control (i.e., programmable bias settings). For example, a power supply 258 responsive to computer control may facilitate adjustment of the bias voltages VB1 and VB2 for pixel drain current, VB3 for column bus drive, VB4 for column amplifier bandwidth, and VBO0 for column output buffer current drive. In some aspects, one or more bias voltages may be adjusted to optimize settling times of signals from enabled pixels. Additionally, the common body voltage V_{BODY} for all ISFETs of the array may be grounded during an optional post-fabrication UV irradiation treatment to reduce trapped charge, and then coupled to a higher voltage (e.g., VDDA) during diagnostic analysis, calibration, and normal operation of the array for measurement/data acquisition. Likewise, the reference voltage VREF may be varied to facilitate a variety of diagnostic and calibration functions.

[00206] As also shown in Fig. 17, the reference electrode 76 which is typically employed in connection with an analyte solution to be measured by the array 100 (as discussed above in connection with Fig. 1), may be coupled to the power supply 258 to provide a reference potential for the pixel output voltages. For example, in one implementation the reference electrode 76 may be coupled to a supply ground (e.g., the analog ground VSSA) to provide a reference for the pixel output voltages based on Eq. (3) above. In other exemplary implementations, the reference electrode voltage may be set by placing a solution/sample of interest having a known pH level in proximity to the sensor array 100 and adjusting the

reference electrode voltage until the array output signals Vout1 and Vout2 provide pixel voltages at a desired reference level, from which subsequent changes in pixel voltages reflect local changes in pH with respect to the known reference pH level. In general, it should be appreciated that a voltage associated with the reference electrode 76 need not necessarily be identical to the reference voltage VREF discussed above (which may be employed for a variety of array diagnostic and calibration functions), although in some implementations the reference voltage VREF provided by the power supply 258 may be used to set the voltage of the reference electrode 76.

[00207] Regarding data acquisition from the array 100, in one embodiment the array controller 250 of Fig. 17 may include one or more preamplifiers 253 to further buffer the output signals Vout1 and Vout2 from the sensor array and provide selectable gain. In one aspect, the array controller 250 may include one preamplifier for each output signal (e.g., two preamplifiers for two analog output signals). In other aspects, the preamplifiers may be configured to accept input voltages from 0.0 to 3.3 Volts, may have programmable/computer selectable gains (e.g., 1, 2, 5, 10 and 20) and low noise outputs (e.g., <10nV/sqrtHz), and may provide low pass filtering (e.g., bandwidths of 5 MHz and 25 MHz). In yet another aspect, the preamplifiers may have a programmable/computer selectable offset for input and/or output voltage signals to set a nominal level for either to a desired range.

[00208] The array controller 250 of Fig. 17 also comprises one or more analog-to-digital converters 254 (ADCs) to convert the sensor array output signals Vout1 and Vout2 to digital outputs (e.g., 10-bit or 12-bit) so as to provide data to the computer 260. In one aspect, one ADC may be employed for each analog output of the sensor array, and each ADC may be coupled to the output of a corresponding preamplifier (if preamplifiers are employed in a given implementation). In another aspect, the ADC(s) may have a computer-selectable input range (e.g., 50 mV, 200 mV, 500 mV, 1V) to facilitate compatibility with different ranges of array output signals and/or preamplifier parameters. In yet other aspects, the bandwidth of the ADC(s) may be greater than 60 MHz, and the data acquisition/conversion rate greater than 25 MHz (e.g., as high as 100 MHz or greater).

[00209] In the embodiment of Fig. 17, ADC acquisition timing and array row and column selection may be controlled by a timing generator 256. In particular, the timing generator

provides the digital vertical data and clock signals (DV, CV) to control row selection, the digital horizontal data and clock signals (DH, CH) to control column selection, and the column sample and hold signal COL SH to sample respective pixel voltages for an enabled row, as discussed above in connection with Fig. 9. In some implementations, the timing generator 256 may be implemented by a microprocessor executing code and configured as a multi-channel digital pattern generator to provide appropriately timed control signals. In one exemplary implementation, the timing generator 256 may be implemented as a field-programmable gate array (FPGA).

[00210] Fig. 18 illustrates an exemplary timing diagram for such signals, as provided by the timing generator 256, to acquire pixel data from the sensor array 100. For purposes of the following discussion, a "frame" is defined as a data set that includes a value (e.g., pixel output signal or voltage V_S) for each pixel in the array, and a "frame rate" is defined as the rate at which successive frames may be acquired from the array. In the example of Fig. 18, an exemplary frame rate of 20 frames/sec is chosen to illustrate operation of the array (i.e., row and column selection and signal acquisition); however, it should be appreciated that arrays and array controllers according to the present disclosure are not limited in this respect, as different frame rates, including lower frame rates (e.g., 1 to 10 frames/second) or higher frame rates (e.g., 25, 30, 40, 50, 60, 70 to 100 frames/sec., etc.), with arrays having the same or higher numbers of pixels, are possible. In some exemplary applications, a data set may be acquired that includes many frames over several seconds to conduct an experiment on a given analyte or analytes. Several such experiments may be performed in succession, in some cases with pauses in between to allow for data transfer/processing and/or washing of the sensor array ASIC and reagent preparation for a subsequent experiment.

[00211] In one implementation, the array controller 250 controls the array 100 to enable rows successively, one at a time. For example, with reference again for the moment to Fig. 9, a first row of pixels is enabled via the row select signal $\overline{\text{RowSel}_i}$. The enabled pixels are allowed to settle for some time period, after which the COL SH signal is asserted briefly to close the sample/hold switch in each column and store on the column's sample/hold capacitor C_{sh} the voltage value output by the first pixel in the column. This voltage is then available as the column output voltage V_{COLj} applied to one of the two (odd and even

column) array output drivers 198_1 and 198_2 (e.g., see Fig. 16). The COL SH signal is then de-asserted, thereby opening the sample/hold switches in each column and decoupling the column output buffer 111j from the column amplifiers 107A and 107B. Shortly thereafter, the second row of pixels is enabled via the row select signal $\overline{\text{RowSel}_2}$. During the time period in which the second row of pixels is allowed to settle, the column select signals are generated two at a time (one odd and one even; odd column select signals are applied in succession to the odd output driver, even column select signals are applied in succession to the even output driver) to read the column output voltages associated with the first row. Thus, while a given row in the array is enabled and settling, the previous row is being read out, two columns at a time. By staggering row selection and sampling/readout, and by reading multiple columns at a time for a given row, a frame of data may be acquired from the array in a significantly streamlined manner.

[00212] Fig. 18 illustrates the timing details of the foregoing process for an exemplary frame rate of 20 frames/sec. Given this frame rate and 512 rows in the array, each row must be read out in approximately 98 microseconds, as indicated by the vertical delineations in Fig. 18. Accordingly, the vertical clock signal CV has a period of 98 microseconds (i.e., a clock frequency of over 10 kHz), with a new row being enabled on a trailing edge (negative transition) of the CV signal. The left side of Fig. 18 reflects the beginning of a new frame cycle, at which point the vertical data signal DV is asserted before a first trailing edge of the CV signal and de-asserted before the next trailing edge of the CV signal (for data acquisition from successive frames, the vertical data signal is reasserted again only after row 512 is enabled). Also, immediately before each trailing edge of the CV signal (i.e., new row enabled), the COL SH signal is asserted for 2 microseconds, leaving approximately 50 nanoseconds before the trailing edge of the CV signal.

[00213] In Fig. 18, the first occurrence of the COL SH signal is actually sampling the pixel values of row 512 of the array. Thus, upon the first trailing edge of the CV signal, the first row is enabled and allowed to settle (for approximately 96 microseconds) until the second occurrence of the COL SH signal. During this settling time for the first row, the pixel values of row 512 are read out via the column select signals. Because two column select signals are generated simultaneously to read 512 columns, the horizontal clock signal CH must generate 256 cycles within this period, each trailing edge of the CH signal

generating one odd and one even column select signal. As shown in Fig. 18, the first trailing edge of the CH signal in a given row is timed to occur two microseconds after the selection of the row to allow for settling of the voltage values stored on the sample/hold capacitors C_{sh} and provided by the column output buffers. Also for each row, the horizontal data signal DH is asserted before the first trailing edge of the CH signal and de-asserted before the next trailing edge of the CH signal. The last two columns (e.g., 511 and 512) are selected before the occurrence of the COL SH signal which, as discussed above, occurs approximately two microseconds before the next row is enabled. Thus, 512 columns are read, two at a time, within a time period of approximately 94 microseconds (i.e., 98 microseconds per row, minus two microseconds at the beginning and end of each row). This results in a data rate for each of the array output signals Vout1 and Vout2 of approximately 2.7 MHz. In another aspect, the ADC(s) 254 may be controlled by the timing generator 256 to sample the output signals Vout1 and Vout2 at a significantly higher rate to provide multiple digitized samples for each pixel measurement, which may then be averaged (e.g., the ADC data acquisition rate may be approximately 100 MHz to sample the 2.7 MHz array output signals, thereby providing as many as approximately 35-40 samples per pixel measurement).

[00214] In addition to controlling the sensor array and ADCs, the timing generator 256 may be configured to facilitate various array calibration and diagnostic functions, as well as an optional UV irradiation treatment. To this end, the timing generator may utilize the signal LSTV indicating the selection of the last row of the array and the signal LSTH to indicate the selection of the last column of the array. The timing generator 256 also may be responsible for generating the CAL signal which applies the reference voltage VREF to the column buffer amplifiers, and generating the UV signal which grounds the drains of all ISFETs in the array during a UV irradiation process (see Fig. 9). The timing generator also may provide some control function over the power supply 258 during various calibration and diagnostic functions, or UV irradiation, to appropriately control supply or bias voltages; for example, during UV irradiation, the timing generator may control the power supply to couple the body voltage V_{BODY} to ground while the UV signal is activated to ground the ISFET drains. With respect to array calibration and diagnostics, as well as UV irradiation, in some implementations the timing generator may receive specialized programs from the computer 260 to provide appropriate control signals. In one aspect, the computer 260 may

use various data obtained from dummy pixels of the array, as well as column information based on the application of the CAL signal and the reference voltage VREF, to determine various calibration parameters associated with a given array and/or generate specialized programs for calibration and diagnostic functions.

[00215] With respect to the computer interface 252 of the array controller 250, in one exemplary implementation the interface is configured to facilitate a data rate of approximately 200 MB/sec to the computer 260, and may include local storage of up to 400 MB or greater. The computer 260 is configured to accept data at a rate of 200 MB/sec, and process the data so as to reconstruct an image of the pixels (e.g., which may be displayed in false-color on a monitor). For example, the computer may be configured to execute a general-purpose program with routines written in C++ or Visual Basic to manipulate the data and display is as desired.

[00216] Having discussed several aspects of an exemplary ISFET array and an array controller according to the present disclosure, Figs. 19-23 illustrate block diagrams of alternative CMOS IC chip implementations of ISFET sensor arrays having greater numbers of pixels, according to yet other inventive embodiments. In one aspect, each of the ISFET arrays discussed further below in connection with Figs. 19-23 may be controlled by an array controller similar to that shown in Fig. 17, in some cases with minor modifications to accommodate higher numbers of pixels (e.g., additional preamplifiers 253 and analog-to-digital converters 254).

[00217] Fig. 19 illustrates a block diagram of an ISFET sensor array 100A based on the column and pixel designs discussed above in connection with Figs. 9-12 and a 0.35 micrometer CMOS fabrication process, according to one inventive embodiment. The array 100A includes 2048 columns 102_1 through 102_{2048}, wherein each column includes 2048 geometrically square pixels 105_1 through 105_{2048}, each having a size of approximately 9 micrometers by 9 micrometers. Thus, the array includes over four million pixels (> 4 Mega-pixels) and, in one exemplary implementation, the complete array (ISFET pixels and associated circuitry) may be fabricated as an integrated circuit chip having dimensions of approximately 20.5 millimeters by 20.5 millimeters.

[00218] In one aspect of the embodiment shown in Fig. 19, the array 100A may be configured, at least in part, as multiple groups of pixels that may be respectively controlled.

For example, each column of pixels may be divided into top and bottom halves, and the collection of pixels in respective top halves of columns form a first group 400_1 of rows (e.g., a top group, rows 1-1024) and the collection of pixels in respective bottom halves of columns form a second group 400_2 of rows (e.g., a bottom group, rows 1025-2048). In turn, each of the first and second (e.g., top and bottom) groups of rows is associated with corresponding row select registers, column bias/readout circuitry, column select registers, and output drivers. In this manner, pixel selection and data acquisition from each of the first and second groups of rows 400_1 and 400_2 is substantially similar to pixel selection and data acquisition from the entire array 100 shown in Fig. 13; stated differently, in one aspect, the array 100A of Fig. 19 substantially comprises two simultaneously controlled "sub-arrays" of different pixel groups to provide for significantly streamlined data acquisition from higher numbers of pixels.

[00219] In particular, Fig. 19 shows that row selection of the first group 400_1 of rows may be controlled by a first row select register 192_1, and row selection of the second group 400_2 of rows may be controlled by a second row select register 192_2. In one aspect, each of the row select registers 192_1 and 192_2 may be configured as discussed above in connection with Fig. 14 to receive vertical clock (CV) and vertical data (DV) signals and generate row select signals in response; for example the first row select register 192_1 may generate the signals $\overline{\text{RowSel}_1}$ through $\overline{\text{RowSel}_{1024}}$ and the second row select register 192_2 may generate the signals $\overline{\text{RowSel}_{1025}}$ through $\overline{\text{RowSel}_{2048}}$. In another aspect, both row select registers 192_1 and 192_2 may simultaneously receive common vertical clock and data signals, such that two rows of the array are enabled at any given time, one from the top group and another from the bottom group.

[00220] For each of the first and second groups of rows, the array 100A of Fig. 19 further comprises column bias/readout circuitry 110_{1T}-110_{2048T} (for the first row group 400_1) and 110_{1B}-110_{2048B} (for the second row group 400_2), such that each column includes two instances of the bias/readout circuitry 110j shown in Fig. 9. The array 100A also comprises two column select registers $192_{1,2}$ (odd and even) and two output drivers $198_{1,2}$ (odd and even) for the second row group 400_2, and two column select registers $192_{3,4}$ (odd and even) and two output drivers $198_{3,4}$ (odd and even) for the first row group 400_1 (i.e., a total of four column select registers and four output drivers). The column select registers receive

horizontal clock signals (CHT and CHB for the first row group and second row group, respectively) and horizontal data signals (DHT and DHB for the first row group and second row group, respectively) to control odd and even column selection. In one implementation, the CHT and CHB signals may be provided as common signals, and the DHT and DHB may be provided as common signals, to simultaneously read out four columns at a time from the array (i.e., one odd and one even column from each row group); in particular, as discussed above in connection with Figs. 13-18, two columns may be simultaneously read for each enabled row and the corresponding pixel voltages provided as two output signals. Thus, via the enablement of two rows at any given time, and reading of two columns per row at any given time, the array 100A may provide four simultaneous output signals Vout1, Vout2, Vout3 and Vout4.

[00221] In one exemplary implementation of the array 100A of Fig. 19, in which complete data frames (all pixels from both the first and second row groups 400_1 and 400_2) are acquired at a frame rate of 20 frames/sec, 1024 pairs of rows are successively enabled for periods of approximately 49 microseconds each. For each enabled row, 1024 pixels are read out by each column select register/output driver during approximately 45 microseconds (allowing 2 microseconds at the beginning and end of each row, as discussed above in connection with Fig. 18). Thus, in this example, each of the array output signals Vout1, Vout2, Vout3 and Vout4 has a data rate of approximately 23 MHz. Again, it should be appreciated that in other implementations, data may be acquired from the array 100A of Fig. 19 at frame rates other than 20 frames/sec (e.g., 50-100 frames/sec).

[00222] Like the array 100 of Fig. 13, in yet other aspects the array 100A of Fig. 19 may include multiple rows and columns of dummy or reference pixels 103 around a perimeter of the array to facilitate preliminary test/evaluation data, offset determination an/or array calibration. Additionally, various power supply and bias voltages required for array operation (as discussed above in connection with Fig. 9) are provided to the array 100A in block 195, in a manner similar to that discussed above in connection with Fig. 13.

[00223] Fig. 20 illustrates a block diagram of an ISFET sensor array 100B based on a 0.35 micrometer CMOS fabrication process and having a configuration substantially similar to the array 100A discussed above in Fig. 19, according to yet another inventive embodiment. While the array 100B also is based generally on the column and pixel designs

discussed above in connection with Figs. 9-12, the pixel size/pitch in the array 100B is smaller than that of the pixel shown in Fig. 10. In particular, with reference again to Figs. 10 and 11, the dimension "e" shown in Fig. 10 is substantially reduced in the embodiment of Fig. 20, without affecting the integrity of the active pixel components disposed in the central region of the pixel, from approximately 9 micrometers to approximately 5 micrometers; similarly, the dimension "f' shown in Fig. 10 is reduced from approximately 7 micrometers to approximately 4 micrometers. Stated differently, some of the peripheral area of the pixel surrounding the active components is substantially reduced with respect to the dimensions given in connection with Fig. 10, without disturbing the top-view and cross-sectional layout and design of the pixel's active components as shown in Fig. 10 and 11. A top view of such a pixel 105A is shown in Fig. 20A, in which the dimension "e" is 5.1 micrometers and the dimension "f" is 4.1 micrometers. In one aspect of this pixel design, to facilitate size reduction, fewer body connections B are included in the pixel 105A (e.g., one at each corner of the pixel) as compared to the pixel shown in Fig. 10, which includes several body connections B around the entire perimeter of the pixel.

[00224] As noted in Fig. 20, the array 100B includes 1348 columns 102_1 through 102_{1348}, wherein each column includes 1152 geometrically square pixels $105A_1$ through $105A_{1152}$, each having a size of approximately 5 micrometers by 5 micrometers. Thus, the array includes over 1.5 million pixels (> 1.5 Mega-pixels) and, in one exemplary implementation, the complete array (ISFET pixels and associated circuitry) may be fabricated as an integrated circuit chip having dimensions of approximately 9 millimeters by 9 millimeters. Like the array 100A of Fig. 19, in one aspect the array 100B of Fig. 20 is divided into two groups of rows 400_1 and 400_2, as discussed above in connection with Fig. 19. In one exemplary implementation, complete data frames (all pixels from both the first and second row groups 400_1 and 400_2) are acquired at a frame rate of 50 frames/sec, thereby requiring 576 pairs of rows to be successively enabled for periods of approximately 35 microseconds each. For each enabled row, 674 pixels are read out by each column select register/output driver during approximately 31 microseconds (allowing 2 microseconds at the beginning and end of each row, as discussed above in connection with Fig. 18). Thus, in this example, each of the array output signals Vout1, Vout2, Vout3 and Vout4 has a data rate of approximately 22 MHz. Again, it should be appreciated that in other implementations, data may be acquired from the array 100B of Fig. 20 at frame rates other than 50 frames/sec.

[00225] Fig. 21 illustrates a block diagram of an ISFET sensor array 100C based on a 0.35 micrometer CMOS fabrication process and incorporating the smaller pixel size discussed above in connection with Figs. 20 and 20A (5.1 micrometer square pixels), according to yet another embodiment. As noted in Fig. 21, the array 100C includes 4000 columns 102_1 through 102_{4000}, wherein each column includes 3600 geometrically square pixels $105A_1$ through $105A_{3600}$, each having a size of approximately 5 micrometers by 5 micrometers. Thus, the array includes over 14 million pixels (> 14 Mega-pixels) and, in one exemplary implementation, the complete array (ISFET pixels and associated circuitry) may be fabricated as an integrated circuit chip having dimensions of approximately 22 millimeters by 22 millimeters. Like the arrays 100A and 100B of Figs. 19 and 20, in one aspect the array 100C of Fig. 21 is divided into two groups of rows 400_1 and 400_2. However, unlike the arrays 100A and 100B, for each row group the array 100C includes sixteen column select registers and sixteen output drivers to simultaneously read sixteen pixels at a time in an enabled row, such that thirty-two output signals Vout1-Vout32 may be provided from the array 100C. In one exemplary implementation, complete data frames (all pixels from both the first and second row groups 400_1 and 400_2) may be acquired at a frame rate of 50 frames/sec, thereby requiring 1800 pairs of rows to be successively enabled for periods of approximately 11 microseconds each. For each enabled row, 250 pixels (4000/16) are read out by each column select register/output driver during approximately 7 microseconds (allowing 2 microseconds at the beginning and end of each row). Thus, in this example, each of the array output signals Vout1 – Vout32 has a data rate of approximately 35 MHz. As with the previous embodiments, it should be appreciated that in other implementations, data may be acquired from the array 100C at frame rates other than 50 frames/sec.

[00226] While the exemplary arrays discussed above in connection with Figs. 13-21 are based on a 0.35 micrometer conventional CMOS fabrication process, it should be appreciated that arrays according to the present disclosure are not limited in this respect, as CMOS fabrication processes having feature sizes of less than 0.35 micrometers may be employed (e.g., 0.18 micrometer CMOS processing techniques) to fabricate such arrays. Accordingly, ISFET sensor arrays with a pixel size/pitch significantly below 5 micrometers may be fabricated, providing for significantly denser ISFET arrays. For example, Figs. 22 and 23 illustrate respective block diagrams of ISFET sensor arrays 100D and 100E

according to yet other embodiments based on a 0.18 micrometer CMOS fabrication process, in which a pixel size of 2.6 micrometers is achieved. The pixel design itself is based substantially on the pixel 105A shown in Fig. 20A, albeit on a smaller scale due to the 0.18 micrometer CMOS process.

[00227] The array 100D of Fig. 22 includes 2800 columns 102_1 through 102_{2800}, wherein each column includes 2400 geometrically square pixels each having a size of approximately 2.6 micrometers by 2.6 micrometers. Thus, the array includes over 6.5 million pixels (> 6.5 Mega-pixels) and, in one exemplary implementation, the complete array (ISFET pixels and associated circuitry) may be fabricated as an integrated circuit chip having dimensions of approximately 9 millimeters by 9 millimeters. Like the arrays 100A, 100B and 100C of Figs. 19-21, in one aspect the array 100D of Fig. 22 is divided into two groups of rows 400_1 and 400_2. However, unlike the arrays 100A, 100B, and 100C, for each row group the array 100D includes eight column select registers and eight output drivers to simultaneously read eight pixels at a time in an enabled row, such that sixteen output signals Vout1-Vout16 may be provided from the array 100D. In one exemplary implementation, complete data frames (all pixels from both the first and second row groups 400_1 and 400_2) may be acquired at a frame rate of 50 frames/sec, thereby requiring 1200 pairs of rows to be successively enabled for periods of approximately 16-17 microseconds each. For each enabled row, 350 pixels (2800/8) are read out by each column select register/output driver during approximately 14 microseconds (allowing 1 to 2 microseconds at the beginning and end of each row). Thus, in this example, each of the array output signals Vout1 – Vout16 has a data rate of approximately 25 MHz. As with the previous embodiments, it should be appreciated that in other implementations, data may be acquired from the array 100D at frame rates other than 50 frames/sec.

[00228] The array 100E of Fig. 23 includes 7400 columns 102_1 through 102_{7400}, wherein each column includes 7400 geometrically square pixels each having a size of approximately 2.6 micrometers by 2.6 micrometers. Thus, the array includes over 54 million pixels (> 54 Mega-pixels) and, in one exemplary implementation, the complete array (ISFET pixels and associated circuitry) may be fabricated as an integrated circuit chip having dimensions of approximately 21 millimeters by 21 millimeters. Like the arrays 100A-100D of Figs. 19-22, in one aspect the array 100E of Fig. 23 is divided into two groups of rows 400_1 and 400_2. However, unlike the arrays 100A-100D, for each row group the array 100E includes

thirty-two column select registers and thirty-two output drivers to simultaneously read thirty-two pixels at a time in an enabled row, such that sixty-four output signals Vout1-Vout64 may be provided from the array 100E. In one exemplary implementation, complete data frames (all pixels from both the first and second row groups 400_1 and 400_2) may be acquired at a frame rate of 100 frames/sec, thereby requiring 3700 pairs of rows to be successively enabled for periods of approximately 3 microseconds each. For each enabled row, 230 pixels (7400/32) are read out by each column select register/output driver during approximately 700 nanoseconds. Thus, in this example, each of the array output signals Vout1 – Vout64 has a data rate of approximately 328 MHz. As with the previous embodiments, it should be appreciated that in other implementations, data may be acquired from the array 100D at frame rates other than 100 frames/sec.

[00229] Thus, in various examples of ISFET arrays based on the inventive concepts disclosed herein, an array pitch of approximately nine (9) micrometers (e.g., a sensor surface area of less than ten micrometers by ten micrometers) allows an ISFET array including over 256,000 pixels (i.e., a 512 by 512 array), together with associated row and column select and bias/readout electronics, to be fabricated on a 7 millimeter by 7 millimeter semiconductor die, and a similar sensor array including over four million pixels (i.e., a 2048 by 2048 array, over 4 Mega-pixels) to be fabricated on a 21 millimeter by 21 millimeter die. In other examples, an array pitch of approximately 5 micrometers allows an ISFET array including approximately 1.55 Mega-pixels (i.e., a 1348 by 1152 array) and associated electronics to be fabricated on a 9 millimeter by 9 millimeter die, and an ISFET sensor array including over 14 Mega-pixels and associated electronics on a 22 millimeter by 20 millimeter die. In yet other implementations, using a CMOS fabrication process in which feature sizes of less than 0.35 micrometers are possible (e.g., 0.18 micrometer CMOS processing techniques), ISFET sensor arrays with a pixel size/pitch significantly below 5 micrometers may be fabricated (e.g., array pitch of 2.6 micrometers or pixel/sensor area of less than 8 or 9 micrometers^2), providing for significantly dense ISFET arrays.

[00230] In the embodiments of ISFET arrays discussed above, array pixels employ a p-channel ISFET, as discussed above in connection with Fig. 9. It should be appreciated, however, that ISFET arrays according to the present disclosure are not limited in this respect, and that in other embodiments pixel designs for ISFET arrays may be based on an

n-channel ISFET. In particular, any of the arrays discussed above in connection with Figs. 13 and 19-23 may be implemented with pixels based on n-channel ISFETs.

[00231] For example, Fig. 24 illustrates the pixel design of Fig. 9 implemented with an n-channel ISFET and accompanying n-channel MOSFETs, according to another inventive embodiment of the present disclosure. More specifically, Fig. 24 illustrates one exemplary pixel 105_1 of an array column (i.e., the first pixel of the column), together with column bias/readout circuitry 110j, in which the ISFET 150 (Q1) is an n-channel ISFET. Like the pixel design of Fig. 9, the pixel design of Fig. 24 includes only three components, namely, the ISFET 150 and two n-channel MOSFET switches Q2 and Q3, responsive to one of *n* row select signals ($RowSel_1$ through $RowSel_n$, logic high active). No transmission gates are required in the pixel of Fig. 24, and all devices of the pixel are of a "same type," i.e., n-channel devices. Also like the pixel design of Fig. 9, only four signal lines per pixel, namely the lines 112_1, 114_1, 116_1 and 118_1, are required to operate the three components of the pixel 105_1 shown in Fig. 24. In other respects, the pixel designs of Fig. 9 and Fig. 24 are similar, in that they are both configured with a constant drain current I_{Dj} and a constant drain-to-source voltage V_{DSj} to obtain an output signal V_{Sj} from an enabled pixel.

[00232] One of the primary differences between the n-channel ISFET pixel design of Fig. 24 and the p-channel ISFET design of Fig. 9 is the opposite direction of current flow through the pixel. To this end, in Fig. 24, the element 106_j is a controllable current sink coupled to the analog circuitry supply voltage ground VSSA, and the element 108_j of the bias/readout circuitry 110j is a controllable current source coupled to the analog positive supply voltage VDDA. Additionally, the body connection of the ISFET 150 is not tied to its source, but rather to the body connections of other ISFETs of the array, which in turn is coupled to the analog ground VSSA, as indicated in Fig. 24.

[00233] In addition to the pixel designs shown in Figs. 9 and 24 (based on a constant ISFET drain current and constant ISFET drain-source voltage), alternative pixel designs are contemplated for ISFET arrays, based on both p-channel ISFETs and n-channel ISFETs, according to yet other inventive embodiments of the present disclosure, as illustrated in Figs. 25-27. As discussed below, some alternative pixel designs may require additional and/or modified signals from the array controller 250 to facilitate data acquisition. In particular, a common feature of the pixel designs shown in Figs. 25-27 includes a sample

and hold capacitor within each pixel itself, in addition to a sample and hold capacitor for each column of the array. While the alternative pixel designs of Figs. 25-27 generally include a greater number of components than the pixel designs of Figs. 9 and 24, the feature of a pixel sample and hold capacitor enables "snapshot" types of arrays, in which all pixels of an array may be enabled simultaneously to sample a complete frame and acquire signals representing measurements of one or more analytes in proximity to respective ISFETs of the array. In some applications, this may provide for higher data acquisition speeds and/or improved signal sensitivity (e.g., higher signal-to-noise ratio).

[00234] Fig. 25 illustrates one such alternative design for a single pixel 105C and associated column circuitry 110j. The pixel 105C employs an n-channel ISFET and is based generally on the premise of providing a constant voltage across the ISFET Q1 based on a feedback amplifier (Q4, Q5 and Q6). In particular, transistor Q4 constitutes the feedback amplifier load, and the amplifier current is set by the bias voltage VB1 (provided by the array controller). Transistor Q5 is a common gate amplifier and transistor Q6 is a common source amplifier. Again, the purpose of feedback amplifier is to hold the voltage across the ISFET Q1 constant by adjusting the current supplied by transistor Q3. Transistor Q2 limits the maximum current the ISFET Q1 can draw (e.g., so as to prevent damage from overheating a very large array of pixels). This maximum current is set by the bias voltage VB2 (also provided by the array controller). In one aspect of the pixel design shown in Fig. 25, power to the pixel 105C may be turned off by setting the bias voltage VB2 to 0 Volts and the bias voltage VB1 to 3.3 Volts. In this manner, the power supplied to large arrays of such pixels may be modulated (turned on for a short time period and then off by the array controller) to obtain ion concentration measurements while at the same time reducing overall power consumption of the array. Modulating power to the pixels also reduces heat dissipation of the array and potential heating of the analyte solution, thereby also reducing any potentially deleterious effects from sample heating.

[00235] In Fig. 25, the output of the feedback amplifier (the gate of transistor Q3) is sampled by MOS switch Q7 and stored on a pixel sample and hold capacitor Csh within the pixel itself. The switch Q7 is controlled by a pixel sample and hold signal pSH (provided to the array chip by the array controller), which is applied simultaneously to all pixels of the array so as to simultaneously store the readings of all the pixels on their respective sample and hold capacitors. In this manner, arrays based on the pixel design of Fig. 25 may be

considered as "snapshot" arrays, in that a full frame of data is sampled at any given time, rather than sampling successive rows of the array. After each pixel value is stored on the corresponding pixel sample and hold capacitor Csh, each pixel 105C (ISFET and feedback amplifier) is free to acquire another pH reading or it can by turned off to conserve power.

[00236] In Fig. 25, the pixel values stored on all of the pixel sample and hold capacitors Csh are applied to the column circuitry 110j one row at a time through source follower Q8, which is enabled via the transistor Q9 in response to a row select signal (e.g., RowSel1). In particular, after a row is selected and has settled out, the values stored in the pixel sample and hold capacitors are then in turn stored on the column sample and hold capacitors Csh2, as enabled by the column sample and hold signal COL SH, and provided as the column output signal V_{COLj}.

[00237] Fig. 26 illustrates another alternative design for a single pixel 105D and associated column circuitry 110j, according to one embodiment of the present disclosure. In this embodiment, the ISFET is shown as a p-channel device. At the start of a data acquisition cycle, CMOS switches controlled by the signals pSH (pixel sample/hold) and pRST (pixel reset) are closed (these signals are supplied by the array controller). This pulls the source of ISFET (Q1) to the voltage VRST. Subsequently, the switch controlled by the signal pRST is opened, and the source of ISFET Q1 pulls the pixel sample and hold capacitor Csh to a threshold below the level set by pH. The switch controlled by the signal pSH is then opened, and the pixel output value is coupled, via operation of a switch responsive to the row select signal RowSel1, to the column circuitry 110j to provide the column output signal V_{COLj}. Like the pixel design in the embodiment illustrated in Fig. 25, arrays based on the pixel 105D are "snapshot" type arrays in that all pixels of the array may be operated simultaneously. In one aspect, this design allows a long simultaneous integration time on all pixels followed by a high-speed read out of an entire frame of data.

[00238] Fig. 27 illustrates yet another alternative design for a single pixel 105E and associated column circuitry 110j, according to one embodiment of the present disclosure. In this embodiment, again the ISFET is shown as a p-channel device. At the start of a data acquisition cycle, the switches operated by the control signals p1 and pRST are briefly closed. This clears the value stored on the sampling capacitor Csh and allows a charge to be stored on ISFET (Q1). Subsequently, the switch controlled by the signal pSH is closed,

allowing the charge stored on the ISFET Q1 to be stored on the pixel sample and hold capacitor Csh. The switch controlled by the signal pSH is then opened, and the pixel output value is coupled, via operation of a switch responsive to the row select signal RowSel1, to the column circuitry 110j to provide the column output signal V_{COLj}. Gain may be provided in the pixel 105E via the ratio of the ISFET capacitance to the Csh cap, i.e., gain = C_{QI} / C_{sh} , or by enabling the pixel multiple times (i.e., taking multiple samples of the analyte measurement) and accumulating the ISFET output on the pixel sample and hold capacitor Csh without resetting the capacitor (i.e., gain is a function of the number of accumulations). Like the embodiments of Figs. 25 and 26, arrays based on the pixel 105D are "snapshot" type arrays in that all pixels of the array may be operated simultaneously.

[00239] Turning from the sensor discussion, we will now be addressing the combining of the ISFET array with a microwell array and the attendant fluidics. As most of the drawings of the microwell array structure are presented only in cross-section or showing that array as only a block in a simplified diagram, Figs. 28A and 28B are provided to assist the reader in beginning to visualize the resulting apparatus in three-dimensions. Fig. 28A shows a group of round cylindrical wells 2810 arranged in an array, while Fig. 28B shows a group of rectangular cylindrical wells 2830 arranged in an array. It will be seen that the wells are separated (isolated) from each other by the material 2840 forming the well walls. While it is certain possible to fabricate wells of other cross sections, it is not believed to be advantageous to do so. Such an array of microwells sits over the above-discussed ISFET array, with one or more ISFETs per well. In the subsequent drawings, when the microwell array is identified, one may picture one of these arrays.

[00240] Fluidic System: Apparatus And Method For Use With High Density Electronic Sensor Arrays

[00241] For many uses, to complete a system for sensing chemical reactions or chemical agents using the above-explained high density electronic arrays, techniques and apparatus are required for delivery to the array elements (called "pixels") fluids containing chemical or biochemical components for sensing. In this section, exemplary techniques and methods will be illustrated, which are useful for such purposes, with desirable characteristics.

[00242] As high speed operation of the system may be desired, it is preferred that the fluid delivery system, insofar as possible, not limit the speed of operation of the overall system.

[00243] Accordingly, needs exist not only for high-speed, high-density arrays of ISFETs or other elements sensitive to ion concentrations or other chemical attributes, or changes in chemical attributes, but also for related mechanisms and techniques for supplying to the array elements the samples to be evaluated, in sufficiently small reaction volumes as to substantially advance the speed and quality of detection of the variable to be sensed.

[00244] There are two and sometimes three components or subsystems, and related methods, involved in delivery of the subject chemical samples to the array elements: (1) macrofluidic system of reagent and wash fluid supplies and appropriate valving and ancillary apparatus, (2) a flow cell and (3) in many applications, a microwell array. Each of these subsystems will be discussed, though in reverse order.

[00245] Microwell Array

[00246] As discussed elsewhere, for many uses, such as in DNA sequencing, it is desirable to provide over the array of semiconductor sensors a corresponding array of microwells, each microwell being small enough preferably to receive only one DNA-loaded bead, in connection with which an underlying pixel in the array will provide a corresponding output signal.

[00247] The use of such a microwell array involves three stages of fabrication and preparation, each of which is discussed separately: (1) creating the array of microwells to result in a chip having a coat comprising a microwell array layer; (2) mounting of the coated chip to a fluidic interface; and in the case of DNA sequencing, (3) loading DNA-loaded bead or beads into the wells. It will be understood, of course, that in other applications, beads may be unnecessary or beads having different characteristics may be employed.

[00248] Microwell Array Fabrication

[00249] Microwell fabrication may be accomplished in a number of ways. The actual details of fabrication may require some experimentation and vary with the processing capabilities that are available.

[00250] In general, fabrication of a high density array of microwells involves photo-lithographically patterning the well array configuration on a layer or layers of material such as photoresist (organic or inorganic), a dielectric, using an etching process. The patterning may be done with the material on the sensor array or it may be done separately and then transferred onto the sensor array chip, of some combination of the two. However, techniques other than photolithography are not to be excluded if they provide acceptable results.

[00251] One example of a method for forming a microwell array is now discussed, starting with reference to Fig. 29. That figure diagrammatically depicts a top view of one corner (i.e., the lower left corner) of the layout of a chip showing an array 2910 of the individual ISFET sensors 2912 on the CMOS die 2914. Signal lines 2916 and 2918 are used for addressing the array and reading its output. Block 2920 represents some of the electronics for the array, as discussed above, and layer 2922 represents a portion of a wall which becomes part of a microfluidics structure, the flow cell, as more fully explained below; the flow cell is that structure which provides a fluid flow over the microwell array or over the sensor surface directly, if there is no microwell structure. On the surface of the die, a pattern such as pattern 2922 at the bottom left of Fig. 29 may be formed during the semiconductor processing to form the ISFETs and associated circuitry, for use as alignment marks for locating the wells over the sensor pixels when the dielectric has covered the die's surface.

[00252] After the semiconductor structures, as shown, are formed, the microwell structure is applied to the die. That is, the microwell structure can be formed right on the die or it may be formed separately and then mounted onto the die, either approach being acceptable. To form the microwell structure on the die, various processes may be used. For example, the entire die may be spin-coated with, for example, a negative photoresist such as Microchem's SU-8 2015 or a positive resist/polyimide such as HD Microsystems HD8820, to the desired height of the microwells. The desired height of the wells (e.g., about 4 - 12 μm in the example of one pixel per well, though not so limited as a general matter) in the photoresist layer(s) can be achieved by spinning the appropriate resist at predetermined rates (which can be found by reference to the literature and manufacturer specifications, or empirically), in one or more layers. (Well height typically may be selected in correspondence with the lateral dimension of the sensor pixel, preferably for a nominal 1:1

– 1.5:1 aspect ratio, height:width or diameter. Based on signal-to-noise considerations, there is a relationship between dimensions and the required data sampling rates to achieve a desired level of performance. Thus there are a number of factors that will go into selecting optimum parameters for a given application.) Alternatively, multiple layers of different photoresists may be applied or another form of dielectric material may be deposited. Various types of chemical vapor deposition may also be used to build up a layer of materials suitable for microwell formation therein.

[00253] Once the photoresist layer (the singular form "layer" is used to encompass multiple layers in the aggregate, as well) is in place, the individual wells (typically mapped to have either one or four ISFET sensors per well) may be generated by placing a mask (e.g., of chromium) over the resist-coated die and exposing the resist to cross-linking (typically UV) radiation. All resist exposed to the radiation (i.e., where the mask does not block the radiation) becomes cross-linked and as a result will form a permanent plastic layer bonded to the surface of the chip (die). Unreacted resist (i.e., resist in areas which are not exposed, due to the mask blocking the light from reaching the resist and preventing cross-linking) is removed by washing the chip in a suitable solvent (i.e., developer) such as propyleneglycolmethylethylacetate (PGMEA) or other appropriate solvent. The resultant structure defines the walls of the microwell array.

[00254] Fig. 30 shows an example of a layout for a portion of a chromium mask 3010 for a one-sensor-per-well embodiment, corresponding to the portion of the die shown in Fig. 29. The grayed areas 3012, 3014 are those that block the UV radiation. The alignment marks in the white portions 3016 on the bottom left quadrant of Fig. 30, within gray area 3012, are used to align the layout of the wells with the ISFET sensors on the chip surface. The array of circles 3014 in the upper right quadrant of the mask block radiation from reaching the well areas, to leave unreacted resist which can be dissolved in forming the wells.

[00255] Fig. 31 shows a corresponding layout for the mask 3020 for a 4-sensors-per-well embodiment. Note that the alignment pattern 3016 is still used and that the individual well-masking circles 3014A in the array 2910 now have twice the diameter as the wells 3014 in Fig. 30, for accommodating four sensors per well instead of one sensor-per-well.

[00256] After exposure of the die/resist to the UV radiation, a second layer of resist may be coated on the surface of the chip. This layer of resist may be relatively thick, such as about 400 - 450 μm thick, typically. A second mask 3210 (Fig. 32), which also may be of chromium, is used to mask an area 3220 which surrounds the array, to build a collar or wall (or basin, using that term in the geological sense) 3310 of resist which surrounds the active array of sensors on substrate 3312, as shown in Fig. 33. In the particular example being described, the collar is 150 μm wider than the sensor array, on each side of the array, in the x direction, and 9 μm wider on each side than the sensor array, in the y direction. Alignment marks on mask 3210 (most not shown) are matched up with the alignment marks on the first layer and the CMOS chip itself.

[00257] Other photolithographic approaches may be used for formation of the microwell array, of course, the foregoing being only one example.

[00258] For example, contact lithography of various resolutions and with various etchants and developers may be employed. Both organic and inorganic materials may be used for the layer(s) in which the microwells are formed. The layer(s) may be etched on a chip having a dielectric layer over the pixel structures in the sensor array, such as a passivation layer, or the layer(s) may be formed separately and then applied over the sensor array. The specific choice or processes will depend on factors such as array size, well size, the fabrication facility that is available, acceptable costs, and the like.

[00259] Among the various organic materials which may be used in some embodiments to form the microwell layer(s) are the above-mentioned SU-8 type of negative-acting photoresist, a conventional positive-acting photoresist and a positive-acting photodefineable polyimide. Each has its virtues and its drawbacks, well known to those familiar with the photolithographic art.

[00260] Naturally, in a production environment, modifications will be appropriate.

[00261] Contact lithography has its limitations and it may not be the production method of choice to produce the highest densities of wells – i.e., it may impose a higher than desired minimum pitch limit in the lateral directions. Other techniques, such as a deep UV step-and-repeat process, are capable of providing higher resolution lithography and can be used to produce small pitches and possibly smaller well diameters. Of course, for different desired specifications (e.g., numbers of sensors and wells per chip), different techniques

may prove optimal. And pragmatic factors, such as the fabrication processes available to a manufacturer, may motivate the use of a specific fabrication method. While novel methods are discussed, various aspects of the invention are limited to use of these novel methods.

[00262] Preferably the CMOS wafer with the ISFET array will be planarized after the final metallization process. A chemical mechanical dielectric planarization prior to the silicon nitride passivation is suitable. This will allow subsequent lithographic steps to be done on very flat surfaces which are free of back-end CMOS topography.

[00263] By utilizing deep-UV step-and-repeat lithography systems, it is possible to resolve small features with superior resolution, registration, and repeatability. However, the high resolution and large numerical aperture (NA) of these systems precludes their having a large depth of focus. As such, it may be necessary, when using such a fabrication system, to use thinner photodefinable spin-on layers (i.e., resists on the order of 1-2 μm rather than the thicker layers used in contact lithography) to pattern transfer and then etch microwell features to underlying layer or layers. For example, four 1 μm plasma-enhanced chemical vapor thin-film depositions (standard fab process) may be done sequentially to render a target microwell thickness of 4 μm. High resolution lithography can then be used to pattern the microwell features and conventional SiO2 etch chemistries can be used – one each for the bondpad areas and then the microwell areas – having selective etch stops; the etch stops then can be on aluminum bondpads and silicon nitride passivation (or the like), respectively. Alternatively, other suitable substitute pattern transfer and etch processes can be employed to render microwells of inorganic materials.

[00264] Another approach is to form the microwell structure in an organic material. For example, a dual-resist "soft-mask" process may be employed, whereby a thin high-resolution deep-UV resist is used on top of a thicker organic material (e.g., cured polyimide or opposite-acting resist). The top resist layer is patterned. The pattern can be transferred using an oxygen plasma reactive ion etch process. This process sequence is sometimes referred to as the "portable conformable mask" (PCM) technique. See B.J. Lin et al., "Practicing the Novolac deep-UV portable conformable masking technique", Journal of Vacuum Science and Technology 19, No. 4, 1313-1319 (1981); and A. Cooper et al, "Optimization of a photosensitive spin-on dielectric process for copper inductor coil and interconnect protection in RF SoC devices."

[00265] Alternatively a "drill-focusing" technique may be employed, whereby several sequential step-and-repeat exposures are done at different focal depths to compensate for the limited depth of focus (DOF) of high-resolution steppers when patterning thick resist layers. This technique depends on the stepper NA and DOF as well as the contrast properties of the resist material.

[00266] Another PCM technique may be adapted to these purposes, such as that shown in U.S. patent application publication no. 2006/0073422 by Edwards et al. This is a three-layer PCM process and it is illustrated in Fig. 33A. As shown there, basically six major steps are required to produce the microwell array and the result is quite similar to what contact lithography would yield.

[00267] In a first step, 3320, a layer of high contrast negative-acting photoresist such as type Shipley InterVia Photodielectric Material 8021 (IV8021) 3322 is spun on the surface of a wafer, which we shall assume to be the wafer providing the substrate 3312 of Fig. 33 (in which the sensor array is fabricated), and a soft bake operation is performed. Next, in step 3324, a blocking anti-reflective coating (BARC) layer 3326, is applied and soft baked. On top of this structure, a thin resist layer 3328 is spun on and soft baked, step 3330, the thin layer of resist being suitable for fine feature definition. The resist layer 3328 is then patterned, exposed and developed, and the BARC in the exposed regions 3329, not protected any longer by the resist 3328, is removed, Step 3332. This opens up regions 3329 down to the uncured IV8021 layer. The BARC layer can now act like a conformal contact mask A blanket exposure with a flooding exposure tool, Step 3334, cross-links the exposed IV8021, which is now shown as distinct from the uncured IV8021 at 3322. One or more developer steps 3338 are then performed, removing everything but the cross-linked IV8021 in regions 3336. Regions 3336 now constitute the walls of the microwells.

[00268] Although as shown above, the wells bottom out (i.e. terminate) on the top passivation layer of the ISFETs, it is believed that an improvement in ISFET sensor performance (i.e. such as signal-to-noise ratio) can be obtained if the active bead(s) is(are) kept slightly elevated from the ISFET passivation layer. One way to do so is to place a spacer "bump " within the boundary of the pixel microwell. An example of how this could be rendered would be not etching away a portion of the layer-or-layers used to form the microwell structure (i.e. two lithographic steps to form the microwells – one to etch part

way done, the other to pattern the bump and finish the etch to bottom out), by depositing and lithographically defining and etching a separate layer to form the "bump", or by using a permanent photo-definable material for the bump once the microwells are complete. The bump feature is shown as 3350 in Fig. 33B. An alternative (or additional) non-integrated approach is to load the wells with a layer or two of very small packing beads before loading the DNA-bearing beads.

[00269] Mounting the coated chip to a flow cell (fluidic interface)

[00270] The process of using the assembly of an array of sensors on a chip combined with an array of microwells to sequence the DNA in a sample is referred to as an "experiment." Executing an experiment requires loading the wells with the DNA-bound beads and the flowing of several different solutions (i.e., reagents and washes) across the wells. A fluid delivery system coupled with a fluidic interface is needed which flows the various solutions across the wells in a controlled laminar flow with acceptably small dead volumes and small cross contamination between sequential solutions. The fluidic interface is sometimes referred to as a "flow cell."

[00271] Flow cell designs of many configurations are possible; the system and methods presented herein are not dependent on use of a specific flow cell configuration. It is desirable, though, that a suitable flow cell substantially conform to the following set of objectives:

- suitable interconnections with a fluidics delivery system – e.g., via appropriately-sized tubing;
- appropriate (for dna sequencing, approximately 300 μm) head space above wells ;
- minimization of dead volumes encountered by fluids prior to their entry to the flow chamber (i.e., the enclosed space above the microwell array).
- elimination of small spaces in contact with liquid but not swept by through the flow cell (to minimize cross contamination).
- uniform expansion of flow from the inlet tubing to a broad/flat front at the entry to the flow chamber.

- laminar flow characteristics such that the broad/flat front profile is maintained as it traverses across the chip from inlet side to outlet side.
- adaptable to placement of a removable reference electrode inside or as close to the flow chamber as possible.
- easy loading of beads.
- manufacturable at acceptable cost
- easy assembly of flow cell and attachment to the chip package.

[00272] Each of several example designs will be discussed, meeting these criteria. In each instance, one typically may choose to implement the design in one of two ways: either by attaching the flow cell to a frame and gluing the frame (or otherwise attaching it) to the chip or by integrating the frame into the flow cell structure and attaching this unified assembly to the chip. Further, designs may be categorized by the way the reference electrode is integrated into the arrangement. Depending on the design, the reference electrode may be integrated into the flow cell (e.g., form part of the ceiling of the flow chamber) or be in the flow path (typically to the outlet or downstream side of the flow path, after the sensor array).

[00273] A first example of a suitable experiment apparatus 3410 incorporating such a fluidic interface is shown in Figs. 34 - 37, the manufacture and construction of which will be discussed in greater detail below.

[00274] The apparatus comprises a semiconductor chip 3412 (indicated generally, though hidden) on or in which the arrays of wells and sensors are formed, and a fluidics assembly 3414 on top of the chip and delivering the sample to the chip for reading. The fluidics assembly includes a portion 3416 for introducing fluid containing the sample, a portion 3418 for allowing the fluid to be piped out, and a flow chamber portion 3420 for allowing the fluid to flow from inlet to outlet and along the way interact with the material in the wells. Those three portions are unified by an interface comprising a glass slide 3422 (e.g., Erie Microarray Cat #C22-5128-M20 from Erie Scientific Company, Portsmouth, NH, cut in thirds of size about 25mm x 25mm).

[00275] Mounted on the top face of the glass slide are two fittings, 3424 and 3426, such as nanoport fittings Part # N-333 from Upchurch Scientific of Oak Harbor, WA. One port

(e.g., 3424) serves as an inlet delivering liquids from the pumping/valving system described below but not shown here. The second port (e.g., 3426) is the outlet which pipes the liquids to waste. Each port connects to a conduit 3428, 3432 such as flexible tubing of appropriate inner diameter. The nanoports are mounted such that the tubing can penetrate corresponding holes in the glass slide. The tube apertures should be flush with the bottom surface of the slide.

[00276] On the bottom of the glass slide, flow chamber 3420 may comprise various structures for promoting a substantially laminar flow across the microwell array. For example, a series of microfluidic channels fanning out from the inlet pipe to the edge of the flow chamber may be patterned by contact lithography using positive photoresists such as SU-8 photoresist from MicroChem Corp. of Newton, MA. Other structures will be discussed below.

[00277] The chip 3412 will in turn be mounted to a carrier 3430, for packaging and connection to connector pins 3432.

[00278] For ease of description, to discuss fabrication starting with Fig. 38 we shall now consider the glass slide 3422 to be turned upside down relative to the orientation it has in Figs. 34-37.

[00279] A layer of photoresist 3810 is applied to the "top" of the slide (which will become the "bottom" side when the slide and its additional layers is turned over and mounted to the sensor assembly of ISFET array with microwell array on it). Layer 3810 may be about 150 μm thick in this example, and it will form the primary fluid carrying layer from the end of the tubing in the nanoports to the edge of the sensor array chip. Layer 3810 is patterned using a mask such as the mask 3910 of Fig. 39 ("patterned' meaning that a radiation source is used to expose the resist through the mask and then the non-plasticized resist is removed). The mask 3910 has radiation-transparent regions which are shown as white and radiation-blocking regions 3920, which are shown in shading. The radiation-blocking regions are at 3922-3928. The region 3926 will form a channel around the sensor assembly; it is formed about .5mm inside the outer boundary of the mask 3920, to avoid the edge bead that is typical. The regions 3922 and 3924 will block radiation so that corresponding portions of the resist are removed to form voids shaped as shown. Each of regions 3922, 3924 has a rounded end dimensioned to receive an end of a corresponding

one of the tubes 3428, 3432 passing through a corresponding nanoport 3424, 3426. From the rounded end, the regions 3922, 3924 fan out in the direction of the sensor array to allow the liquid to spread so that the flow across the array will be substantially laminar. The region 3928 is simply an alignment pattern and may be any suitable alignment pattern or be replaced by a suitable substitute alignment mechanism. Dashed lines on Fig. 38 have been provided to illustrate the formation of the voids 3822 and 3824 under mask regions 3922 and 3924.

[00280] A second layer of photoresist is formed quite separately, not on the resist 3810 or slide 3422. Preferably it is formed on a flat, flexible surface (not shown), to create a peel-off, patterned plastic layer. This second layer of photoresist may be formed using a mask such as mask 4010, which will leave on the flexible substrate, after patterning, the border under region 4012, two slits under regions 4014, 4016, whose use will be discussed below, and alignment marks produced by patterned regions 4018 and 4022. The second layer of photoresist is then applied to the first layer of photoresist using one alignment mark or set of alignment marks, let's say produced by pattern 4018, for alignment of these layers. Then the second layer is peeled from its flexible substrate and the latter is removed.

[00281] The other alignment mark or set of marks produced by pattern 4022 is used for alignment with a subsequent layer to be discussed.

[00282] The second layer is preferably about 150 μm deep and it will cover the fluid-carrying channel with the exception of a slit about 150 μm long at each respective edge of the sensor array chip, under slit-forming regions 4014 and 4016.

[00283] Once the second layer of photoresist is disposed on the first layer, a third patterned layer of photoresist is formed over the second layer, using a mask such as mask 4110, shown in Fig. 41. The third layer provides a baffle member under region 4112 which is as wide as the collar 3310 on the sensor chip array (see Fig. 33) but about 300 μm narrower to allow overlap with the fluid-carrying channel of the first layer. The third layer may be about 150 μm thick and will penetrate the chip collar 3310, toward the floor of the basin formed thereby, by 150 μm. This configuration will leave a headspace of about 300 μm above the wells on the sensor array chip. The liquids are flowed across the wells along the entire width of the sensor array through the 150 μm slits under 4014, 4016.

[00284] Fig. 36 shows a partial sectional view, in perspective, of the above-described example embodiment of a microfluidics and sensor assembly, also depicted in Figs. 34 and 35, enlarged to make more visible the fluid flow path. (A further enlarged schematic of half of the flow path is shown in Fig. 37.) Here, it will be seen that fluid enters via the inlet pipe 3428 in inlet port 3424. At the bottom of pipe 3428, the fluid flows through the flow expansion chamber 3610 formed by mask area 3922, that the fluid flows over the collar 3310 and then down into the bottom 3320 of the basin, and across the die 3412 with its microwell array. After passing over the array, the fluid then takes a vertical turn at the far wall of the collar 3310 and flows over the top of the collar to and across the flow concentration chamber 3612 formed by mask area 3924, exiting via outlet pipe 3432 in outlet port 3426. Part of this flow, from the middle of the array to the outlet, may be seen also in the enlarged diagrammatic illustration of Fig. 37, wherein the arrows indicate the flow of the fluid.

[00285] The fluidics assembly may be secured to the sensor array chip assembly by applying an adhesive to parts of mating surfaces of those two assemblies, and pressing them together, in alignment.

[00286] Though not illustrated in Figs. 34-36, the reference electrode may be understood to be a metallization 3710, as shown in Fig. 37, at the ceiling of the flow chamber.

[00287] Another way to introduce the reference electrode is shown in Fig. 42. There, a hole 4210 is provided in the ceiling of the flow chamber and a grommet 4212 (e.g., of silicone) is fitted into that hole, providing a central passage or bore through which a reference electrode 4220 may be inserted. Baffles or other microfeatures (not shown) may be patterned into the flow channel to promote laminar flow over the microwell array.

[00288] Figs. 43 - 44 show another alternative flow cell design, 4310. This design relies on the molding of a single plastic piece or member 4320 to be attached to the chip to complete the flow cell. The connection to the fluidic system is made via threaded connections tapped into appropriate holes in the plastic piece at 4330 and 4340. Or, if the member 4320 is made of a material such as polydimethylsiloxane (PDMS), the connections may be made by simply inserting the tubing into an appropriately sized hole in the member 4320. A vertical cross section of this design is shown in Figs. 43-44. This design may use an overhanging plastic collar 4350 (which may be a solid wall as shown or a series of

depending, spaced apart legs forming a downwardly extending fence-like wall) to enclose the chip package and align the plastic piece with the chip package, or other suitable structure, and thereby to alignment the chip frame with the flow cell forming member 4320. Liquid is directed into the flow cell via one of apertures 4330, 4340, thence downwardly towards the flow chamber.

[00289] In the illustrated embodiment, the reference electrode is introduced to the top of the flow chamber via a bore 4325 in the member 4320. The placement of the removable reference electrode is facilitated by a silicone sleeve 4360 and an epoxy stop ring 4370 (see the blow-up of Fig. 44). The silicone sleeve provides a tight seal and the epoxy stop ring prevent the electrode from being inserted too far into the flow cell. Of course, other mechanisms may be employed for the same purposes, and it may not be necessary to employ structure to stop the electrode. And if a material such as PDMS is used for member 4320, the material itself may form a watertight seal when the electrode is inserted, obviating need for the silicone sleeve.

[00290] Figs. 45 and 46 show a similar arrangement except that member 4510 lacks a bore for receiving a reference electrode. Instead, the reference electrode 4515 is formed on or affixed to the bottom of central portion 4520 and forms at least part of the flow chamber ceiling. For example, a metallization layer may be applied onto the bottom of central portion 4520 before member 4510 is mounted onto the chip package.

[00291] Figs. 47-48 show another example, which is a variant of the embodiment shown in Figs. 43-44, but wherein the frame is manufactured as part of the flow cell rather attaching a flow port structure to a frame previously attached to the chip surface. In designs of this type, assembly is somewhat more delicate since the wirebonds to the chip are not protected by the epoxy encapsulating the chip. The success of this design is dependent on the accurate placement and secure gluing of the integrated "frame" to the surface of the chip. A counterpart embodiment to that of Figs. 45-46, with the reference electrode 4910 on the ceiling of the flow chamber, and with the frame manufactured as part of the flow cell, is shown in Figs. 49-50.

[00292] Yet another alternative for a fluidics assembly, as shown in Figs. 51-52, has a fluidics member 5110 raised by about 5.5 mm on stand-offs 5120 from the top of the chip package 5130. This allows for an operator to visually inspect the quality of the bonding

between plastic piece 5140 and chip surface and reinforce the bonding externally if necessary.

[00293] Some of the foregoing alternative embodiments also may be implemented in a hybrid plastic/PDMS configuration. For example, as shown in Figs. 53-54, a plastic part 5310 may make up the frame and flow chamber, resting on a PDMS "base" portion 5320. The plastic part 5310 may also provides a region 5330 to the array, for expansion of the fluid flow from the inlet port; and the PDMS part may then include communicating slits 5410, 5412 through which liquids are passed from the PDMS part to and from the flow chamber below.

[00294] The fluidic structure may also be made from glass as discussed above, such as photo-definable (PD) glass. Such a glass may have an enhanced etch rate in hydrofluoric acid once selectively exposed to UV light and features may thereby be micromachined on the top-side and back-side, which when glued together can form a three-dimensional low aspect ratio fluidic cell.

[00295] An example is shown in Fig. 55. A first glass layer or sheet 5510 has been patterned and etched to create nanoport fluidic holes 5522 and 5524 on the top-side and fluid expansion channels 5526 and 5528 on the back-side. A second glass layer or sheet 5530 has been patterned and etched to provide downward fluid input/output channels 5532 and 5534, of about 300μm height (the thickness of the layer). The bottom surface of layer 5530 is thinned to the outside of channels 5532 and 5534, to allow the layer 5530 to rest on the chip frame and protrusion area 5542 to be at an appropriate height to form the top of the flow channel. Two glass layers, or wafers, and four lithography steps required. Both wafers should be aligned and bonded (e.g., with an appropriate glue, not shown) such that the downward fluid input/output ports are aligned properly with the fluid expansion channels. Alignment targets may be etched into the glass to facilitate the alignment process.

[00296] Nanoports may be secured over the nanoport fluidic holes to facilitate connection of input and output tubing.

[00297] A central bore 5550 may be etched through the glass layers for receiving a reference electrode, 5560. The electrode may be secured and sealed in place with a silicone collar 5570 or like structure; or the electrode may be equipped integrally with a suitable washer for effecting the same purpose.

[00298] By using glass materials for the two-layer fluidic cell, the reference electrode may also be a conductive layer or pattern deposited on the bottom surface of the second glass layer (not shown). Or, as shown in Fig. 56, the protrusion region may be etched to form a permeable glass membrane 5610 on the top of which is coated a silver (or other material) thin-film 5620 to form an integrated reference electrode. A hole 5630 may be etched into the upper layer for accessing the electrode and if that hole is large enough, it can also serve as a reservoir for a silver chloride solution. Electrical connection to the thin-film silver electrode may be made in any suitable way, such as by using a clip-on pushpin connector or alternatively wirebonded to the ceramic ISFET package.

[00299] Still another example embodiment for a fluidic assembly is shown in Figs. 57-58. This design is limited to a plastic piece 5710 which incorporates the frame and is attached directly to the chip surface, and to a second piece 5720 which is used to connect tubing from the fluidic system and similarly to the PDMS piece discussed above, distributes the liquids from the small bore tube to a wide flat slit. The two pieces are glued together and multiple (e.g., three) alignment markers (not shown) may be used to precisely align the two pieces during the gluing process. A hole may be provided in the bottom plate and the hole used to fill the cavity with an epoxy (for example) to protect the wirebonds to the chip and to fill in any potential gaps in the frame/chip contact. In the illustrated example, the reference electrode is external to the flow cell (downstream in the exhaust stream, through the outlet port – see below), though other configurations of reference electrode may, of course, be used.

[00300] Still further examples of flow cell structures are shown in Figs. 59-60. Fig. 59A comprises eight views (A-H) of an injection molded bottom layer, or plate, 5910, for a flow cell fluidics interface, while Fig. 59B comprises seven views (A-G) of a mating, injection molded top plate, or layer, 5950. The bottom of plate 5910 has a downwardly depending rim 5912 configured and arranged to enclose the sensor chip and an upwardly extending rim 5914 for mating with the top plate 5610 along its outer edge. To form two fluid chambers (an inlet chamber and an outlet chamber) between them. A stepped, downwardly depending portion 5960 of top plate 5950, separates the input chamber from the output chamber. An inlet tube 5970 and an outlet tube 5980 are integrally molded with the rest of top plate 5950. From inlet tube 5970, which empties at the small end of the inlet chamber formed by a

depression 5920 in the top of plate 5910, to the outlet edge of inlet chamber fans out to direct fluid across the whole array.

[00301] Whether glass or plastic or other material is used to form the flow cell, it may be desirable, especially with larger arrays, to include in the inlet chamber of the flow cell, between the inlet conduit and the front edge of the array, not just a gradually expanding (fanning out) space, but also some structure to facilitate the flow across the array being suitably laminar. Using the bottom layer 5990 of an injection molded flow cell as an example, one example type of structure for this purpose, shown in Fig. 59C, is a tree structure 5992 of channels from the inlet location of the flow cell to the front edge of the microwell array or sensor array, which should be understood to be under the outlet side of the structure, at 5994.

[00302] There are various other ways of providing a fluidics assembly for delivering an appropriate fluid flow across the microwell and sensor array assembly, and the forgoing examples are thus not intended to be exhaustive.

[00303] Reference Electrode

[00304] Commercial flow-type fluidic electrodes, such as silver chloride proton-permeable electrodes, may be inserted in series in a fluidic line and are generally designed to provide a stable electrical potential along the fluidic line for various electrochemical purposes. In the above-discussed system, however, such a potential must be maintained at the fluidic volume in contact with the microwell ISFET chip. With conventional silver chloride electrodes, it has been found difficult, due to an electrically long fluidic path between the chip surface and the electrode (through small channels in the flow cell), to achieve a stable potential. This led to reception of noise in the chip's electronics. Additionally, the large volume within the flow cavity of the electrode tended to trap and accumulate gas bubbles that degraded the electrical connection to the fluid. With reference to Fig. 60, a solution to this problem has been found in the use of a stainless steel capillary tube electrode 6010, directly connected to the chip's flow cell outlet port 6020 and connected to a voltage source (not shown) through a shielded cable 6030. The metal capillary tube 6010 has a small inner diameter (e.g., on the order of 0.01") that does not trap gas to any appreciable degree and effectively transports fluid and gas like other microfluidic tubing. Also, because the capillary tube can be directly inserted into the flow cell port 6020,

it close to the chip surface, reducing possible electrical losses through the fluid. The large inner surface area of the capillary tube (typically about 2" long) may also contribute to its high performance. The stainless steel construction is highly chemically resistant, and should not be subject to electrochemical effects due to the very low electrical current use in the system (< 1μA). A fluidic fitting 6040 is attached to the end of the capillary that is not in the flow cell port, for connection to tubing to the fluid delivery and removal subsystem.

[00305] Fluidics System

[00306] A complete system for using the sensor array will include suitable fluid sources, valving and a controller for operating the valving to low reagents and washes over the microarray or sensor array, depending on the application. These elements are readily assembled from off-the-shelf components, with and the controller may readily be programmed to perform a desired experiment.

[00307] As already discussed, the apparatus and systems of the invention can be used to detect and/or monitor interactions between various entities. These interactions include chemical or enzymatic reactions in which substrates and/or reagents are consumed and/or reaction byproducts are generated. An example of an enzymatic reaction that can be monitored according to the invention is nucleic acid sequencing, which will be discussed in greater detail herein. In the context of a sequencing reaction, the apparatus and system provided herein is able to detect nucleotide incorporation based on changes in the chemFET current. Current changes may be the result of one or more of the following events either singly or some combination thereof: generation of PPi, generation of Pi (e.g., in the presence of pyrophosphatase), generation of hydrogen (and concomitant changes in pH for example in the presence of low strength buffer), reduced concentration of unincorporated dNTP at the chemFET surface, delayed arrival of dNTP at the chemFET surface, and the like. It is to be understood that the methods provided herein are not dependent upon the mechanism by which the current change is effected. And accordingly, the invention contemplates sequencing of nucleic acids based on changes in the chemFET current. The methods provided herein in regards to sequencing can be contrasted to those in the literature including Pourmand et al. PNAS 2006 103(17):6466-6470.

[00308] Fig. 61 illustrates the production of PPi resulting from the incorporation of a nucleotide in a newly synthesized nucleic acid strand. PPi generated as a reaction

byproduct of nucleotide incorporation in a nucleic acid strand can be detected directly even in the absence of a PPi receptor (such as those provided in Fig. 11B) and in the absence of a detectable pH change (e.g., as may occur in the presence of a strong buffer, as defined herein). The simple presence of PPi is sufficient, in some instances, to cause an electrical change in the chemFET surface, thereby resulting in a current change. The current change may result from PPi generation alone or in combination with other events such as those described above.

[00309] Thus, in one aspect, the invention contemplates sequencing nucleic acids using a chemFET array such as an ISFET array. The method of the invention is a "sequencing by synthesis" method since it requires synthesis of a new nucleic acid strand that is complementary to the strand being sequenced.

[00310] The release of PPi following incorporation of a nucleotide in a newly synthesized nucleic acid strand is shown in Fig. 61. The incorporation of a dNTP into the nucleic acid strand releases PPi which can then be hydrolyzed to two orthophosphates (Pi) and one hydrogen ion. The generation of the hydrogen ion therefore can facilitate detection of nucleotide incorporation on the basis of pH change. Alternatively, as discussed herein, PPi generation (as detected in the absence or presence of PPi receptors) can facilitate detection of nucleotide incorporation on the basis of pH change. And in still another embodiment, PPi may be converted to Pi using pyrophosphatase and Pi may be detected directly or indirectly. Any and all of these events (and more as described herein) may be involved in causing a current change in the chemFET that correlates with nucleotide incorporation.

[00311] The sequencing reactions aim to maximize complete incorporation across all wells for any given dNTP, reduce or decrease the number of unincorporated dNTPs that remain in the wells, and achieve as a high a signal to noise ratio as possible.

[00312] The nucleic acid being sequenced is referred to herein as the target nucleic acid. Target nucleic acids include but are not limited to DNA such as but not limited to genomic DNA, mitochondrial DNA, cDNA and the like, and RNA such as but not limited to mRNA, miRNA, and the like. The nucleic acid may be from any source including naturally occurring sources or synthetic sources. The nucleic acids may be PCR products, cosmids, plasmids, naturally occurring or synthetic libraries, and the like. The invention is not intended to be limited in this regard. The methods provided herein can be used to sequence

nucleic acids of any length. To be clear, the Examples provide a proof of principle demonstration of the sequencing of four templates of known sequence. This artificial model is intended to show that the apparatus and system are able to readout nucleotide incorporation that correlates to the known sequence of the templates. This is not intended to represent typical use of the method or system in the field. The following is a brief description of these methods.

[00313] Target nucleic acids are prepared using any manner known in the art. As an example, genomic DNA may be harvested from a sample according to techniques known in the art (see for example Sambrook et al. "Maniatis"). Following harvest, the DNA may be fragmented to yield nucleic acids of smaller length. The resulting fragments may be on the order of hundreds, thousands, or tens of thousands nucleotides in length. In some embodiments, the fragments are 200-1000 base pairs in size, or 300-800 base pairs in size, although they are not so limited. Nucleic acids may be fragmented by any means including but not limited to mechanical, enzymatic or chemical means. Examples include shearing, sonication, nebulization and endonuclease (e.g., Dnase I) digestion, or any other technique known in the art to produce nucleic acid fragments, preferably of a desired length. Fragmentation can be followed by size selection techniques can be used enrich or isolate fragments of a particular length or size. Such techniques are also known in the art and include but are not limited to gel electrophoresis or SPRI.

[00314] In some embodiments, the size selected target nucleic acids are ligated to adaptor sequences on both the 5' and 3' ends. These adaptor sequences comprise amplification primer sequences to be used in amplifying the target nucleic acids. One adaptor sequence may also comprise a sequence complementary to the sequencing primer. The opposite adaptor sequence may comprise a moiety that facilitates binding of the nucleic acid to a solid support such as but not limited to a bead. An example of such a moiety is a biotin molecule (or a double biotin moiety, as described by Diehl et al. Nature Methods, 2006, 3(7):551-559) and such a labeled nucleic acid can therefore be bound to a solid support having avidin or streptavidin groups. The resulting nucleic acid is referred to herein as a template nucleic acid. The template nucleic acid comprises at least the target nucleic acid and usually comprises nucleotide sequences in addition to the target.

[00315] In some instances a spacer is used to distance the template nucleic acid (and in particular the target nucleic acid sequence comprised therein) from the bead. This facilitates sequencing of the end of the target closest to the bead. Examples of suitable linkers are known in the art (see Diehl et al. Nature Methods, 2006, 3(7):551-559) and include but are not limited to carbon-carbon linkers such as but not limited to iSp18.

[00316] The solid support to which the template nucleic acids are bound is referred to herein as the "capture solid support". If the solid support is a bead, then such bead is referred to herein as a "capture bead". The beads can be made of any material including but not limited to cellulose, cellulose derivatives, gelatin, acrylic resins, glass, silica gels, polyvinyl pyrrolidine (PVP), co-polymers of vinyl and acrylamide, polystyrene, polystyrene cross-linked with divinylbenzene or the like (see, Merrifield Biochemistry 1964, 3, 1385-1390), polyacrylamides, latex gels, dextran, crosslinked dextrans (e.g., Sephadex™), rubber, silicon, plastics, nitrocellulose, natural sponges, metal, and agarose gel (Sepharose™). In one embodiment, the beads are streptavidin-coated beads. The bead diameter will depend on the density of the ISFET and well array used with larger arrays (and thus smaller sized wells) requiring smaller beads. Generally the bead size may be about 1-10 μM, and more preferably 2-6 μM. In some embodiments, the beads are about 5.91 μM while in other embodiments the beads are about 2.8 μM. It is to be understood that the beads may or may not be perfectly spherical in shape. It is to be understood that other beads may be used and other mechanisms for attaching the nucleic acid to the beads may be utilized.

[00317] As discussed herein, the sequencing reactions are carried out in wells that are situated above the chemFETs. The wells (referred to herein interchangeably as reaction chambers or microwells) may vary in size between arrays. Preferably the width to height ratio of the well is 1:1 to 1:1.5. The bead to well size is preferably in the range of 0.6-0.8.

[00318] A homogeneous population of amplified nucleic acids are conjugated to one or more beads with the proviso that each bead will ultimately be bound to a plurality of identical nucleic acid sequences. The degree of loading of nucleic acid templates onto beads will depend on a number of factors including the bead size and the length of the nucleic acid. In most aspects, maximal loading of the beads is desired. Amplification and conjugation of nucleic acids to solid support such as beads may be accomplished in a

number of ways, including but not limited to emulsion PCR as described by Margulies et al. Nature 2005 437(15):376-380 and accompanying supplemental materials. In some embodiments, the amplification is a representative amplification. A representative amplification is an amplification that does not alter the relative representation of any nucleic acid species.

[00319] Before and/or while in the wells of the flow chamber, the beads are incubated with a sequencing primer that binds to its complementary sequence located on the 3' end of the template nucleic acid (i.e., either in the amplification primer sequence or in another adaptor sequence ligated to the 3' end of the target nucleic acid) and with a polymerase for a time and under conditions that promote hybridization of the primer to its complementary sequence and that promote binding of the polymerase to the template nucleic acid. The primer can be of virtually any sequence provided it is long enough to be unique. The hybridization conditions are such that the primer will hybridize to only its true complement on the 3' end of the template. Suitable conditions are disclosed in Margulies et al. Nature 2005 437(15):376-380 and accompanying supplemental materials.

[00320] Suitable polymerases include but are not limited to DNA polymerase, RNA polymerase, or a subunit thereof, provided it is capable of synthesizing a new nucleic acid strand based on the template and starting from the hybridized primer. An example of a suitable polymerase subunit is the exo-version of the Klenow fragment of E. coli DNA polymerase I which lacks 3' to 5' exonuclease activity. The enzyme is therefore bound to the bead (or corresponding solid support) but not to the ISFET surface itself. The template nucleic acid is also contacted with other reagents and/or cofactors including but not limited to buffer, detergent, reducing agents such as dithiothrietol (DTT, Cleland's reagent), single stranded binding proteins, and the like before and/or while in the well. In one embodiment, the template nucleic acid is contacted with the primer and the polymerase prior to its introduction into the flow chamber and wells thereof.

[00321] The nucleic acid loaded beads are introduced into the flow chamber and ultimately the wells situated above the ISFET array. The method requires that each well in the flow chamber contain only one nucleic acid loaded bead since the presence of two beads per well will yield one unusable sequencing information derived from two different nucleic acids. The Examples provides a brief description of an exemplary bead loading protocol in

the context of magnetic beads. It is to be understood that a similar approach could be used to load other bead types. The protocol has been demonstrated to reduce the likelihood and incidence of trapped air in the wells of the flow chamber, uniformly distribute nucleic acid loaded beads in the totality of wells of the flow chamber, and avoid the presence and/or accumulation of excess beads in the flow chamber.

[00322] The percentage of occupied wells on the chip may vary depending on the methods being performed. If the method is aimed at extracting maximum sequence data in the shortest time possible, then higher occupancy is desirable. If speed and throughout is not as critical, then lower occupancy may be tolerated. Therefore depending on the embodiment, suitable occupancy percentages may be at least 10%, at least 20%, at least 30%, at least 40%, at least 50%, at least 60%, at least 70%, at least 80%, at least 90%, or 100% of the wells. As used herein, occupancy refers to the presence of one nucleic acid loaded bead in a well and the percentage occupancy refers to the proportion of total wells on a chip that are occupied by a single bead. Wells that are occupied by more than one bead cannot be used in the analyses contemplated by the invention.

[00323] Ultimately a homogeneous population of template nucleic acids is placed into one or more of a plurality of wells, each well situated over and thus corresponding to at least one ISFET. As discussed above, preferably the well contains at least 10, at least 100, at least 1000, at least 10^4, at least 10^5, at least 10^6, or more copies of an identical template nucleic acid. Identical template nucleic acids means at a minimum that the templates are identical in sequence. Most and preferably all the template nucleic acids within a well are uniformly hybridized to a primer. Uniform hybridization of the template nucleic acids to the primers means that the primer hybridizes to the template at the same location (i.e., the sequence along the template that is complementary to the primer) as every other primer-template hybrid in the well. The uniform positioning of the primer on every template allows the co-ordinated synthesis of all new nucleic acid strands within a well, thereby resulting in a greater signal-to-noise ratio.

[00324] Nucleotides are then added in flow, or by any other suitable method, in sequential order to the flow chamber and thus the wells. The nucleotides can be added in any order provided it is known and for the sake of simplicity kept constant throughout a run. If the incorporation of nucleotides is based on detection of PPi rather than detection of pH change

as a result of PPi release, then it is preferable to maintain a relatively constant level and concentration of nucleotides throughout the reactions and washes. One way of accomplishing this is to add ATP to the wash buffer such that dNTPs flowing into a well are displacing ATP from the well. The ATP matches the ionic strength of the dNTPs entering the wells and it also has a similar diffusion profile as those dNTPs. In this way, influx and efflux of dNTPs during the sequencing reaction do not interfere with measurements at the chemFET. The concentration of ATP used is on the order of the concentration of dNTP used.

[00325] A typical sequencing cycle proceeds as follows: washing of the flow chamber (and wells) with wash buffer containing ATP, introduction of a first dNTP species (e.g., dATP) into the flow chamber (and wells), release and detection of PPi (by any of the mechanisms described herein), washing of the flow chamber (and wells) with wash buffer containing ATP, washing of the flow chamber (and wells) with wash buffer containing apyrase, washing of the flow chamber (and wells) with wash buffer containing ATP, and introduction of a second dNTP species. This process is continued until all 4 dNTP (i.e., dATP, dCTP, dGTP and dTTP) have been flowed through the chamber and allowed to incorporate into the newly synthesized strands. This 4-nucleotide cycle may be repeated any number of times including but not limited to 10, 25, 50, 100, 200 or more times. The number of cycles will be governed by the length of the template being sequenced and the need to replenish reaction reagents, in particular the dNTP stocks and wash buffers.

[00326] As part of the sequencing reaction, a dNTP will be ligated to (or "incorporated into" as used herein) the 3' of the newly synthesized strand (or the 3' end of the sequencing primer in the case of the first incorporated dNTP) if its complementary nucleotide is present at that same location on the template nucleic acid. Incorporation of the introduced dNTP (and concomitant release of PPi) therefore indicates the identity of the corresponding nucleotide in the template nucleic acid. If no change in the electric field is detected by the ISFET, then the dNTP has not been incorporated and one can conclude that the complementary nucleotide was not present in the template at that location. If a change in the electric field is detected, then the introduced dNTP has been incorporated into the newly synthesized strand. There is a positive correlation between dNTP incorporation and PPi release and the response of the ISFET, and as a result it is further possible to quantitate the number of dNTP incorporated. In other words, the voltage change registered at the ISFET

is related to the number of dNTP incorporated. The result is that no sequence information is lost through the sequencing of a homopolymer stretch (e.g., poly A, poly T, poly C, or poly G) in the template. As an example, if the template nucleic acid includes a sequence of 5' CAAAAG 3', the ISFET will register a signal (e.g., in terms of millivolt change) upon introduction of dCTP, and then it will register a signal of greater magnitude upon the introduction of dTTP, followed by another signal upon the introduction of dGTP. The magnitude of the signals arising upon introduction of dCTP and dTTP will be essentially equivalent and will correlate with the millivoltage change resulting from a single nucleotide incorporation. The magnitude of the signal arising upon introduction of dTTP will be greater than the signals arising from single dNTP incorporation. The magnitude of these signals may be additive, and depending on the length of the homopolymer stretch may not be readily apparent in a voltage versus time (or frame) plot (such as those shown in Fig. 71A-D, right panels). Signals may be measured using peak intensity or area under the curve from a voltage versus time (or frame) plot.

[00327] Apyrase is an enzyme that degrades residual unincorporated nucleotides converting them into monophosphate and releasing inorganic phosphate in the process. It is useful for degrading dNTPs that are not incorporated and/or that are in excess in any and all wells. It is important that excess and/or unreacted dNTP be washed away from any and all wells before introduction of the subsequent dNTP. Accordingly, addition of apyrase during the synthesis reaction and between the introduction of different dNTPs is useful to remove excess dNTPs that would otherwise obscure the sequencing data.

[00328] Additional sequencing reaction reagents such as those described above may be introduced throughout the reaction, although in some cases this may not be necessary. For example additional polymerase, DTT, SBB and the like may be added if necessary.

[00329] The invention therefore contemplates performing a plurality of different sequencing reactions simultaneously. A plurality of identical sequencing reactions is occurring in each occupied well simultaneously. It is this simultaneous and identical incorporation of dNTP within each well that increases the signal to noise ratio, thereby making detection of the sequencing reaction byproduct possible. By performing sequencing reactions in a plurality of wells simultaneously, a plurality of different sequencing reactions are also performed simultaneously.

[00330] The sequencing reaction can be run at a range of temperatures. Typically, the reaction is run in the range of 30-60°C, 35-55°C, or 40-45°C. It is preferable to run the reaction at temperatures that prevent formation of secondary structure in the nucleic acid. However this must be balanced with the binding of the primer (and the newly synthesized strand) to the template nucleic acid and the reduced half-life of apyrase at higher temperatures. A suitable temperature is about 41°C. The solutions including the wash buffers and the dNTP solutions are generally warmed to these temperatures in order not to alter the temperature in the wells. The wash buffer containing apyrase however is preferably maintained at a lower temperature in order to extend the half-life of the enzyme. Typically, this solution is maintained at about 4-15°C, and more preferably 4-10°C.

[00331] The nucleotide incorporation reaction can occur very rapidly. As a result, it may be desirable in some instances to slow the reaction down in order to ensure maximal data capture during the reaction. The diffusion of reagents and/or byproducts can be slowed down in a number of ways including but not limited to addition of packing beads in the wells. The packing beads also tend to increase the concentration of reagents and/or byproducts at the chemFET surface, thereby increasing the potential for signal. The presence of packing beads generally allows a greater time to sample (e.g., by 2- or 4-fold).

[00332] Data capture rates can vary and be for example anywhere from 10-100 frames per second and the choice of which rate to use will be dictated at least in part by the well size and the presence of packing beads. Smaller well sizes generally require faster data capture rates.

[00333] In some aspects of the invention that are flow-based and where the top face of the well is open and in communication with fluid over the entirety of the chip, it is important to detect the released PPi or other byproduct (e.g., H^+) prior to diffusion out of the well. Diffusion of either reaction byproduct out of the well will lead to false negatives (because the byproduct is not detected in that well) and potential false positives in adjacent or downstream wells, and thus should be avoided. Packing beads may also help reduce the degree of diffusion and/or cross-talk between wells.

[00334] Thus in some embodiments packing beads are used in addition to the nucleic acid-loaded beads. The packing beads may be magnetic (including superparamagnetic) but they are not so limited. In some embodiments the packing beads and the capture beads are

made of the same material (e.g., both are magnetic, both are polystyrene, etc.), while in other embodiment they are made of different materials (e.g., the packing beads are polystyrene and the capture beads are magnetic). The packing beads are generally smaller than the capture beads. The difference in size may be vary and may be 5-fold, 10-fold, 15-fold, 20-fold or more. As an example, 0.35 μm diameter packing beads have been used with 5.91 μm capture beads. Such packing beads are commercially available from sources such as Bang Labs. The placement of the packing beads relative to the capture bead may vary. For example, the packing beads may surround the capture bead and thereby prevent the capture bead from contacting the ISFET surface. As another example, the packing beads may be loaded into the wells following the capture beads in which case the capture bead is in contact with the ISFET surface. The presence of packing beads between the capture bead and the ISFET surface slows the diffusion of the sequencing byproducts such as PPi, thereby facilitating data capture.

[00335] The invention further contemplates the use of packing beads or modifications to the chemFET surface (as described herein) to prevent contact and thus interference of the chemFET surface with the template nucleic acids bound to the capture beads. A layer of packing beads that is 0.1-0.5 μm in depth or height would preclude this interaction.

[00336] The sequencing reaction may be preceded by an analysis of the arrays to determine the location of beads. It has been found that in the absence of flow the background signal (i.e., noise) is less than or equal to about 0.25 mV, but that in the presence of DNA-loaded capture beads that signal increases to about 1.0 mV =/- 0.5 mV. This increase is sufficient to allow one to determine wells with beads.

[00337] The invention further contemplates kits comprising the various reagents necessary to perform a sequencing reaction and instructions of use according to the methods set forth herein.

[00338] One preferred kit comprises one or more containers housing wash buffer, one or more containers each containing one of the following reagents: dATP buffer, dCTP buffer, dGTP buffer or dTTP buffer, dATP, dCTP, dGTP and dTTP stocks, apyrase, SSB, polymerase, packing beads and optionally pyrophosphatase. Importantly the kits comprise only naturally occurring dNTPs.

[00339] It is to be understood that interactions between receptors and ligands or between two members of a binding pair or between components of a molecular complex can also be detected using the chemFET arrays. Examples of such interactions include hybridization of nucleic acids to each other, protein-nucleic acid binding, protein-protein binding, enzyme-substrate binding, enzyme-inhibitor binding, antigen-antibody binding, and the like. Any binding or hybridization event that causes a change of the semiconductor charge density at the FET interface and thus changes the current that flows from the source to the drain of the sensors described herein can be detected according to the invention.

[00340] In these embodiments, the passivation layer (or possibly an intermediate layer coated onto the passivation layer) is functionalized with nucleic acids (e.g., DNA, RNA, miRNA, cDNA, and the like), antigens (which can be of any nature), proteins (e.g., enzymes, cofactors, antibodies, antibody fragments, and the like), and the like. Conjugation of these entities to the passivation layer can be direct or indirect (e.g., using bifunctional linkers that bind to both the passivation layer reactive group and the entity to be bound).

[00341] As an example, reaction groups such as amine or thiol groups may be added to a nucleic acid at any nucleotide during synthesis to provide a point of attachment for a bifunctional linker. As another example, the nucleic acid may be synthesized by incorporating conjugation-competent reagents such as Uni-Link AminoModifier, 3'-DMT-C6-Amine-ON CPG, AminoModifier II, N-TFA-C6-AminoModifier, C6-ThiolModifier, C6-Disulfide Phosphoramidite and C6-Disulfide CPG (Clontech, Palo Alto, CA). Other methods for attaching nucleic acids are discussed below.

[00342] In one aspect of the invention, the chemFET arrays are provided in combination with nucleic acid arrays. Nucleic acids in the form of short nucleic acids (e.g., oligonucleotides) or longer nucleic acids (e.g., full length cDNAs) can be provided on chemFET surfaces of the arrays described herein. Nucleic acid arrays generally comprise a plurality of physically defined regions on a planar surface (e.g., "spots") each of which has conjugated to it one and more preferably more nucleic acids. The nucleic acids are usually single stranded. The nucleic acids conjugated to a given spot are usually identical. In the context of an oligonucleotide array, these nucleic acids may be on the order of less 100 nucleotides in length (including about 10, 20, 25, 30, 40, 50, 60, 70, 80, 90 or 100 nucleotides in length). If the arrays are used to detect certain genes (including mutations in

such genes or expression levels of such genes), then the array may include a number of spots each of which contains oligonucleotides that span a defined and potentially different sequence of the gene. These spots are then located across the planar surface in order to exclude position related effects in the hybridization and readout means of the array.

[00343] The arrays are contacted with a sample being tested. The sample may be a genomic DNA sample, a cDNA sample from a cell, a tissue or a mass (e.g., a tumor), a population of cells that are grown on the array, potentially in a two dimensional array that corresponds to the underlying sensor array, and the like. Such arrays are therefore useful for determining presence and/or level of a particular gene or of its expression, detecting mutations within particular genes (such as but not limited to deletions, additions, substitutions, including single nucleotide polymorphisms), and the like.

[00344] The binding or hybridization of the sample nucleic acids and the immobilized nucleic acids is generally performed under stringent hybridization conditions as that term is understood in the art. (See for example Sambrook et al. "Maniatis".) Examples of relevant conditions include (in order of increasing stringency): incubation temperatures of 25°C, 37°C, 50°C and 68°C; buffer concentrations of 10X SSC, 6X SSC, 4X SSC, 1X SSC, 0.1X SSC (where SSC is 0.15 M NaCl and 15 mM citrate buffer) and their equivalents using other buffer systems; formamide concentrations of 0%, 25%, 50%, and 75%; incubation times from 5 minutes to 24 hours; 1, 2, or more washing steps; wash incubation times of 1, 2, or 15 minutes; and wash solutions of 6X SSC, 1X SSC, 0.1 X SSC, or deionized water. By way of example hybridization may be performed at 50% formamide and 4X SSC followed by washes of 2X SSC/formamide at 50°C and with 1X SSC.

[00345] Nucleic acid arrays include those in which already formed nucleic acids such as cDNAs are deposited (or "spotted") on the array in a specific location. Nucleic acids can be spotted onto a surface by piezoelectrically deposition, UV crosslinking of nucleic acids to polymer layers such as but not limited to poly-L-lysine or polypyrrole, direct conjugation to silicon coated SiO_2 as described in published US patent application 2003/0186262, direct conjugation to a silanised chemFET surface (e.g., a surface treated with 3-aminopropyltriethoxysilane (APTES) as described by Uslu et al. Biosensors and Bioelectronics 2004, 19:1723-1731, for example.

[00346] Nucleic acid arrays also include those in which nucleic acids (such as oligonucleotides of known sequence) are synthesized directly on the array. Nucleic acids can be synthesized on arrays using art-recognized techniques such as but not limited to printing with fine-pointed pins onto glass slides, photolithography using pre-made masks, photolithography using dynamic micromirror devices (such as DLP mirrors), ink-jet printing, or electrochemistry on microelectrode arrays. Reference can also be made to Nuwaysir et al. 2002 "Gene expression analysis using oligonucleotide arrays produced by maskless photolithography.". *Genome Res* **12**: 1749-1755. Commercial sources of this latter type of array include Agilent, Affymetrix, and NimbleGen.

[00347] Thus the chemFET passivation layer may be coated with an intermediate layer of reactive molecules (and therefore reactive groups) to which the nucleic acids are bound and/or from which they are synthesized.

[00348] The invention contemplates combining such nucleic acid arrays with the chemFET arrays and particularly the "large scale" chemFET arrays described herein. The chemFET/nucleic acid array can be used in a variety of applications, some of which will not require the wells (or microwells or reaction chambers, as they are interchangeably referred to herein). Since analyses may still be carried out in flow, including in a "closed" system (i.e., where the flow of reagents and wash solutions and the like is automated), there will be one or more flow chambers situated above and in contact with the array. The use of multiple flow chambers allows multiple samples (or nucleic acid libraries) to be analyzed simultaneously. There may be 2, 3, 4, 5, 6, 7, 8, 9, 10 or more flow chambers. This configuration applies equally to other biological arrays including those discussed herein such as protein arrays, antibody arrays, enzyme arrays, chemical arrays, and the like.

[00349] Since the binding event between binding partners or between components of a complex is detected electronically via the underlying FET, such assays may be carried out without the need to manipulate (e.g., extrinsically label) the sample being assayed. This is advantageous since such manipulation invariably results in loss of sample and generally requires increased time and work up. In addition, the present method allows binding interactions to be studied in real time.

[00350] Protein arrays used in combination with the chemFET arrays of the invention are also contemplated. Protein arrays comprise proteins or peptides or other amino acid

comprising biological moiety bound to a planar surface in an organized and predetermined manner. Such proteins include but are not limited to enzymes, antibodies and antibody fragments or antibody mimics (e.g., single chain antibodies).

[00351] In one embodiment, a protein array may comprise a plurality of different proteins (or other amino acid containing biological moieties). Each protein, and preferably a plurality of proteins, is present in a predetermined region or "cell" of the array. The regions (or cells) are aligned with the sensors in the sensor array such that there is one sensor for each region (or cell). The plurality of proteins in a single region (or cell) may vary depending on the size of the protein and the size of the region (or cell) and may be but is not limited to at least 10, 50, 100, 500, 10^3, 10^4 or more. The array itself may have any number of cells, including but not limited to at least 10, 10^2, 10^3, 10^4, 10^5, 10^6, 10^7, or more. In one application, the array is exposed to a sample that is known to contain or is suspected of containing an analyte that binds to the protein. The analyte may be a substrate or an inhibitor if the protein is an enzyme. The analyte may be any molecule that binds to the protein including another protein, a nucleic acid, a chemical species (whether synthetic or naturally occurring), and the like.

[00352] It is to be understood that, like the nucleic acid arrays contemplated herein, the readout from the protein arrays will be a change in current through the chemFET and thus no additional step of labeling and/or label detection is required in these array methods.

[00353] In another embodiment, the protein array may comprise a plurality of identical proteins (or other amino acid containing biological moieties). The identical proteins may be uniformly distributed on a planar surface or they may be organized into discrete regions (or cells) on that surface. In these latter embodiments, the regions (or cells) are aligned with the sensors in the sensor array such that there is one sensor for each region (or cell).

[00354] The proteins may be synthesised off-chip, then purified and attached to the array. Alternatively they can be synthesised on-chip, similarly to the nucleic acids discussed above. Synthesis of proteins using cell-free DNA expression or chemical synthesis is amenable to on-chip synthesis. Using cell-free DNA expression, proteins are attached to the solid support once synthesized. Alternatively, proteins may be chemically synthesized on the solid support using solid phase peptide synthesis. Selective deprotection is carried out through lithographic methods or by SPOT-synthesis. Reference can be made to at least

MacBeath and Schreiber, Science, 2000, 289:1760-1763, or Jones et al. Nature, 2006, 439:168-174. Reference can also be made to US Patent 6919211 to Fodor et al.

[00355] Chemical compound microarrays in combination with chemFET arrays are also envisioned. Chemical compound microarrays can be made by covalently immobilizing the compounds (e.g., organic compounds) on the solid surface with diverse linking techniques (may be referred to in the literature as "small molecule microarray"), by spotting and drying compounds (e.g., organic compounds) on the solid surface without immobilization (may be referred to in the literature as "micro arrayed compound screening (μARCS)"), or by spotting organic compounds in a homogenous solution without immobilization and drying effect (commercialized as DiscoveryDot™ technology by Reaction Biology Corporation).

[00356] Tissue microarrays in combination with chemFET arrays are further contemplated by the invention. Tissue microarrays are discussed in greater detail in Battifora Lab Invest 1986, 55:244-248; Battifora and Mehta Lab Invest 1990, 63:722-724; and Kononen et al. Nat Med 1998, 4:844-847.

[00357] The configurations of the chemFET arrays and the biological or chemical arrays are similar in each instance and the discussion of one combination array will apply to others described herein or otherwise known in the art.

[00358] In yet another aspect, the invention contemplates analysis of cell cultures (e.g., two-dimensional cells cultures) (see for example Baumann et al. Sensors and Actuators B 55 1999 77:89), and tissue sections placed in contact with the chemFET array. As an example, a brain section may be placed in contact with the chemFET array of the invention and changes in the section may be detected either in the presence or absence of stimulation such as but not limited to neurotoxins and the like. Transduction of neural processes and/or stimulation can thereby be analyzed. In these embodiments, the chemFETs may operate by detecting calcium and/or potassium fluxes via the passivation layer itself or via receptors for these ions that are coated onto the passivation layer.

[00359] In yet another aspect, the invention contemplates the use of chemFET arrays, functionalized as described herein or in another manner, for use in vivo. Such an array may be introduced into a subject (e.g., in the brain or other region that is subject to ion flux) and then analyzed for changes based on the status of the subject.

[00360] While several inventive embodiments have been described and illustrated herein, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the function and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the inventive embodiments described herein. More generally, those skilled in the art will readily appreciate that all parameters, dimensions, materials, and configurations described herein are meant to be exemplary and that the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the inventive teachings is/are used. Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific inventive embodiments described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described and claimed. Inventive embodiments of the present disclosure are directed to each individual feature, system, article, material, kit, and/or method described herein. In addition, any combination of two or more such features, systems, articles, materials, kits, and/or methods, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the inventive scope of the present disclosure.

[00361] All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

[00362] The indefinite articles "a" and "an," as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean "at least one."

[00363] The phrase "and/or," as used herein in the specification and in the claims, should be understood to mean "either or both" of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with "and/or" should be construed in the same fashion, i.e., "one or more" of the elements so conjoined. Other elements may optionally be present other than the elements specifically identified by the "and/or" clause, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to "A and/or

B", when used in conjunction with open-ended language such as "comprising" can refer, in one embodiment, to A only (optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

[00364] As used herein in the specification and in the claims, "or" should be understood to have the same meaning as "and/or" as defined above. For example, when separating items in a list, "or" or "and/or" shall be interpreted as being inclusive, i.e., the inclusion of at least one, but also including more than one, of a number or list of elements, and, optionally, additional unlisted items. Only terms clearly indicated to the contrary, such as "only one of" or "exactly one of," or, when used in the claims, "consisting of," will refer to the inclusion of exactly one element of a number or list of elements. In general, the term "or" as used herein shall only be interpreted as indicating exclusive alternatives (i.e. "one or the other but not both") when preceded by terms of exclusivity, such as "either," "one of," "only one of," or "exactly one of." "Consisting essentially of," when used in the claims, shall have its ordinary meaning as used in the field of patent law.

[00365] As used herein in the specification and in the claims, the phrase "at least one," in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, "at least one of A and B" (or, equivalently, "at least one of A or B," or, equivalently "at least one of A and/or B") can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

[00366] It should also be understood that, unless clearly indicated to the contrary, in any methods claimed herein that include more than one step or act, the order of the steps or acts of the method is not necessarily limited to the order in which the steps or acts of the method are recited.

[00367] In the claims, as well as in the specification above, all transitional phrases such as "comprising," "including," "carrying," "having," "containing," "involving," "holding," "composed of," and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases "consisting of" and "consisting essentially of" shall be closed or semi-closed transitional phrases, respectively, as set forth in the United States Patent Office Manual of Patent Examining Procedures, Section 2111.03.

Examples

[00368] The following is an example of a proof of principle for rapid sequencing of single-stranded oligonucleotides using an ISFET array.

[00369] **1.1. Binding of Single-Stranded Oligonucleotides to Streptavidin-Coated Magnetic Beads.**

[00370] Single-stranded DNA oligonucleotide templates with a 5' Dual Biotin tag (HPLC purified), and a 20-base universal primer were ordered from IDT (Integrated DNA Technologies, Coralville, IN). Templates were 60 bases in length, and were designed to include 20 bases at the 3' end that were complementary to the 20-base primer (Table 1, *italics*). The lyophilized and biotinylated templates and primer were re-suspended in TE buffer (10 mM Tris-HCl, 1 mM EDTA, pH 8) as 40 μM stock solutions and as a 400 μM stock solution, respectively, and stored at -20 °C until use.

[00371] For each template, 60 μl of magnetic 5.91 μm (Bangs Laboratories, Inc. Fishers, IN) streptavidin-coated beads, stored as an aqueous, buffered suspension (8.57×10^4 beads/μL), at 4°C, were prepared by washing with 120 μl bead wash buffer three times and then incubating with templates 1, 2, 3 and 4 (T1, T2, T3, T4: Table 1) with biotin on the 5' end, respectively.

[00372] Due to the strong covalent binding affinity of streptavidin for biotin (Kd ~ 10-15), these magnetic beads are used to immobilize the templates on a solid support, as

described below. The reported binding capacity of these beads for free biotin is 0.650 pmol/ µL of bead stock solution. For a small (<100 bases) biotinylated ssDNA template, it was conservatively calculated that 9.1 x 10^5 templates could be bound per bead. The beads are easily concentrated using simple magnets, as with the Dynal Magnetic Particle Concentrator or MPC-s (Invitrogen, Carlsbad, CA). The MPC-s was used in the described experiments.

[00373] An MPC-s was used to concentrate the beads for 1 minute between each wash, buffer was then added and the beads were resuspended. Following the third wash the beads were resuspended in 120 µL bead wash buffer plus 1 µl of each template (40 µM). Beads were incubated for 30 minutes with rotation (Labquake Tube Rotator, Barnstead, Dubuque, IA). Following the incubation, beads were then washed thee times in 120 µL Annealing Buffer (20 mM Tris-HCl, 5 mM magnesium acetate, pH 7.5), and re-suspended in 60 µL of the same buffer.

Table 1. Sequences for Templates 1, 2, 3, and 4

T1: 5'/52Bio/GCA AGT GCC CTT AGG CTT CAG TTC AAA AGT CCT AAC TGG G*CA AGG CAC ACA GGG GAT AGG-3'* (SEQ ID NO:1)
T2: 5'/52Bio/CCA TGT CCC CTT AAG CCC CCC CCA TTC CCC CCT GAA CCC C*CA AGG CAC ACA GGG GAT AGG-3'* (SEQ ID NO:2)
T3: 5'/ 52Bio/AAG CTC AAA AAC GGT AAA AAA AAG CCA AAA AAC TGG AAA A*CA AGG CAC ACA GGG GAT AGG-3'* (SEQ ID NO:3)
T4: 5'/ 52Bio/TTC GAG TTT TTG CCA TTT TTT TTC GGT TTT TTG ACC TTT T*CA AGG CAC ACA GGG GAT AGG-3'* (SEQ ID NO:4)

[00374] 1.2. Annealing of Sequencing Primer.

[00375] The immobilized templates, bound at the 5' end to 5.91 µm magnetic beads, are then annealed to a 20-base primer complementary to the 3' end of the templates (Table 1). A 1.0 µL aliquot of the 400 µM primer stock solution, representing a 20-fold excess of primer to immobilized template, is then added and then the beads plus template are incubated with primer for 15 minutes at 95°C and the temperature was then slowly lowered to room temperature. The beads were then washed 3 times in 120 µL of 25 mM Tricine buffer (25 mM Tricine, 0.4 mg/ml PVP, 0.1 % Tween 20, 8.8mM Magnesium Acetate; ph 7.8) as described above using the MPC-s. Beads were resuspended in 25 mM Tricine buffer.

[00376] **1.3. Incubation of Hybridized Templates/Primer with DNA Polymerase.**

[00377] Template and primer hybrids are incubated with polymerase essentially as described by Margulies et al. Nature 2005 437(15):376-380 and accompanying supplemental materials.

[00378] **2. Loading of Prepared Test Samples onto the ISFET Sensor Array.**

[00379] The dimensions and density of the ISFET array and the microfluidics positioned thereon may vary depending on the application. A non-limiting example is a 512 x 512 array. Each grid of such an array (of which there would be 262144) has a single ISFET. Each grid also has a well (or as they may be interchangeably referred to herein as a "microwell") positioned above it. The well (or microwell) may have any shape including columnar, conical, square, rectangular, and the like. In one exemplary conformation, the wells are square wells having dimensions of 7 x 7 x 10 μm. The center-to-center distance between wells is referred to herein as the "pitch". The pitch may be any distance although it is preferably to have shorter pitches in order to accommodate as large of an array as possible. The pitch may be less than 50 μm, less than 40 μm, less than 30 μm, less than 20 μm, or less than 10 μm. In one embodiment, the pitch is about 9 μm. The entire chamber above the array (within which the wells are situated) may have a volume of equal to or less than about 30 μL, equal to or less than about 20 μL, equal to or less than about 15 μL, or equal to or less than 10 μL. These volumes therefore correspond to the volume of solution within the chamber as well.

[00380] **2.1 Loading of Beads in an 'Open' System.**

[00381] Beads with templates 1-4 were loaded on the chip (10 μL of each template). Briefly, an aliquot of each template was added onto the chip using an Eppendorf pipette. A magnet was then used to pull the beads into the wells.

[00382] **2.2 Loading of Beads in a 'Closed' System.**

[00383] Both the capture beads the packing beads are loaded using flow. Microliter precision of bead solution volume, as well as positioning of the bead solution through the fluidics connections, is achieved as shown in Fig. 62 using the bead loading fitting, which includes a major reservoir (approx. 1mL in volume), minor reservoir (approx. 10μL in volume), and a microfluidic channel for handling small volumes of bead solution. This

method also leverages the microliter precision of fluid application allowed by precision pipettes.

[00384] The chip comprising the ISFET array and flow cell is seated in the ZIF (zero insertion force) socket of the loading fixture, then attaching a stainless steel capillary to one port of the flow cell and flexible nylon tubing on the other port. Both materials are microfluidic-type fluid paths (e.g., on the order of < 0.01" inner diameter). The bead loading fitting, consisting of the major and minor reservoirs, it attached to the end of the capillary. A common plastic syringe is filled with buffer solution, then connected to the free end of the nylon tubing. The electrical leads protruding from the bottom of the chip are inserted into a socket on the top of a fixture unit (not shown).

[00385] The syringe is pushed to inject the buffer solution through the tubing, across the flow cell (and chip surface) and up through the capillary as shown in Fig. 63. This process is called priming, and ensures that the fluidic circuit is free of air. The buffer is injected until the level of the liquid can be seen at the top of the minor reservoir, through the transparent major reservoir.

[00386] Next, a solution containing the nucleic acid-coated beads is applied with a precision pipette to the minor reservoir, as shown in Fig. 64. This application produces a large droplet at the top of the reservoir. The volume of solution added is equal to the volume of the flow chamber (e.g., on the order of 10 μL), and has a concentration of beads, such that when added to the volume of buffer solution initially in the minor reservoir, produces the desired concentration of beads to be delivered to the flow cell. The pipette is retracted, and the syringe is pulled carefully and slowly until the droplet recedes to the top of the minor reservoir, again viewed through the transparent major reservoir as shown in Fig. 65. Because the microfluidic channel extending down from the minor reservoir is very small (e.g., on the order of 0.01" diameter), very little mixing occurs between the bead solution and buffer solution in the fluidic path during this process.

[00387] At this point, the bead solution is loaded into the fluidic path, but is not yet at the location of flow cell. Before transferring the bead solution plug, or volume of bead solution in the fluidic path, the solution in the minor reservoir is cleaned. First, approximately 1mL of buffer solution is injected into the major reservoir, effectively diluting the bead solution left in the minor reservoir, as shown in Fig. 66. Then, the solution is pipetted out by placing

a pipette tip along the bottom edge of the major reservoir. The level of solution in the minor reservoir is left at its top as shown in Fig. 67.

[00388] A volume of buffer solution is then added as droplet above the minor reservoir, as in prior bead solution application as shown in Fig. 68. The volume of this solution is equal to the volume of the fluidic path between the minor reservoir and the flow chamber of the flow cell (i.e., the microfluidic channel volume plus the capillary volume plus the volume of flow cell before the flow chamber). Again, the syringe is pulled until the droplet retracts to the top of the minor reservoir as shown in Fig. 69. Now the bead solution plug is loaded into the flow cell's flow chamber.

[00389] The loading fixture is now lifted and placed over a pyramidal base, containing a magnet at its apex, as shown in Fig. 70. The magnet pulls the beads from the bead solution into the microwells of the chip. The fixture is removed from the base after a few seconds. The entire process, excluding the initial priming of the fluidics with buffer solution, can be repeated for the loading of small packing beads into the microwells, if necessary.

[00390] It will be appreciated that there will be other ways of drawing the beads into the wells of the flow chamber, including centrifugation or gravity. The invention is not limited in this respect.

[00391] **3. DNA Sequencing using the ISFET Sensor Array.**

[00392] **3.1 DNA Sequencing in an 'Open' System.**

[00393] The results shown are representative of an experiment carried out in an 'open' system (i.e., the ISFET chip is placed on the platform of the ISFET apparatus and then each nucleotide (5 μL resulting in 6.5 μM each) was manually added in the following order: dATP, dCTP, dGTP and dTT (100 mM stock solutions, Pierce, Milwaukee, WI), by pipetting the given nucleotide into the liquid already on the surface of the chip and collecting data from the chip at a rate of 2.5 mHz. This resulted in data collection over 7.5 seconds at approximately 18 frames/second. Data were then analyzed using LabView.

[00394] Given the sequences of the templates, addition of dATP resulted in a 4 base extension in template 4. Addition of dCTP resulted in a 4 base extension in template 1. Addition of dGTP caused template 1, 2 and 4 to extend as indicated in Table 2 and addition of dTTP results in a run-off (extension of all templates as indicated).

[00395] Fig. 71 (A-D) illustrates the extension reactions. In the left panel, all pixels for one snapshot in time are shown, and on the right, mV vs. time graphs are shown for four selected pixels from the set on the left. White arrows indicate active pixels where extensions are taking place. In the run-off (Fig. 71D) in addition to the wells marked in Fig. 71C, an additional arrow indicates a well where an extension did not take place following the addition of dGTP, but rather dATP and is then seen again during the run-off.

[00396] Preferably when the method is performed in a non-automated manner (i.e., in the absence of automated flow and reagent introduction), each well contains apyrase in order to degrade the unincorporated dNTPs. It is to be understood that apyrase can be substituted, in this embodiment or in any other embodiment discussed herein, with another compound (or enzyme) capable of degrading dNTPs.

[00397] **Table 2.** Set-up of experiment and order of nucleotide addition.

	dATP	dCTP	dGTP	dTTP
T1	0	(3:C; 1:A)4	1	Run-off (25)
T2	0	0	4	Run-off (26)
T3	0	0	0	Run-off (30)
T4	4	0	2	Run-off (24)

[00398] 3.2 **DNA Sequencing Using Microfluidics on Sensor Chip**

[00399] Sequencing in the flow regime is an extension of open application of nucleotide reagents for incorporation into DNA. Rather than add the reagents into a bulk solution on the ISFET chip, the reagents are flowed in a sequential manner across the chip surface, extending a single DNA base(s) at a time. The dNTPs are flowed sequentially, beginning with dTTP, then dATP, dCTP, and dGTP. Due to the laminar flow nature of the fluid movement over the chip, diffusion of the nucleotide into the microwells and finally around the nucleic acid loaded bead is the main mechanism for delivery. The flow regime also ensures that the vast majority of nucleotide solution is washed away between applications. This involves rinsing the chip with buffer solution and apyrase solution following every nucleotide flow. The nucleotides and wash solutions are stored in chemical bottles in the system, and are flowed over the chip using a system of fluidic tubing and automated valves.

The ISFET chip is activated for sensing chemical products of the DNA extension during nucleotide flow.

CLAIMS

1. An apparatus, comprising:

an array (100) of CMOS-fabricated sensors (105), each sensor comprising one chemically-sensitive field effect transistor (chemFET) (150) and occupying an area on a surface of the array of approximately ten micrometers by ten micrometers or less and each sensor configured to provide at least one output signal representing a presence and/or concentration of an analyte proximate to said surface.

2. The apparatus of claim 1, wherein the area occupied by each sensor is approximately nine micrometers by nine micrometers or less.

3. The apparatus of claim 2, wherein the area occupied by each sensor is approximately five micrometers by five micrometers or less.

4. The apparatus of claim 3, wherein the area occupied by each sensor is approximately three micrometers by three micrometers or less.

5. The apparatus of any of claims 1 to 4, wherein the plurality of CMOS-fabricated sensors includes more than 256 sensors.

6. The apparatus of claim 5, wherein the array includes a two-dimensional array of at least 512 rows and at least 512 columns of the CMOS-fabricated sensors.

7. The apparatus of claim 6, wherein the two-dimensional array includes at least 2048 rows and at least 2048 columns of the CMOS-fabricated sensors.

8. The apparatus of claim 6, wherein the two-dimensional array includes at least 7400 rows and at least 7400 columns of the CMOS-fabricated sensors.

9. The apparatus of any of claims 5 to 8, wherein a collection of chemFET output signals from all chemFETs of the array constitutes a frame of data, and wherein the apparatus

further comprises control circuitry (110, 192, 194, 198) coupled to the array and configured to generate at least one array output signal (Vout) to provide multiple frames of data from the array at a frame rate of at least 10 frames per second.

10. The apparatus of claim 9, wherein the control circuitry is configured such that the frame rate is at least 20 frames per second.

11. The apparatus of claim 10, wherein the control circuitry is configured such that the frame rate is at least 30 frames per second.

12. The apparatus of claim 11, wherein the control circuitry is configured such that the frame rate is at least 40 frames per second.

13. The apparatus of any of claims 1 to 12, wherein the chemFET of each sensor comprises:

a floating gate structure (170); and

a source (156) and a drain (158) having a first semiconductor type and fabricated in a region (154) having a second semiconductor type, wherein there is no electrical conductor that electrically connects the region having the second semiconductor type to either the source or the drain.

14. The apparatus of claim 13, further comprising at least one first electrical conductor to electrically connect together all regions having the second semiconductor type of all chemFETs in the array.

15. The apparatus of any of claims 1 to 14, wherein each sensor comprises:

a plurality of field effect transistors (FETs), including the chemFET; and

a plurality of second electrical conductors electrically connected to the plurality of FETs, wherein the plurality of FETs are arranged such that the plurality of second electrical conductors includes no more than four conductors traversing an area occupied by each sensor and interconnecting multiple sensors of the array.

16. The apparatus of any of claims 1 to 15, wherein each sensor comprises three or fewer field effect transistors (FETs), including the chemFET.

17. The apparatus of any of claims 15 or 16, wherein all of the FETs in each sensor are of a same channel type and implemented in the region having the second semiconductor type.

18. The apparatus of any of claims 1 to 17, wherein the chemFET of each sensor is an ion-sensitive field effect transistor (ISFET).

19. The apparatus of any of claims 1 to 17, wherein:

at least one first sensor of the array includes a first chemFET configured to be chemically sensitive to at least one first analyte; and

at least one second sensor of the array includes a second chemFET configured to be chemically sensitive to at least one second analyte different from the at least one first analyte.

20. The apparatus of claim 19, wherein the at least one first analyte represents at least one first binding event associated with a nucleic acid sequencing process, and wherein the at least one second analyte represents at least one second binding event associated with the nucleic acid sequencing process.

21. The apparatus of any of claims 1 to 20 wherein said array further comprises a plurality of reaction chambers disposed thereon such that each reaction chamber is in contact with a chemFET of said sensor array.

22. An apparatus, comprising:

an array (100) of CMOS-fabricated sensors (105), each sensor comprising a chemically-sensitive field effect transistor (chemFET) (150), the chemFET comprising:

a floating gate structure (170); and

a source (156) and a drain (158) having a first semiconductor type and fabricated in a region (154) having a second semiconductor type, wherein there is no electrical conductor that electrically connects the region having the second semiconductor type to either the source or the drain.

23. The apparatus of claim 22, further comprising at least one first electrical conductor to electrically connect together all regions having the second semiconductor type of all chemFETs in the array.

24. The apparatus of claims 22 or 23, wherein the chemFET is a p-channel chemFET, and wherein the region having the second semiconductor type is formed as an n-type well in a p-type substrate (152) for the array.

25. The apparatus of any of claims 22-24, wherein each sensor comprises:

a plurality of field effect transistors (FETs), including the chemFET; and

a plurality of second electrical conductors electrically connected to the plurality of FETs,

wherein the plurality of FETs are arranged such that the plurality of second electrical conductors includes no more than four conductors traversing an area occupied by each sensor and interconnecting multiple sensors of the array.

26. The apparatus of any of claims 22-25, wherein each sensor comprises three or fewer field effect transistors (FETs), including the chemFET.

27. The apparatus of claim 26, wherein each sensor consists of three FETs, including the chemFET.

28. The apparatus of any of claims 25-27, wherein all of the FETs in each sensor are of a same channel type and implemented in the region having the second semiconductor type.

29. The apparatus of claim 28, wherein all of the FETs in each sensor are p-channel FETs, and wherein the region having the second semiconductor type is formed as an n-type well (154) in a p-type substrate (152) for the array.

30. The apparatus of any of claims 22-29, wherein each sensor occupies an area on a surface of the array of ten micrometers by ten micrometers or less.

31. The apparatus of claim 30, wherein the area occupied by each sensor is approximately five micrometers by five micrometers or less.

32. The apparatus of claim 31, wherein the area occupied by each sensor is approximately three micrometers by three micrometers or less.

33. The apparatus of any of claims 22-32, wherein the array includes a two-dimensional array of the CMOS-fabricated sensors arranged in a plurality of rows and a plurality of columns.

34. The apparatus of claim 33, wherein the array includes at least 512 rows and at least 512 columns of the CMOS-fabricated sensors.

35. The apparatus of claim 33 or 34, wherein for each column of the plurality of columns, the array further comprises:

column circuitry (110) configured to provide a constant drain current and a constant drain-to-source voltage to respective chemFETs in the column.

36. The apparatus of claim 35, wherein the column circuitry includes two operational amplifiers (107A,B) and a diode-connected FET arranged in a Kelvin bridge configuration with the respective chemFETs to provide the constant drain-to-source voltage.

37. The apparatus of any of claims 33-36, wherein the array further comprises:

at least one row select shift register (192) to enable respective rows of the plurality of rows; and

at least one column select shift register (194) to acquire chemFET output signals from respective columns of the plurality of columns.

38. The apparatus of claim 37, wherein the at least one column select shift register includes a plurality of column select shift registers (194_1, 194_2) to simultaneously acquire chemFET output signals from multiple columns of the plurality of columns.

39. The array of claims 37 or 38, wherein the at least one row select shift register includes a plurality of row select shift registers to simultaneously enable multiple rows of the plurality of rows.

40. The apparatus of any of claims 33-39, further comprising at least one output driver (198), the at least one output driver comprising:

at least one buffer amplifier (199); and

at least one asymmetric switch (191) to couple at least some columns of the plurality of columns to the at least one buffer amplifier so as to provide at least one array output signal (Vout),

wherein the at least one asymmetric switch comprises a CMOS-pair transmission gate having differently-sized FETs.

41. The apparatus of claim 40, wherein a collection of chemFET output signals from all chemFETs of the array constitutes a frame of data, and wherein the at least one row select shift register, the at least one column select shift register, and/or the at least one output driver is/are configured to generate the at least one array output signal so as to provide multiple frames of data from the array at a frame rate of at least 20 frames per second.

42. The apparatus of any of claims 22-41, wherein the chemFET of each sensor is an ion-sensitive field effect transistor (ISFET).

43. An apparatus, comprising:

an array (100) of CMOS-fabricated sensors (105), each sensor comprising a chemically-sensitive field effect transistor (chemFET) (150), the chemFET comprising:

a floating gate structure (170); and

a source (156) and a drain (158) having a first semiconductor type and fabricated in a region (154) having a second semiconductor type, wherein there is no electrical conductor that electrically connects the region having the second semiconductor type to either the source or the drain,

wherein:

the array includes a two-dimensional array of at least 512 rows and at least 512 columns of the CMOS-fabricated sensors;

each sensor consists of three field effect transistors (FETs) including the chemFET;

each sensor includes a plurality of electrical conductors electrically connected to the three FETs;

the three FETs are arranged such that the plurality of electrical conductors includes no more than four conductors traversing an area occupied by each sensor and interconnecting multiple sensors of the array;

all of the FETs in each sensor are of a same channel type and implemented in a single semiconductor region of an array substrate; and

a collection of chemFET output signals from all chemFETs of the array constitutes a frame of data,

and wherein the apparatus further comprises:

control circuitry (110, 192, 194, 198) coupled to the array and configured to generate at least one array output signal (Vout) to provide multiple frames of data from the array at a frame rate of at least 20 frames per second.

44. A method for sequencing a nucleic acid comprising

disposing a plurality of template nucleic acids into a plurality of reaction chambers, wherein the plurality of reaction chambers is in contact with a chemical-sensitive field effect transistor (chemFET) array comprising at least one chemFET for each reaction chamber, and wherein each of the template nucleic acids is hybridized to a sequencing primer and is bound to a polymerase,

synthesizing a new nucleic acid strand by incorporating one or more known nucleotide triphosphates sequentially at the 3' end of the sequencing primer,

detecting the incorporation of the one or more known nucleotide triphosphates by a change in current at the at least one chemFET within the array.

45. The method of claim 44, wherein the chemFET array comprises more than 256 sensors.

46. The method of claim 44, wherein said array comprises more than 10,000 of said chemFETs.

47. The method of claim 44, wherein chemFETs of the array are of the same n-channel type or the same p-channel type.

48. The method of claim 44, wherein said chemFET array has a pitch less than 10 μm.

49. The method of claim 44, wherein the body of each said chemFET is not connected to its source.

50. A method for sequencing a nucleic acid comprising

disposing a plurality of template nucleic acids into a plurality of reaction chambers, wherein the plurality of reaction chambers is in contact with an chemical-sensitive field effect transistor (chemFET) array comprising at least one chemFET for each reaction chamber, and wherein each of the template nucleic acids is hybridized to a sequencing primer and is bound to a polymerase,

synthesizing a new nucleic acid strand by incorporating one or more known nucleotide triphosphates sequentially at the 3' end of the sequencing primer,

detecting the incorporation of the one or more known nucleotide triphosphates by the generation of sequencing reaction byproduct,

wherein a center-to-center distance between adjacent reaction chambers is 1-10 μm.

51. A method for sequencing a nucleic acid comprising

disposing a plurality of template nucleic acids into a plurality of reaction chambers, wherein the plurality of reaction chambers is in contact with an chemical-sensitive field effect transistor (chemFET) array comprising at least one chemFET for each reaction chamber, and wherein each of the template nucleic acids is hybridized to a sequencing primer and is bound to a polymerase,

synthesizing a new nucleic acid strand by incorporating one or more known nucleotide triphosphates sequentially at the 3' end of the sequencing primer,

directly detecting release of inorganic pyrophosphate (PPi) as an indicator of incorporation of the one or more known nucleotide triphosphates.