

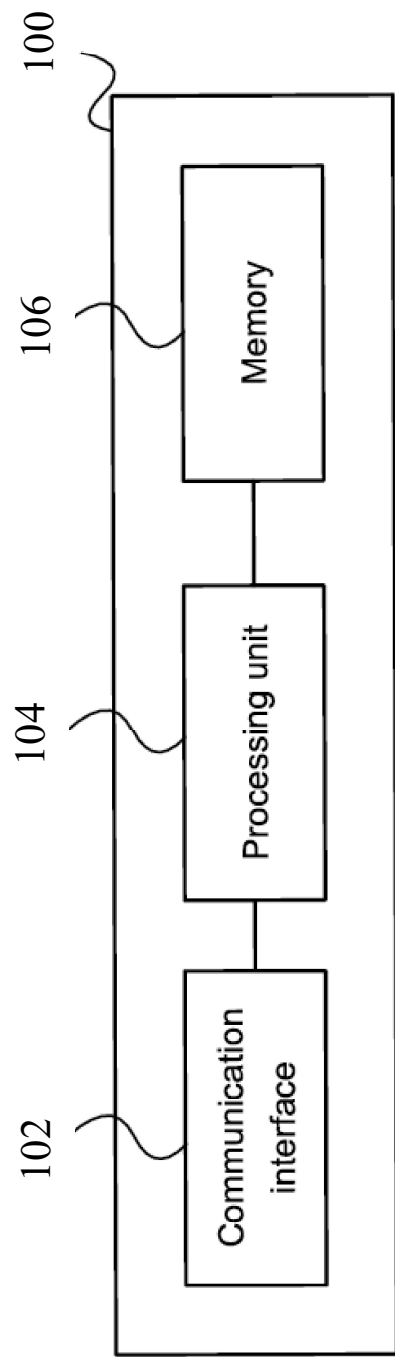


FIG. 1

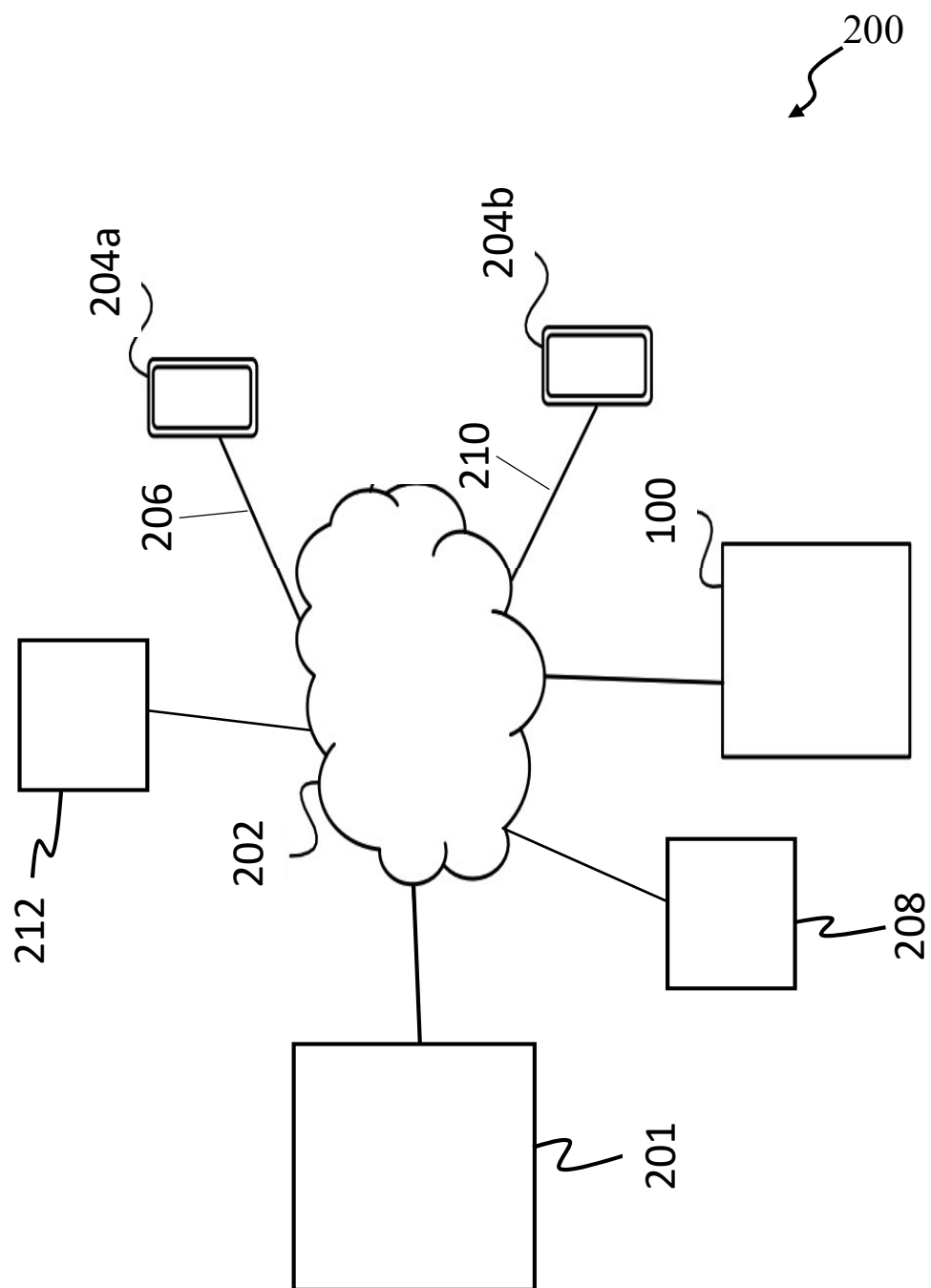
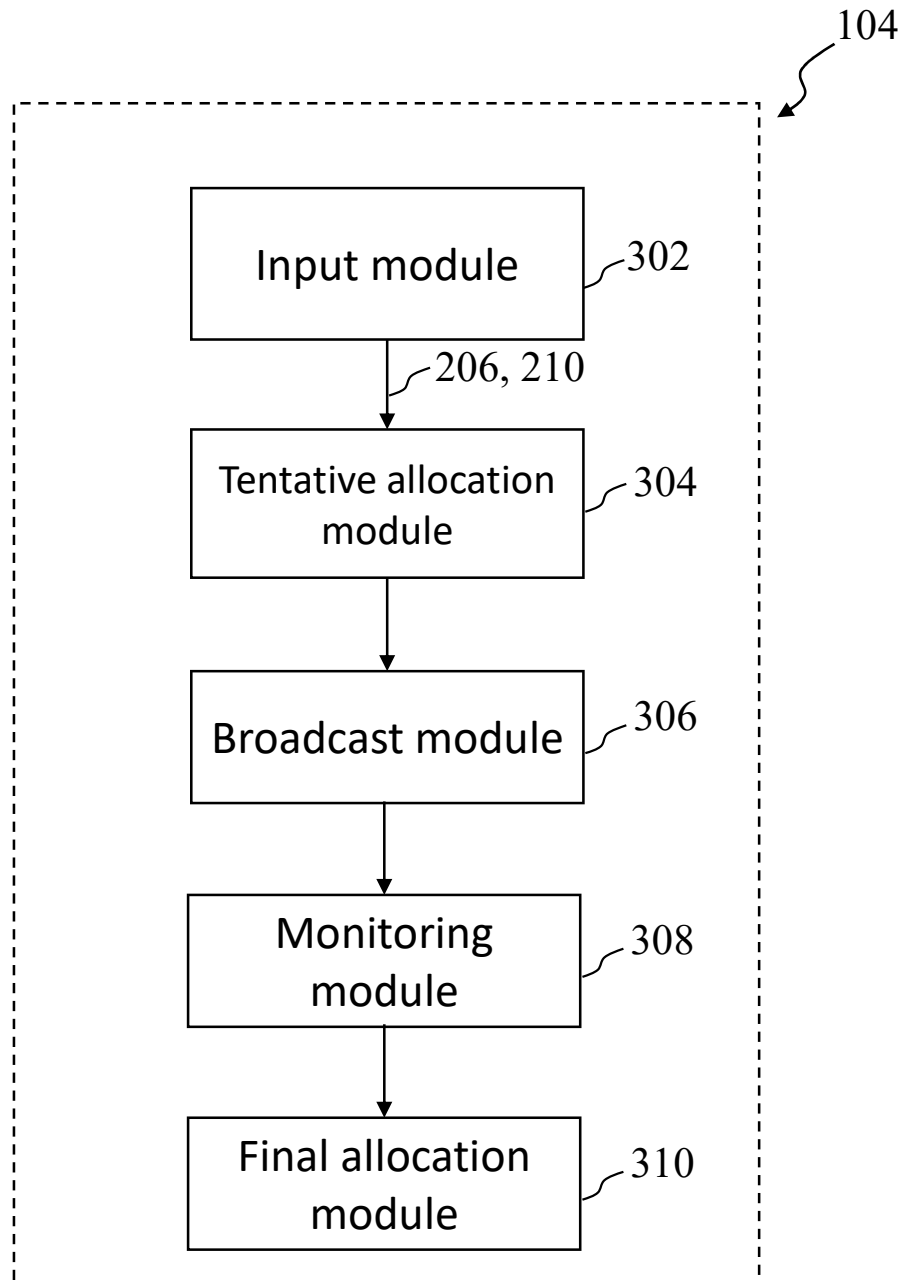


FIG. 2



 Modules may be optionally integrated and implemented as a single processor

FIG. 3

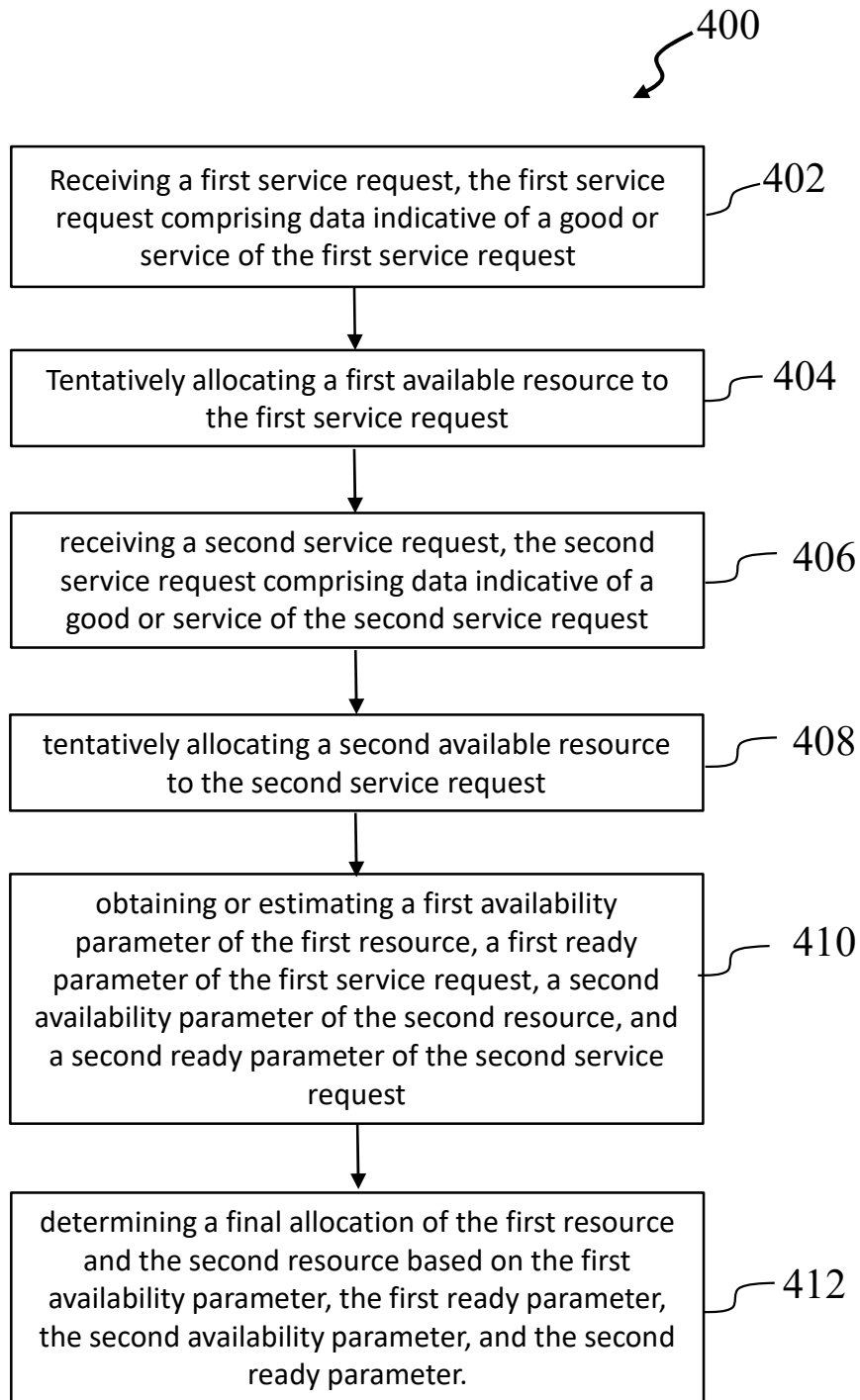


FIG. 4