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(21) International Application Number: PCT/US98/23563 (22) International Filing Date: 3 November 1998 (03.11.98) (30) Priority Data: 08/988,232 10 December 1997 (10.12.97) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): PAWLOWSKI, Stephen, S. [US/US]; 6624 S.W. 158th Avenue, Beaverton, OR 97007 (US). LAU, Daniel, G. [US/US]; 1800 Austin Avenue, Los Altos, CA 94024 (US). WEIER, Kimberly, C. [US/US]; 13742 S.W. Tracy Place, Tigard, OR 97223 (US). (74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).		(81) Designated States: AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.	

(54) Title: TRANSACTIONS SUPPORTING INTERRUPT DESTINATION REDIRECTION AND LEVEL TRIGGERED INTERRUPT SEMANTICS

(57) Abstract

In one embodiment, the invention includes an apparatus, such as a bridge (104), for use with a computer system (100) having a processor bus (18). The apparatus includes decode logic (36) to receive through the processor bus a task priority designation of a processor of the computer system, and to provide a signal responsive thereto. The apparatus also includes remote priority capture logic (32) to receive the signal responsive to the task priority update transaction and update contents of the remote priority capture logic in response thereto. In another embodiment, the invention includes an apparatus for use with a computer system having a processor bus. The apparatus includes decode logic to receive through the processor bus an end-of-interrupt (EOI) transactions and to provide an EOI signal responsive thereto. The apparatus also includes an interrupt controller including a table having a state bit that is set in response to the interrupt controller receiving an interrupt signal and reset in response to the interrupt controller receiving the EOI signal.

