

## DYNAMIC REDUNDANCY FOR RANDOM ACCESS MEMORY ASSEMBLIES

## ABSTRACT

Reduced specification DRAMs ( $13_1, \dots, 13_8$ ) are used in memory assemblies in such a way as to maximize the use of the good cells in the reduced specification DRAM chips ( $13_1, \dots, 13_8$ ). An external memory array is mapped to replace defective memory locations on a real time basis. The major components are (1) a non-volatile storage device (14), (2) a logic device (15), and (3) a volatile storage device. The non-volatile storage device (14), such as an EPROM, EEPROM, or a flash memory chip, is used to retain address information for all memory fails on a given assembly. The logic device (15) is an ASIC or programmable logic device which contains the bit steering logic and timing generation logic to redirect defective RAM addresses to an alternate storage device for all read and write operations. The volatile storage device is a RAM array that is used to replace failing address locations in the original reduced specification memory. This array may be in the form a static random access memory (SRAM or DRAM) array, resident in the logic device (15) described above. The size of the device determines the amount of failing addresses that can be allowed in the reduced specification memory.

Fig. 1

This Sheet Has Been Replaced



THIS SHEET HAS BEEN  
REPLACED