CLAIMS

1. A method, comprising:

receiving, at a controller, a first set of bits of an input vector from a host device;

determining whether a quantity of the first set of bits that have a first logic value is within a threshold interval stored at the controller;

allocating a block of memory to store one or more bits and the first set of bits based at least in part on the determining;

generating a second set of bits that comprises at least some of the first set of bits and the one or more bits; and

initiating storing the generated second set of bits in the block of memory.

2. The method of claim 1, further comprising:

dividing the first set of bits into one or more bit segments based at least in part on a factor associated with the threshold interval;

selecting at least one bit segment of the one or more bit segments; and

inverting a logic state of a set of bits of the selected at least one bit segment.

3. The method of claim 2, further comprising:

determining a number of bit segments of the one or more bit segments based at least in part on the factor associated with the threshold interval, wherein a number of the one or more bits corresponds to the number of bit segments.

4. A method, comprising:

receiving, at a controller, a first set of bits of an input vector from a host device;

comparing at least a portion of the first set of bits that have a first logic value to a threshold stored at the controller, wherein comparing at least the portion of the first set of bits comprises:

identifying a percentage of bits of the input vector having a first logic state; and

comparing the percentage to a percentage range, the percentage range based at least in part on a factor associated with the threshold;

allocating a block of memory to store one or more bits and the first set of bits based at least in part on the comparing;

generating a second set of bits that comprises at least some of the first set of bits and the one or more bits; and

initiating storing the generated second set of bits in the block of memory.

5. The method of claim 1, wherein determining whether the quantity of the first set of bits that have the first logic value is within the threshold interval comprises:

determining that the quantity of the first set of bits is outside of the threshold interval; and

inverting respective logic states of the first set of bits based at least in part on the determination that the quantity of the first set of bits is outside of the threshold interval.

6. The method of claim 5, further comprises:

determining that the quantity of the first set of bits is outside of the threshold interval based at least in part on inverting the respective logic states of the first set of bits;

restoring original logic states of the first set of bits based on the determination that the quantity of the first set of bits is outside of the threshold interval after the inversion; and

comparing a different portion of the first set of bits that have the first logic value to the threshold interval stored at the controller.

7. A method, comprising:

receiving, at a controller, a first set of bits of an input vector from a host device;

comparing at least a portion of the first set of bits that have a first logic value to a threshold stored at the controller, wherein comparing at least the portion of the first set of bits comprises:

comparing a pattern weight of the input vector to a range that is based at least in part on a factor associated with the threshold;

allocating a block of memory to store one or more bits and the first set of bits based at least in part on the comparing;

generating a second set of bits that comprises at least some of the first set of bits and the one or more bits; and

initiating storing the generated second set of bits in the block of memory.

8. A method comprising:

receiving, at a controller, a first set of bits of an input vector from a host device;

determining a pattern weight of the input vector based at least in part on a number of bits having a first logic state, the first logic state associated with a first set of threshold voltages of memory cells, wherein the first set of threshold voltages is less than a second set of threshold voltages associated with a second logic state different from the first logic state;

comparing at least a portion of the first set of bits that have the first logic state to a threshold stored at the controller;

allocating a block of memory to store one or more bits and the first set of bits based at least in part on the comparing;

generating a second set of bits that comprises at least some of the first set of bits and the one or more bits; and

initiating storing the generated second set of bits in the block of memory.

9. An electronic memory apparatus, comprising:

a memory medium; and

a controller coupled with the memory medium, wherein the controller is operable to:

receive a first set of bits of an input vector from a host device;

determine whether a quantity of the first set of bits that have a first logic value is within a threshold interval stored at the controller;

allocate a block of memory of the memory medium to store one or more bits and the first set of bits based at least in part on the determining;

generate a second set of bits that comprises at least some of the first set of bits and the one or more bits; and

initiate storing the generated second set of bits in the block of memory.

10. The electronic memory apparatus of claim 9, wherein the controller is further operable to:

divide the first set of bits into one or more bit segments based at least in part on a factor associated with the threshold interval;

select at least one bit segment of the one or more bit segments; and

invert a logic state of a set of bits of the selected at least one bit segment.

11. An electronic memory apparatus, comprising:

a memory medium; and

a controller coupled with the memory medium, wherein the controller is operable to:

receive a first set of bits of an input vector from a host device;

compare at least a portion of the first set of bits that have a first logic value to a threshold stored at the controller, wherein the controller is further operable to:

identify a percentage of bits of the input vector having a first logic state; and

compare the percentage to a percentage range, the percentage range based at least in part on a factor associated with the threshold;

allocate a block of memory of the memory medium to store one or more bits and the first set of bits based at least in part on the comparing;

generate a second set of bits that comprises at least some of the first set of bits and the one or more bits; and

initiate storing the generated second set of bits in the block of memory.

12. The electronic memory apparatus of claim 9, wherein the controller is further operable to:

determine that the quantity of the first set of bits is outside of the threshold interval; and

invert respective logic states of the first set of bits based at least in part on the determination that the quantity of the first set of bits is outside of the threshold interval.

13. An electronic memory apparatus, comprising:

a memory medium; and

a controller coupled with the memory medium, wherein the controller is operable to:

receive a first set of bits of an input vector from a host device;

compare at least a portion of the first set of bits that have a first logic value to a threshold stored at the controller, wherein the controller is further operable to:

compare a pattern weight of the input vector to a range, the range based at least in part on a factor associated with the threshold;

allocate a block of memory of the memory medium to store one or more bits and the first set of bits based at least in part on the comparing;

generate a second set of bits that comprises at least some of the first set of bits and the one or more bits; and

initiate storing the generated second set of bits in the block of memory.

14. The electronic memory apparatus of claim 9, wherein:

the memory medium comprises a three-dimensional cross-point array of phase change memory cells.