

Description

The invention relates to an amplifier arrangement being provided with a differential pair comprising at least a first and a second transistor of a first conductivity type, a first main electrode of the first transistor and a first main electrode of the second transistor being mutually coupled and coupled to a first supply terminal by means of a current source, a control electrode of the first transistor being coupled to an input terminal and a control electrode of the second transistor being coupled to an output terminal, with a current mirror comprising at least a third and a fourth transistor of a second conductivity type, a first main electrode of the third transistor and a first main electrode of the fourth transistor being mutually coupled and coupled to a second supply terminal by means of a common terminal, a second main electrode of the third transistor being coupled to a second main electrode of the first transistor and a second main electrode of the fourth transistor being coupled to a second main electrode of the second transistor, and with a buffer stage comprising at least a fifth transistor of the first conductivity type, a control electrode of the fifth transistor being coupled to the second main electrode of the second transistor, a first main electrode of the fifth transistor being coupled to the output terminal and a second main electrode of the fifth transistor being coupled to the second supply terminal.

Such an amplifier arrangement can be widely used and, more specifically, be used as a voltage-to-current converter in integrated semiconductor circuits.

An amplifier arrangement of the described type is known from United States Patent US 4,338, 527.

In this known amplifier arrangement the input terminal is connected to a grounded voltage source, the first and second supply terminals being connected to a negative and a positive supply voltage respectively. Furthermore, the mutually coupled control electrodes of the third and fourth transistors are connected to the mutually coupled second main electrodes of the first and third transistors, so that the second main electrode of the first transistor is adjusted to a voltage equal to the positive supply voltage minus the voltage between the second main electrode and the control electrode of the third transistor. The second main electrode of the second transistor, however, when discarding the offset voltage between the input terminal and the output terminal, is adjusted to a voltage equal to the voltage on the input terminal augmented by the voltage between the second main electrode and the control electrode of the fifth transistor. This known amplifier arrangement is disadvantageous in that with an arbitrary choice of the two supply voltages there is a voltage difference between the respective voltages on the second main electrodes of the first and second transistors, so that the differential

pair is adjusted asymmetrically and, consequently, an undesired non-linear signal transmission from the input terminal to the output terminal takes place. In addition, this disadvantage is enhanced because the voltage on the second main electrode of the first transistor varies with variations of the positive supply voltage, whereas the voltage on the second main electrode of the second transistor does not substantially vary in that case.

It is an object of the invention to provide an amplifier arrangement with improved linear signal transmission.

An amplifier arrangement according to the invention is characterised in that the control electrode of the first transistor is coupled to the common terminal by means of a first level shifting circuit which provides a fixed voltage difference between the common terminal and the control electrode of the first transistor. By means of the level shifting circuit thus coupled a fixed voltage-difference is applied between the common terminal and the control electrode of the first transistor, so that a coupling is achieved between the voltages on the second main electrodes of the first and second transistors. Consequently, the voltage difference between the respective voltages can be adjusted to zero volts and thus an improved linear signal transmission is obtained.

It is to be noted that United States Patent US-A-3 619 798 discloses a current conveyor with a differential transistor pair, additional transistors being provided to obtain a zero voltage offset between the input and the output of the differential transistor pair. It is further noted that United States Patent US-A-4 258 331 discloses a differential amplifier including a current mirror with additional transistors at the input portion. The additional transistors act to absorb the base current of the differential pair and to maintain the input terminal voltage of the differential amplifier at substantially zero potential when no input signal is received irrespective of variations of the power source voltage.

An amplifier arrangement according to the invention can furthermore be characterised in that the control electrode of the fifth transistor is coupled to the second main electrode of the second transistor by means of a second level shifting circuit. By means of the second level shifting circuit thus coupled, an adjustable voltage is applied between the control electrode of the fifth transistor and the second main electrode of the second transistor, so that the voltage between the second main electrode and the control electrode of the second transistor is adjustable. This is advantageous in that the influence of the Early-effect on both the second and first transistors can be reduced. The Early-effect relates to variations of the gain factor of a transistor due to variations of its second main electrode - control electrode voltage. By means of the level shifting circuits inserted according

to the invention the second main electrode - control electrode voltages of both the second and first transistors can be adjusted to zero volts, at which voltage the influence of the Early-effect is practically nothing.

An embodiment of an amplifier arrangement according to the invention can be characterised in that the first level shifting circuit comprises a transistor of the second conductivity type and a current source, a first main electrode of the transistor of the first level shifting circuit being coupled to both the second supply terminal by means of the current source of the first level shifting circuit and to the common terminal, a second main electrode of the transistor of the first level shifting circuit being coupled to the first supply terminal and a control electrode of the transistor of the first level shifting circuit being coupled to the control electrode of the first transistor. In this embodiment the second main electrode and the control electrode of the first transistor are coupled by means of two serially opposed control electrode - main electrode junctions, so that the voltage between these electrodes is adjusted to practically zero volts. In addition, the current source thus coupled achieves that the various voltages in the amplifier arrangement are no longer related to the voltage coupled to the second supply terminal, so that larger output signals can be tapped from the output terminal. Moreover, in this embodiment the control electrode currents of the first and the additional transistors are oppositely oriented. This is advantageous in that the control electrode currents of these transistors compensate each other if properly dimensioned, so that the amplifier arrangement in a state of rest does not cause any current to flow through the input terminal and, consequently, has a high input impedance.

A further embodiment of an amplifier arrangement according to the invention may be characterised in that the second level shifting circuit comprises a transistor of the second conductivity type and a current source, a first main electrode of the transistor of the second level shifting circuit being coupled to both the second supply terminal by means of the current source of the second level shifting circuit and to the control electrode of the fifth transistor, a second main electrode of the transistor of the second level shifting circuit being coupled to the first supply terminal and a control electrode of the transistor of the second level shifting circuit being coupled to the second main electrode of the second transistor. In this embodiment the second main electrode and the control electrode of the second transistor are coupled by means of two serially opposed control electrode - main electrode junctions, so that also the voltage between these electrodes is adjusted to practically zero volts. Since the additional transistor further applies a control electrode current to the second main electrode of the second transistor, in this further embodiment the offset voltage is likewise reduced due to unequal ad-

justing currents through the first and second transistors, if the control electrodes of the third and fourth transistors are coupled to the second main electrode of the third transistor.

A still further embodiment of an amplifier arrangement according to the invention may be characterised in that the current source connected to the differential pair and the current source belonging to the second level shifting circuit are arranged for producing substantially equal currents. With a current mirror comprising only the third and fourth transistors, this embodiment is advantageous in that the control electrode current of the fourth transistor is equal to the sum of the control electrode currents of the third and fourth transistors because the current-source currents are equal. Consequently, in addition to equal second main electrode currents of the third and fourth transistors, also equal control electrode currents are applied to the second main electrodes of the first and second transistors, so that the aforementioned offset voltage is practically zero.

The invention will be further explained with reference to the appended drawing, in which

Fig. 1 shows an amplifier arrangement according to the state of the art,

Fig. 2 shows an embodiment of an amplifier arrangement according to the invention, and

Fig. 3 shows a further embodiment of an amplifier arrangement according to the invention.

In these Figures like components are denoted by like reference characters.

The prior-art amplifier arrangement represented in Fig. 1 shows a differential pair of a first transistor N1 and a second transistor N2, whose mutually coupled emitters are coupled to a first supply terminal 1 by means of a current source I1. The bases of the transistors N1 and N2 are coupled, respectively, to an input terminal 3 for supplying an input signal V_{in} and an output terminal 4 for tapping an output signal V_{out} . The collectors of the transistors N1 and N2 are coupled to respective input and output terminals of a current mirror circuit, which terminals are constituted by the collectors of a third transistor P1 and a fourth transistor P2 respectively. The emitters of the third and fourth transistors are coupled to a second supply terminal 2 by means of a common terminal 5. The bases of the transistors P1 and P2 are mutually coupled and also coupled to the collector of transistor P1, whereas the collector of transistor P2 is likewise coupled to the base of a fifth transistor N3. This transistor N3 constitutes a buffer stage in which its collector is coupled to the supply terminal 2 and its emitter to the output terminal 4. The input signal V_{in} produces complementary current changes in the transistors N1 and N2 with the transistors P1 and P2 of the current mirror following the current changes in the transistor N1. Consequently, the base of the transistor N3 receives a differential current which is the difference between

the collector currents of the transistors N2 and P2, which differential current is amplified by the transistor N3. The amplified differential current results in the output signal V_{out} .

However, the prior-art amplifier arrangement has an undesired non-linear signal transmission as a result of unequal voltages on the collectors of the transistors N1 and N2, which voltages are determined by the control voltage connected to the supply terminal 2 and the adjusted voltage of the input terminal 3 respectively. The non-linear signal transmission is also amplified because the collector voltage of the transistor N1 varies when said supply voltage varies. Resultant voltages between the collector and the base of both transistor N1 and transistor N2 achieve that the prior-art amplifier arrangement circuit is impeded by the Early-effect. An additional disadvantage of this amplifier arrangement is its offset voltage between the input terminal 3 and the output terminal 4. Because the base-emitter voltages of the transistors P1 and P2 are equal, these transistors carry equal collector currents. The collector current of transistor P1 together with the base currents of the transistors P1 and P2 is applied to the collector of transistor N1, whereas the collector current of transistor P2 minus the base current of transistor N3 is applied to the collector of transistor N2. Consequently, the transistors N1 and N2 carry both unequal collector currents and unequal emitter currents of which the latter cause unequal base-emitter voltages. Since the emitters of the transistors N1 and N2 are mutually coupled, these unequal base-emitter voltages result in the undesired offset voltage.

A further disadvantage of the prior-art amplifier arrangement is its relatively low input impedance which is especially undesired if the amplifier arrangement is used as a voltage-current conversion circuit.

Fig. 2 shows an embodiment of an amplifier arrangement according to the invention in which a first level shifting circuit 6 and a second level shifting circuit 7 are additionally inserted in the amplifier arrangement shown in Fig. 1. The level shifting circuit 6 comprises a transistor P3 as well as a current source I2 and is coupled between the base of the transistor N1 and the common terminal 5. In this arrangement the base of transistor P3 is coupled to the base of transistor N1 and the emitter of transistor P3 is coupled to the common terminal 5. This terminal 5 is also coupled to the supply terminal 2 across the current source I2. The collector of the transistor P3 is coupled to the supply terminal 1. The level shifting circuit 7 comprises a transistor P4 as well as a current source I3 and is inserted between the mutually coupled collectors of the transistors N2 and P2 and the base of transistor N3. In this arrangement the base of transistor P4 is coupled to the mutually coupled collectors of the transistors N2 and P2 and the emitter of transistor P4 to the base of transistor N3, which

base is also coupled to the supply terminal 2 by means of the current source I3. The collector of the transistor P4 is connected to the supply terminal 1. The level shifting circuits 6 and 7 thus arranged cause mutually equal voltages to occur on the collectors of the transistors N1 and N2. In addition, contrary to the corresponding voltages in Fig. 1, the voltages are not related to the supply voltage but to the adjusted voltage on the input terminal. Because the base and the collector of transistor N1 are coupled by means of the serially opposed base-emitter junctions of the transistors P3 and P1, there will be a voltage between the base and the collector of transistor N1 which is practically zero volts, with an attendant reduced influence of the Early-effect on the transistor N1. Furthermore, the current source I2 thus coupled causes a reduced influence of variations of the supply voltage on the base-collector voltage of the transistor N1. So as to obtain a likewise reduced influence of the Early-effect on the transistor N2, the base and the collector of transistor N2 are coupled by means of the serially opposed base-emitter junctions of the transistors N3 and P4, so that a voltage of practically zero volts is adjusted also between the base and collector of transistor N2. When adding to the arrangement of Fig. 1 the level shifting circuit 6 without adding the level shifting circuit 7, the level shifting circuit 6 is required to comprise a diode inserted between the emitters of the transistors P1 and P3. The base-collector voltage of transistor N1 is then made equal to the corresponding voltage of transistor N2, so that the Early-effect again has a reduced influence on transistors N1 and N2 with an attendant improved linearity of the signal transmission. An additional advantage of the use of the level shifting circuit 6 is the opposite orientation of the base currents of the transistors N1 and P3. When properly choosing the adjusting currents through these transistors, the base current of transistor N1 in an absolute sense is equal to the base current of transistor P3 so that in a state of rest no current flows through input terminal 3. This increases the input impedance. In addition, the level shifting circuit 7 applies the base current of transistor P3 to the collector of transistor N2, which base current is oriented similar to the base currents of the transistors P1 and P2 applied to the collector of transistor N1. This reduces the current inequality of the currents flowing through the transistors N1 and N2 caused by the current mirror circuit (P1, P2), which results in a reduction of the undesired offset voltage between the input and output terminals. If the currents of the current sources I1 and I3 are equal, a minimum offset voltage will be obtained, because then the base current of transistor P3 will be equal to the sum of the base currents of the transistors P1 and P2.

The further embodiment of an amplifier arrangement according to the invention represented in Fig. 3 differs from the embodiment represented in Fig. 2 in

the manner in which the current mirror circuit and, consequently, the level shifting circuit 6 are arranged. To the current mirror circuit a transistor P5 of the second conductivity type is added, which is coupled via its emitter and collector respectively, to the collector of the transistor P2 and the base of transistor N3 and the collector of transistor N2. The base of transistor P5 is coupled to the collectors of the transistors N1 and P1, so that Fig. 3 differs from Fig. 2 in this respect, because the bases of the transistors P1 and P2 are coupled to the collector of the transistor P2. Furthermore, a diode D1 is added to level shifting circuit 6, which diode may be arranged, for example, as a diode-coupled transistor. The diode D1 is inserted between the emitter of the transistor P3 on the one hand and the common terminal 5 and the current source I2 on the other. This embodiment illustrates a manner in which a reduction of the influence of the Early-effect is obtained when a different type of current mirror circuit is used. The voltage between the base and the collector of transistor N1 is now adjusted to practically zero volts by coupling the base of transistor N1 to the collector of transistor N1 via the base-emitter junction of transistor P3, the anode-cathode junction of diode D1, the emitter-base junction of transistor P1 and the emitter-base junction of transistor P5. With respect to the base-collector voltage of transistor N2 nothing has changed compared to Fig. 2.

The invention is not restricted to the embodiments shown. Within the scope of the appended claims a number of variations may be contemplated by those skilled in the art. For example, the differential pair may be arranged in various ways, for example, by means of Darlington transistors. Also the current mirror circuit may be implemented in more ways than the one shown; in which circuit the influence of the Early-effect can always be reduced by adapting one or both level shifting circuits. Also a substitution of the buffer stage comprising the third transistor with another buffer stage comprising, for example, a Darlington transistor, is one of the options whereas the object aimed at can be achieved by adapting one or both level shifting circuits. Furthermore, the amplifier arrangement according to the invention can be arranged to comprise transistors of a conductivity type opposite to the transistors shown in the Figures or also unipolar transistors or a combination of unipolar and bipolar transistors.

Claims

1. Amplifier arrangement being provided with a differential pair comprising at least a first (N1) and a second (N2) transistor of a first conductivity type, a first main electrode of the first transistor (N1) and a first main electrode of the second transistor (N2) being mutually coupled and coupled

pled to a first supply terminal (1) by means of a current source (I1), a control electrode of the first transistor (N1) being coupled to an input terminal (3) and a control electrode of the second transistor (N2) being coupled to an output terminal (4), with a current mirror comprising at least a third (P1) and a fourth (P2) transistor of a second conductivity type, a first main electrode of the third transistor (P1) and a first main electrode of the fourth transistor (P2) being mutually coupled and coupled to a second supply terminal (2) by means of a common terminal (5), a second main electrode of the third transistor (P1) being coupled to a second main electrode of the first transistor (N1) and a second main electrode of the fourth transistor (P2) being coupled to a second main electrode of the second transistor (N2), and with a buffer stage comprising at least a fifth transistor (N3) of the first conductivity type, a control electrode of the fifth transistor (N3) being coupled to the second main electrode of the second transistor (N2), a first main electrode of the fifth transistor (N3) being coupled to the output terminal (4) and a second main electrode of the fifth transistor (N3) being coupled to the second supply terminal (2), characterised in that the control electrode of the first transistor (N1) is coupled to the common terminal (5) by means of a first level shifting circuit (6) which provides a fixed voltage difference between the common terminal (5) and the control electrode of the first transistor (N1).

2. Amplifier arrangement as claimed in Claim 1, characterised in that the control electrode of the fifth transistor (N3) is coupled to the second main electrode of the second transistor (N2) by means of a second level shifting circuit (7).
3. Amplifier arrangement as claimed in Claim 1 or 2, characterised in that the first level shifting circuit (6) comprises a transistor (P3) of the second conductivity type and a current source (I2), a first main electrode of the transistor (P3) of the first level shifting circuit (6) being coupled to both the second supply terminal (2) by means of the current source (I2) of the first level shifting circuit (6) and to the common terminal (5), a second main electrode of the transistor (P3) of the first level shifting circuit (6) being coupled to the first supply terminal (1) and a control electrode of the transistor (P3) of the first level shifting circuit being coupled to the control electrode of the first transistor (N1).
4. Amplifier arrangement as claimed in Claim 2 or 3, characterised in that the second level shifting circuit (7) comprises a transistor (P4) of the second conductivity type and a current source (I3),

the manner in which the current mirror circuit and, consequently, the level shifting circuit 6 are arranged. To the current mirror circuit a transistor P5 of the second conductivity type is added, which is coupled via its emitter and collector respectively, to the collector of the transistor P2 and the base of transistor N3 and the collector of transistor N2. The base of transistor P5 is coupled to the collectors of the transistors N1 and P1, so that Fig. 3 differs from Fig. 2 in this respect, because the bases of the transistors P1 and P2 are coupled to the collector of the transistor P2. Furthermore, a diode D1 is added to level shifting circuit 6, which diode may be arranged, for example, as a diode-coupled transistor. The diode D1 is inserted between the emitter of the transistor P3 on the one hand and the common terminal 5 and the current source I2 on the other. This embodiment illustrates a manner in which a reduction of the influence of the Early-effect is obtained when a different type of current mirror circuit is used. The voltage between the base and the collector of transistor N1 is now adjusted to practically zero volts by coupling the base of transistor N1 to the collector of transistor N1 via the base-emitter junction of transistor P3, the anode-cathode junction of diode D1, the emitter-base junction of transistor P1 and the emitter-base junction of transistor P5. With respect to the base-collector voltage of transistor N2 nothing has changed compared to Fig. 2.

The invention is not restricted to the embodiments shown. Within the scope of the appended claims a number of variations may be contemplated by those skilled in the art. For example, the differential pair may be arranged in various ways, for example, by means of Darlington transistors. Also the current mirror circuit may be implemented in more ways than the one shown, in which circuit the influence of the Early-effect can always be reduced by adapting one or both level shifting circuits. Also a substitution of the buffer stage comprising the third transistor with another buffer stage comprising, for example, a Darlington transistor, is one of the options whereas the object aimed at can be achieved by adapting one or both level shifting circuits. Furthermore, the amplifier arrangement according to the invention can be arranged to comprise transistors of a conductivity type opposite to the transistors shown in the Figures or also unipolar transistors or a combination of unipolar and bipolar transistors.

Claims

1. Amplifier arrangement being provided with a differential pair comprising at least a first (N1) and a second (N2) transistor of a first conductivity type, a first main electrode of the first transistor (N1) and a first main electrode of the second transistor (N2) being mutually coupled and coupled

pled to a first supply terminal (1) by means of a current source (I1), a control electrode of the first transistor (N1) being coupled to an input terminal (3) and a control electrode of the second transistor (N2) being coupled to an output terminal (4), with a current mirror comprising at least a third (P1) and a fourth (P2) transistor of a second conductivity type, a first main electrode of the third transistor (P1) and a first main electrode of the fourth transistor (P2) being mutually coupled and coupled to a second supply terminal (2) by means of a common terminal (5), a second main electrode of the third transistor (P1) being coupled to a second main electrode of the first transistor (N1) and a second main electrode of the fourth transistor (P2) being coupled to a second main electrode of the second transistor (N2), and with a buffer stage comprising at least a fifth transistor (N3) of the first conductivity type, a control electrode of the fifth transistor (N3) being coupled to the second main electrode of the second transistor (N2), a first main electrode of the fifth transistor (N3) being coupled to the output terminal (4) and a second main electrode of the fifth transistor (N3) being coupled to the second supply terminal (2), characterised in that the control electrode of the first transistor (N1) is coupled to the common terminal (5) by means of a first level shifting circuit (6) which provides a fixed voltage difference between the common terminal (5) and the control electrode of the first transistor (N1).

2. Amplifier arrangement as claimed in Claim 1, characterised in that the control electrode of the fifth transistor (N3) is coupled to the second main electrode of the second transistor (N2) by means of a second level shifting circuit (7).
3. Amplifier arrangement as claimed in Claim 1 or 2, characterised in that the first level shifting circuit (6) comprises a transistor (P3) of the second conductivity type and a current source (I2), a first main electrode of the transistor (P3) of the first level shifting circuit (6) being coupled to both the second supply terminal (2) by means of the current source (I2) of the first level shifting circuit (6) and to the common terminal (5), a second main electrode of the transistor (P3) of the first level shifting circuit (6) being coupled to the first supply terminal (1) and a control electrode of the transistor (P3) of the first level shifting circuit being coupled to the control electrode of the first transistor (N1).
4. Amplifier arrangement as claimed in Claim 2 or 3, characterised in that the second level shifting circuit (7) comprises a transistor (P4) of the second conductivity type and a current source (I3),



a first main electrode of the transistor (P4) of the second level shifting circuit (7) being coupled to both the second supply terminal (2) by means of the current source (I3) of the second level shifting circuit (7) and to the control electrode of the fifth transistor (N3), a second main electrode of the transistor (P4) of the second level shifting circuit (7) being coupled to the first supply terminal (1) and a control electrode of the transistor (P4) of the second level shifting circuit (7) being coupled to the second main electrode of the second transistor (N2).

5. Amplifier arrangement as claimed in Claim 4, characterised in that the current source (I1) connected to the differential pair (N1,N2) and the current source (I3) belonging to the second level shifting circuit (7) are arranged for producing substantially equal currents.

Patentansprüche

1. Verstärkeranordnung mit einem Differenzpaar mit wenigstens einem ersten (N1) und einem zweiten (N2) Transistor eines ersten Leitungstyps, wobei eine erste Hauptelektrode des ersten Transistors (N1) und eine erste Hauptelektrode des zweiten Transistors (N2) miteinander gekoppelt und mittels einer Stromquelle (I1) mit einem ersten Versorgungsanschluß (1) gekoppelt sind, wobei eine Steuerelektrode des ersten Transistors (N1) mit einem Eingangsanschluß (3) gekoppelt ist und eine Steuerelektrode des zweiten Transistors (N2) mit einem Ausgangsanschluß (4) gekoppelt ist, mit einem Stromspiegel mit wenigstens einem dritten (P1) und einem vierten (P2) Transistor eines zweiten Leitungstyps, wobei eine erste Hauptelektrode des dritten Transistors (P1) und eine erste Hauptelektrode des vierten Transistors (P2) miteinander gekoppelt und mittels eines gemeinsamen Anschlusses (5) mit einem zweiten Versorgungsanschluß (2) gekoppelt sind, eine zweite Hauptelektrode des dritten (P1) Transistors mit einer zweiten Hauptelektrode des ersten Transistors (N1) gekoppelt ist und eine zweite Hauptelektrode des vierten Transistors (P2) mit einer zweiten Hauptelektrode des zweiten Transistors (N2) gekoppelt ist, und mit einer Pufferstufe mit wenigstens einem fünften Transistor (N3) des ersten Leitungstyps, wobei eine Steuerelektrode des fünften Transistors (N3) mit der zweiten Hauptelektrode des zweiten Transistors (N2) gekoppelt ist, eine erste Hauptelektrode des fünften Transistors (N3) mit dem Ausgangsanschluß (4) gekoppelt ist und eine zweite Hauptelektrode des fünften Transistors (N3) mit dem zweiten Versorgungsanschluß (2)

gekoppelt ist, dadurch gekennzeichnet, daß die Steuerelektrode des ersten Transistors (N1) mittels einer ersten Pegelverschiebeschaltung (6) mit dem gemeinsamen Anschluß (5) gekoppelt ist, wodurch eine feste Spannungsdifferenz zwischen dem gemeinsamen Anschluß (5) und der Steuerelektrode des ersten Transistors (N1) erhalten wird.

2. Verstärkeranordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Steuerelektrode des fünften Transistors (N3) mittels einer zweiten Pegelverschiebeschaltung (7) mit der zweiten Hauptelektrode des zweiten Transistors (N2) gekoppelt ist.
3. Verstärkeranordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die erste Pegelverschiebeschaltung (6) einen Transistor (P3) des zweiten Leitungstyps und eine Stromquelle (I2) umfaßt, wobei eine erste Hauptelektrode des Transistors (P3) der ersten Pegelverschiebeschaltung (6) mit sowohl dem zweiten Versorgungsanschluß (2) mittels der Stromquelle (I2) der ersten Pegelverschiebeschaltung (6) als auch mit dem gemeinsamen Anschluß (5) gekoppelt ist, wobei eine zweite Hauptelektrode des Transistors (P3) der ersten Pegelverschiebeschaltung (6) mit dem ersten Versorgungsanschluß (1) gekoppelt ist und eine Steuerelektrode des Transistors (P3) der ersten Pegelverschiebeschaltung mit der Steuerelektrode des ersten Transistors (N1) gekoppelt ist.
4. Verstärkeranordnung nach Anspruch 2 oder 3, dadurch gekennzeichnet, daß die zweite Pegelverschiebeschaltung (7) einen Transistor (P4) des zweiten Leitungstyps und eine Stromquelle (I3) umfaßt, wobei eine erste Hauptelektrode des Transistors (P4) der zweiten Pegelverschiebeschaltung (7) mit sowohl dem zweiten Versorgungsanschluß (2) mittels der Stromquelle (I3) der zweiten Pegelverschiebeschaltung (7) als auch mit der Steuerelektrode des fünften Transistors (N3) gekoppelt ist, wobei eine zweite Hauptelektrode des Transistors (P4) der zweiten Pegelverschiebeschaltung (7) mit dem ersten Versorgungsanschluß (1) gekoppelt ist und eine Steuerelektrode des Transistors (P4) der zweiten Pegelverschiebeschaltung (7) mit der zweiten Hauptelektrode des zweiten Transistors (N2) gekoppelt ist.
5. Verstärkeranordnung nach Anspruch 4, dadurch gekennzeichnet, daß die mit dem Differenzpaar (N1, N2) verbundene Stromquelle (I1) und die zu der zweiten Pegelverschiebeschaltung (7) gehörende Stromquelle (I3) zum Erzeugen nahezu



gleicher Ströme eingerichtet sind.

Revendications

1. Circuit amplificateur muni d'une paire différentielle comprenant au moins un premier transistor (N1) et un deuxième transistor (N2) présentant tous les deux un premier type de conductivité, une première électrode principale du premier transistor (N1) et une première électrode principale du deuxième transistor (N2) étant couplées mutuellement et couplées à une première borne d'alimentation (1) à l'aide d'une source de courant (I1), une électrode de commande du premier transistor (N1) étant couplée à une borne d'entrée (3) et une électrode de commande du deuxième transistor (N2) étant couplée à une borne de sortie (4), d'un miroir de courant comprenant au moins un troisième transistor (P1) et un quatrième transistor (P2) présentant tous les deux un deuxième type de conductivité, une première électrode principale du troisième transistor (P1) et une première électrode principale du quatrième transistor (P2) étant mutuellement couplées et couplées à une deuxième borne d'alimentation (2) à l'aide d'une borne commune (5), une deuxième électrode principale du troisième transistor (P1) étant couplée à une deuxième électrode principale du premier transistor (N1) et une deuxième électrode principale du quatrième transistor (P2) étant couplée à une deuxième électrode principale du deuxième transistor (N2), et d'un étage tampon comprenant au moins un cinquième transistor (N3) du premier type de conductivité, une électrode de commande du cinquième transistor (N3) étant couplée à la deuxième électrode principale du deuxième transistor (N2), une première électrode principale du cinquième transistor (N3) étant couplée à la borne de sortie (4) et une deuxième électrode principale du cinquième transistor (N3) étant couplée à la deuxième borne d'alimentation (2), caractérisé en ce que l'électrode de commande du premier transistor N1 est couplée à la borne commune (5) à l'aide d'un premier circuit de décalage de niveau (6), qui fournit une différence de tension fixe entre la borne commune (5) et l'électrode de commande du premier transistor (N1).
2. Circuit amplificateur selon la revendication 1, caractérisé en ce que l'électrode de commande du cinquième transistor (N3) est couplée à la deuxième électrode principale du deuxième transistor (N2) à l'aide d'un deuxième circuit de décalage de niveau (7).

3. Circuit amplificateur selon la revendication 1 ou 2, caractérisé en ce que le premier circuit de décalage de niveau (6) est muni d'un transistor (P3) du deuxième type de conductivité et d'une source de courant (I2), une première électrode principale du transistor (P3) du premier circuit de décalage de niveau (6) étant couplée à tant la deuxième borne d'alimentation (2) à l'aide de la source de courant (I2) du premier circuit de décalage de niveau (6) qu'à la borne commune (5), une deuxième électrode principale du transistor (P3) du premier circuit de décalage de niveau (6) étant couplée à la première borne d'alimentation (1) et une électrode de commande du transistor (P3) du premier circuit de décalage de niveau étant couplée à l'électrode de commande du premier transistor (N1).
4. Circuit amplificateur selon la revendication 2 ou 3, caractérisé en ce que le deuxième circuit de décalage de niveau (7) est muni d'un transistor (P4) du deuxième type de conductivité et d'une source de courant (I3), une première électrode principale du transistor (P4) du deuxième circuit de décalage de niveau (7) étant couplée à tant la deuxième borne d'alimentation (2) à l'aide de la source de courant (I3) du deuxième circuit de décalage de niveau (7) qu'à l'électrode de commande du cinquième transistor (N3), une deuxième électrode principale du transistor (P4) du deuxième circuit de décalage de niveau (7) étant couplée à la première borne d'alimentation (1) et une électrode de commande du transistor (P4) du deuxième circuit de décalage de niveau (7) étant couplée à la deuxième électrode principale du deuxième transistor (N2).
5. Circuit amplificateur selon la revendication 4, caractérisé en ce que la source de courant (I1) connectée à la paire différentielle (N1, N2) et la source de courant (I3) appartenant au deuxième circuit de décalage de niveau (7) sont conçues pour fournir des courants pratiquement égaux.

