Abstract

A Global Planarization Method For Inter Level Dielectric Layers Using IDL Blocks

The present invention provides a method of manufacturing of planarizing an insulating layer using a reduced size reversed interconnect mask and an etch stop layer. Spaced interconnections 22 are provided over the semiconductor substrate 10. An etch stop layer 26 is formed over the raised portions 22. A dielectric layer 30 is formed over the etch stop layer 26. The top of the first dielectric layer 30 over the valley 23 is about coplanar with the top of the etch stop layer 26 over the raised portion 22. A reduced size, reverse interconnect (photoresist) mask 40 is formed over the first dielectric layer 30. The reduced size, reverse interconnect mask 40 covers portions of the valleys 23 between the raised portions. The first dielectric layer 30 is etched using the reverse interconnect mask 40 as an etch mask leaving dielectric blocks 30A over the narrow valleys 23. The dielectric blocks 30A fill in the valleys 23 between the raised portions thereby eliminating the need for a global planarization step. A second dielectric layer formed over the etch stop layer 26 and blocks 30A thereby providing the dielectric layer with a planar top surface.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)