What is claimed is:

1. A memory module comprising:

a plurality of semiconductor memory devices associated with a same module board, each of the plurality of semiconductor memory devices including a memory cell array that includes a plurality of dynamic memory cells, the plurality of semiconductor memory devices configured to simultaneously perform a training operation, the plurality of semiconductor memory devices including a reception interface circuit configured to,

perform the training operation to search for selected equalization coefficients of an equalizer based on a training pattern from a memory controller, and

transmit a training information signal to the memory controller in a training mode in response to a training command from the memory controller, the training information signal including the selected equalization coefficients.

2. The memory module of claim 1, wherein the plurality of semiconductor memory devices are configured to perform the training operation simultaneously by rank unit of the plurality of semiconductor memory devices.

3. The memory module of claim 1 or claim 2, wherein the reception interface circuit comprises:

the equalizer configured to generate an equalizer output pattern by equalizing the training pattern based on control equalization coefficients in the training mode; and

a self-training circuit configured to provide the control equalization coefficients to the equalizer, the self-training circuit configured to,

generate an error counting value that indicates a difference between the equalizer output pattern and a reference pattern,

adaptively adjust searching equalization coefficients to provide the control equalization coefficients to the equalizer based on the error counting value and a reference value, wherein

the equalizer utilizes the searching equalization coefficients to search for the selected equalization coefficients.

4. The memory module of claim 3, wherein the equalizer includes at least one of a continuous time linear equalizer, a feed-forward equalizer and a decision feedback equalizer.

5. The memory module of claim 3, wherein the equalizer includes a feed-forward equalizer and a decision feedback equalizer connected to the feed-forward equalizer.

6. The memory module of any one of claims 3 to 5, wherein the self-training circuit is configured to,

store the reference pattern in a register associated with the self-training circuit,

generate a comparison signal based on the equalizer output pattern and the reference pattern, and

output the error counting value in response to the comparison signal.

7. The memory module of any one of claims 3 to 5, wherein the self-training circuit is configured to,

output the reference pattern via a replica path in response to the training pattern, the replica path replicating a path that provides the equalizer output pattern while being independent from an external influence,

generate a comparison signal based on the equalizer output pattern and the reference pattern, and

output the error counting value in response to the comparison signal.

8. The memory module of any one of claims 3 to 7, wherein the self-training circuit is configured to,

output an adaptive coefficient control signal based on the error counting value and the reference value,

provide the equalizer with the searching equalization coefficients as the control equalization coefficients in response to the adaptive coefficient control signal such that the adaptive coefficient control signal instructs a controller associated with the self-training circuit to reduce a difference between the error counting value and the reference value, and

output the searched equalization coefficient as the selected equalization coefficients in response to the difference between the error counting value and the reference value reaching a lower threshold value.

9. The memory module of claim 8, wherein the controller is configured to output a flag signal including a pass/fail bit and a memory identifier bit when the adaptive coefficient control signal indicates the difference between the error counting value and the reference value reaches the lower threshold value, the pass/fail bit indicating whether the training operation is successful for a corresponding one of the plurality of semiconductor memory devices and the

memory identifier bit indicating the corresponding one of the plurality of semiconductor memory devices.

10. The memory module of claim 8 or claim 9, wherein the self-training circuit is configured to reduce the difference between the error counting value and the reference value using one of a zero forcing algorithm, a least mean square algorithm and a recursive least square algorithm.

11. The memory module of any one of claims 3 to 10, wherein the reception interface circuit further includes a demultiplexer configured to,

provide the self-training circuit with the equalizer output pattern from the equalizer in the training mode, and

provide an internal circuit with an output of the equalizer in response to data received from the memory controller in a normal mode, wherein

the memory module switches between the training mode and the normal mode in response to a mode signal.

12. The memory module of any one of claims 3 to 11, wherein the self-training circuit further includes a register configured to store the control equalization coefficients, and the self-training circuit is configured to transmit the control equalization coefficients as the selected equalization coefficients to the memory controller in response to a difference between the error counting value and the reference value reaching a lower threshold value.

13. The memory module of any one of claims 3 to 8, wherein each of the semiconductor memory devices is configured to:

receive the selected equalization coefficients and a flag signal in response to a difference between the error counting value and the reference value reaching a lower threshold value, the flag signal including a pass/fail bit and a memory identifier bit, the pass/fail bit indicating a pass or a fail of the training operation and the memory identifier bit identifying a corresponding semiconductor memory device; and

transmit, to the memory controller, the training information signal that further includes the selected equalization coefficients and the flag signal.

14. The memory module of any one of claims 3 to 8, wherein each of the semiconductor memory devices further comprises a signal merger, and wherein the signal merger is configured to:

receive the control equalization coefficients as the selected equalization coefficients when a difference between the error counting value and the reference value becomes a minimum value,

receive a flag signal including a pass/fail bit and a memory identifier bit, the pass/fail bit indicating whether the training operation is successful for a corresponding one of the plurality of semiconductor memory devices and the memory identifier bit identifying the corresponding one of the plurality of semiconductor memory devices, and

merge the training information signal with the selected equalization coefficients and the flag signal to generate a merged training information signal, wherein the memory module further comprises:

a control device configured to receive the merged training information signal from each of the semiconductor memory devices, and to transmit the merged training information signal to the memory controller.

15. The memory module of claim 14, wherein the control device includes a memory configured to store the merged training information signal for each of the semiconductor memory devices.

16. The memory module of any one of claims 3 to 15, wherein the reception interface circuit is further configured to,

compare the training pattern with a reference voltage to output a comparison signal,

generate the reference voltage in response to a control code,

search for the control code corresponding to a desired voltage level of the reference voltage in the training mode, and

output the control code in a normal mode.

17. The memory module of any one of claims 1 to 16, wherein each of the semiconductor memory devices further comprises:

a temperature sensor configured to,

sense an operating temperature of a corresponding semiconductor memory device; and

transmit a training request signal to the memory controller in response to the operating temperature being greater than a reference temperature, the training request

signal requesting the training operation of the corresponding semiconductor memory device, wherein

the reception interface circuit of each of the plurality of semiconductor memory devices is configured to set on-die termination resistance of equally with respect to each other in the training mode, and

each of the semiconductor memory devices includes a double data rate 5 (DDR5) synchronous dynamic random access memory (SDRAM).

18. A memory system comprising:

a memory controller; and

a memory module including a plurality of semiconductor memory devices, each of the plurality of semiconductor memory devices including a memory cell array that includes a plurality of dynamic memory cells, the plurality of semiconductor memory devices configured to simultaneously perform a training operation, the plurality of semiconductor memory devices including a reception interface circuit configured to,

perform a training operation to search for selected equalization coefficients of an equalizer based on a training pattern received from the memory controller, and

transmit a training information signal to the memory controller in a training mode in response to a training command from the memory controller, the training information signal including the selected equalization coefficients.

19. The memory system of claim 18, wherein the plurality of semiconductor memory devices is configured to,

merge the training information signal with selected equalization coefficients and a flag signal to generate a merged training information signal, the flag signal including a pass/fail bit and a memory identifier bit, the pass/fail bit indicating whether the training operation is successful for a corresponding one of the plurality of semiconductor memory devices and the memory identifier bit indicating the corresponding one of the plurality of semiconductor memory devices, and

transmit the training information signal to each of the plurality of semiconductor memory devices, wherein

the memory controller includes a training information storage table configured to store the merged training information signal for each of the semiconductor memory devices.

20. A method of operating a memory module, the memory module including a plurality of semiconductor memory devices, each of the plurality of semiconductor memory devices including a memory cell array that includes a plurality of dynamic memory cells, the method comprising:

determining, by each of the semiconductor memory devices operating in a training mode, selected equalization coefficients of an equalizer based on a training pattern received from a memory controller;

transmitting, by each of the plurality semiconductor memory devices, the selected equalization coefficients to the memory controller; and

performing, by each of the plurality of semiconductor memory devices operating in a normal mode, a memory operation on data received from the memory controller using the selected equalization coefficients.