CLAIMS:

1. An integrated circuit device, comprising:

a wafer; and

an interconnect layer at least partially covering the wafer, the interconnect layer comprising:

a low radio frequency (RF) loss primary coating that forms a main portion of the interconnect layer;

a trench formed in and extending through a full thickness of the primary coating to expose a feature that is positioned on the wafer;

a high aspect ratio patternable secondary coating within the trench; and

a via formed in the secondary coating, wherein an aspect ratio of the via is greater than an aspect ratio of the trench.

2. The integrated circuit device of claim 1, wherein the primary coating has a different composition than the secondary coating.

3. The integrated circuit device of claim 2, wherein the primary coating is a benzocyclobutene (BCB)-based polymer.

4. The integrated circuit device of claim 2, wherein the secondary coating is a high contrast, epoxy-based, negative photoresist possessing an average of eight epoxide functional groups per moiety (SU-8).

5. The integrated circuit device of claim 1, wherein an RF loss tangent of the primary coating is less than an RF loss tangent of the secondary coating.

6. The integrated circuit device of claim 1, wherein an effective thickness of the secondary coating is at least as thick as a thickness of the primary coating.

7. The integrated circuit device of claim 1, wherein the aspect ratio of the via is greater than 0.6.

8. The integrated circuit device of claim 7, wherein the aspect ratio of the via is greater than 1.0.

9. The integrated circuit device of claim 1, wherein a diameter of the via is less than 60 micrometers (μm); and wherein a thickness of the primary coating is greater than 20 μm.

10. The integrated circuit device of claim 9, wherein the diameter of the via is less than 20 μm.

11. An integrated circuit device comprising:

a wafer;

a low radio frequency (RF) loss primary coating at least partially covering the wafer;

a trench formed in the primary coating to expose a feature that is positioned on the wafer;

a high aspect ratio patternable secondary coating within the trench; and

a via formed in the secondary coating and bounded by sidewalls of the secondary coating, wherein an aspect ratio of the via is greater than an aspect ratio of the trench.

12. The integrated circuit device of claim 11, wherein the primary coating has a different composition than the secondary coating.

13. The integrated circuit device of claim 12, wherein the primary coating is a benzocyclobutene (BCB)-based polymer.

14. The integrated circuit device of claim 12, wherein the secondary coating is a high contrast, epoxy-based, negative photoresist possessing an average of eight epoxide functional groups per moiety (SU-8).

15. The integrated circuit device of claim 11, wherein the integrated circuit device is a

monolithic microwave integrated circuit (MMIC).

16. The integrated circuit device of claim 11, wherein the integrated circuit device has an operating frequency that is greater than 10 GHz.

17. A method of reducing radio frequency (RF) loss from an integrated circuit device, the method comprising:

depositing a low RF loss primary coating onto an integrated circuit device wafer;

forming a trench that extends through a full thickness the primary coating to expose a feature that is positioned on the wafer;

depositing a high aspect ratio patternable secondary coating into the trench; and

forming a via in the secondary coating.

18. The method of claim 17, wherein the primary coating has a different composition than the secondary coating.

19. The method of claim 18, wherein the primary coating is a benzocyclobutene (BCB)-based polymer; and wherein the secondary coating is a high contrast, epoxy-based, negative photoresist possessing an average of eight epoxide functional groups per moiety (SU-8).

20. The method of claim 17, and further comprising:

operating the integrated circuit device at a frequency greater than 10 GHz.