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DIVERSITY RECEIVER

FIELD OF THE INVENTION

This invention relates to a diversity receiver, and more particularly to, a diversity receiver where information of antenna's received signal strength is obtained based on one received signal strength indication(RSSI) voltage selected from some RSSI voltages.

BACKGROUND OF THE INVENTION

Conventional diversity receivers comprise a plurality of receivers, each of which provided with a receiving antenna, which output received signal strength indication(hereinafter referred to as 'RSSI') voltages, peak hold circuits for holding the respective RSSI voltages, analog-to-digital converters(hereinafter referred to as 'A/D converter(s)') for digital-converting the outputs of the peak hold circuits, and a comparator for comparing the RSSI voltages. The respective receivers also outputs antenna input system signals used as received data. The outputs of the A/D converters are input to a main circuit, where information of antenna's received signal strength is obtained based on the outputs.

In this diversity receiver, peak hold values of the RSSI voltages are obtained through the receivers, converted into digital signals by the A/D converters, then input to the main circuit, where information of antenna's received signal strength is obtained. On the other hand, the comparator determines which of the RSSI voltages is larger by comparative operation, and it outputs information of maximum antenna input system according to

REPLACED SHEETS		SG
☒ Description	: paged1..... to paged8.....	
☒ Claim(s)	: paged9..... to paged10.....	
☒ Drawing(s)	: paged1..... to paged5.....	
☒ Abstract	: paged11..... to paged12.....	

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that determination.

However, in the conventional diversity receiver, there is a problem that the peak hold circuit and the A/D converter are necessary to process the RSSI voltage output from each of the receivers while only one maximum RSSI voltage is used as a detection data. Therefore, when the number of the receivers is increased to more than two, the number of the peak hold circuits and A/D converters has to be further increased. Namely, the integrated circuit must be so much enlarged, and it will be therefore complicated and costly.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the invention to provide a diversity receiver whose circuit composition is effectively simplified.

According to the invention, a diversity receiver, comprises:
a plurality of receivers, each of which having a receiving antenna;

a maximum received signal strength indication voltage selector circuit which outputs a maximum received signal strength indication voltage to be selected from received signal strength indication voltages to be obtained by the plurality of receivers;
and

a received signal strength information processing circuit which processes information of antenna's received signal strength based on the maximum received signal strength indication voltage to be input from the maximum received signal strength indication voltage selector circuit.



BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be explained in more detail in conjunction with the appended drawings, wherein:

FIG.1 is a block diagram showing main part of a conventional diversity receiver,

FIG.2 is a block diagram showing main part of a diversity receiver in a preferred embodiment according to the invention,

FIG.3 is a circuit diagram showing the details of a maximum RSSI selector circuit 109 in FIG.2,

FIG.4 is a circuit diagram showing the details of a maximum RSSI identification signal generating circuit 114 in FIG.2,

FIG.5 shows a truth table for identification signals A, B in FIG.4,

FIG.6 is a block diagram showing the details of a four-terminal analog switching circuit 115 in FIG.2,

FIG.7 is a circuit diagram showing another maximum RSSI selector circuit adaptable to the diversity receiver in FIG.2, and

FIG.8 is a block diagram showing another four-terminal analog switching circuit adaptable to the diversity receiver in FIG.2.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before explaining a diversity receiver in the preferred embodiment of the invention, the aforementioned conventional diversity receiver will be explained in FIG.1.

FIG.1 shows main part of a conventional diversity receiver,



where 701 and 709 are receiving antennas provided for receivers 702 and 710, respectively, 703 and 711 are received signal strength indication(hereinafter referred to as 'RSSI') voltages to be output from the receivers 702 and 710, respectively, 704 and 712 are peak hold circuits for the RSSI voltages, 705 and 713 are analog-to-digital converters(hereinafter referred to as 'A/D converter(s)') for digital-converting the outputs of the peak hold circuits 704 and 712, and 706 and 714 are outputs of the A/D converters which are input to a main circuit(not shown), where information of antenna's received signal strength is obtained based on the outputs. Also, 707 and 715 are antenna input system signals used as received data, 717 is a comparator for comparing the RSSI voltages, and 718 is an output of the comparator 717.

Next, a diversity receiver in the preferred embodiment of the invention will be explained in FIG.2.

In FIG-2, 101, 102, 103 and 104 are RSSI voltages output individually from four receivers 121, 122, 123 and 124 with receiving antennas 131, 132, 133 and 134, respectively, 105, 106, 107 and 108 are antenna input system signals which are radio-frequency data signals received by the receivers 121 to 124, 109 is a maximum RSSI(received signal strength indication) selector circuit which selects one maximum RSSI voltage from the RSSI voltages 101 to 104, 111 is a peak hold circuit which holds a peak value of the maximum RSSI voltage, 112 is an A/D converter which digital-converts the peak hold voltage and 113 is a 8-bit digital output which holds information of antenna's received signal strength. A received signal strength information



processing circuit 118 is composed of the peak hold circuit 111, the A/D converter 112 and a main circuit where the information of antenna's received signal strength is input.

On the other hand, 114 is a maximum RSSI identification signal generating circuit which outputs a digital signal for identifying a maximum antenna input system based on a 3-bit signal as RSSI selection information output from the maximum RSSI selector circuit 109. 115 is a four-terminal analog switching circuit which switches into and outputs one of the antenna input system signals 105 to 108 as a maximum antenna input system signal 116 based on a 2-bit output of the maximum RSSI identification signal generating circuit 114.

The maximum RSSI selector circuit 109 will be detailed in FIG.3. In this circuit, the two RSSI voltages 101, 102 are compared by a comparator 205, and then one of the RSSI voltages 101, 102 which has a greater level is output selectively by switching an analog switch 208 according to the result of that comparison. On the other hand, the other two RSSI voltages 103, 104 are compared by a comparator 206, and then one of the RSSI voltages 103, 104 which has a greater level is output selectively by switching an analog switch 209 according to the result of that comparison.

Then, the two RSSI voltages output through the analog switches 208, 209 are compared by a comparator 207, and then one of the two RSSI voltages which has a greater level is output selectively as the maximum RSSI voltage by switching an analog switch 210 according to the result of that comparison. In FIG.3, a, b and c are comparison result outputs(3 bits) from the



comparators 205, 206 and 207.

The maximum RSSI identification signal generating circuit 114 will be detailed in FIG.4. 251 is a NAND circuit where the two comparison result outputs a and c are input, 252 is an inverter for inverting the comparison result output c, 253 is a NAND circuit where the inverted output and the comparison result output b are input, and 254 is an AND circuit which conducts AND operation between the outputs of the NAND circuits 251, 253. The AND circuit 254 outputs an output A and the inverter 252 outputs an output B. FIG.5 is a truth table of the outputs A, B to the RSSI voltages.

FIG.6 shows the details of the four-terminal analog switching circuit 115, where a maximum one of the antenna input system signals 105 to 108 is selected by an analog switch 271 based on the outputs A, B and is output as the maximum antenna input signal 116.

As described above, in the diversity receiver in this embodiment, firstly, the maximum RSSI selector circuit 109 selects the maximum one of the four RSSI voltages output from the receivers 121 to 124 and outputs it as the maximum RSSI voltage 110. In detail, the four RSSI voltages are input to the comparators 205, 206, and then the greater ones of them are selected by the analog switches 208, 209 according to the comparison results and are again input to the comparator 207, and then the greater one is selected by the analog switch 210 according to the comparison result to output the maximum RSSI voltage 110. Namely, the RSSI voltages are compared in a tournament manner to obtain the maximum RSSI voltage.



Then, the maximum RSSI voltage 110 obtained is input through the peak hold circuit 111, A/D converter 112 as a 8-bit digital signal to the main circuit 117, where information of antenna's received signal strength is obtained based on the digital signal.

On the other hand, in the maximum RSSI identification signal generating circuit 114, the outputs a, b and c(3 bits) of the maximum RSSI selector circuit 109 as shown in FIG.3 are input to the logical circuit as shown in FIG.4, and then the 2-bit identification data A, B corresponding to the RSSI voltages as shown in FIG.5 are obtained. Also, the antenna input system signals 105 to 108 as the radio-frequency data signals are input to the four-terminal analog switching circuit 115. In the four-terminal analog switching circuit 115, the maximum antenna input system signal 116 which is the maximum one of the antenna input system signals 105 to 108 is selected according to the 2-bit identification data A, B and is output to a demodulator(not shown), where reception data is produced and output.

Thus, by selecting the maximum RSSI voltage to be used as data from the four RSSI voltages, the number of peak hold circuits and A/D converters, which were conventionally necessary to provide corresponding to the number of receivers, can be reduced. Namely, only the peak hold circuit 111 and A/D converter 113 are necessary. Therefore, the number of parts can be reduced, the entire circuit can be simplified, the number of interfaces to LSI can be reduced and the manufacturing cost can be reduced.

Meanwhile, as the four-terminal analog switching circuit 115, a double-circuit type is generally used other than the



single-circuit type as shown in FIG.6. In such a case, a maximum RSSI selector circuit 109A, where the analog switch 210 of the maximum RSSI selector circuit 109 as shown in FIG.3 is omitted, is used to provide outputs a, b and c(3 bits) as shown in FIG.7. Based on the outputs, the maximum RSSI identification signal generating circuit 114 generates the maximum RSSI identification signals A, B(2 bits).

On the other hand, based on the maximum RSSI identification signals A, B, a four-terminal analog switching circuit 115A, which has a first analog switch 151 and a second analog switch 152, as shown in FIG.8, outputs the maximum RSSI voltage 110 selected from the RSSI voltages 101 to 104 and outputs the maximum antenna input system signal 116 selected from the antenna input system signals 105 to 108. Thus, by using the four-terminal analog switching circuit 115A, the electric power loss can be saved since the RSSI voltage need only one analog switch.

Although the invention has been described with respect to specific embodiment for complete and clear disclosure, the appended claims are not to be thus limited but are to be construed as embodying all modification and alternative constructions that may be occurred to one skilled in the art which fairly fall within the basic teaching here is set forth.





Claims

1. A diversity receiver, comprising:

a plurality of receivers, each of which having a receiving antenna;

a maximum received signal strength indication voltage selector circuit which outputs a maximum received signal strength indication voltage to be selected from received signal strength indication voltages to be obtained by said plurality of receivers; and

a received signal strength information processing circuit which processes information of antenna's received signal strength based on said maximum received signal strength indication voltage to be input from said maximum received signal strength indication voltage selector circuit.

2. A diversity receiver, according to claim 1, wherein:

said maximum received signal strength indication voltage selector circuit comprises a plurality of comparators, each of which comparing two of said received signal strength indication voltages in a tournament manner, and a plurality of switches, each of which outputting greater one of said two received signal strength indication voltages according to a comparison result of said corresponding comparator and finally outputting said maximum received signal strength indication voltage through said tournament-manner comparative operation.

3. A diversity receiver, according to claim 2, further



comprising:

a maximum received signal strength indication voltage identification signal generating circuit which generates an identification signal of said maximum received signal strength indication voltage based on outputs of said comparators of said maximum received signal strength indication voltage selector circuit; and

an analog switching circuit which outputs a maximum antenna input system signal to be selected from antenna input system signals received by said receiving antenna based on said identification signal to be generated by said maximum received signal strength indication voltage identification signal generating circuit.

4. A diversity receiver, according to claim 3, wherein:

said analog switching circuit comprises a first analog switch which outputs said maximum received signal strength indication voltage to be selected from said plurality of received signal strength indication voltages based on said identification signal to be generated by said maximum received signal strength indication voltage identification signal generating circuit, and a second analog switch which outputs said maximum antenna input system signal to be selected from said antenna input system signals.



DIVERSITY RECEIVER

ABSTRACT

Disclosed is a diversity receiver which has: a plurality of receivers (121, 122, 123 and 124), each of which having a receiving antenna (131, 132, 133 and 134); a maximum received signal strength indication voltage selector circuit (109) which outputs a maximum received signal strength indication voltage to be selected from received signal strength indication voltages to be obtained by said plurality of receivers (121, 122, 123 and 124); and a received signal strength information processing circuit (118) which processes information of antenna's received signal strength based on said maximum received signal strength indication voltage to be input from said maximum received signal strength indication voltage selector circuit (109).

Fig. 2

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FIG. 1 PRIOR ART

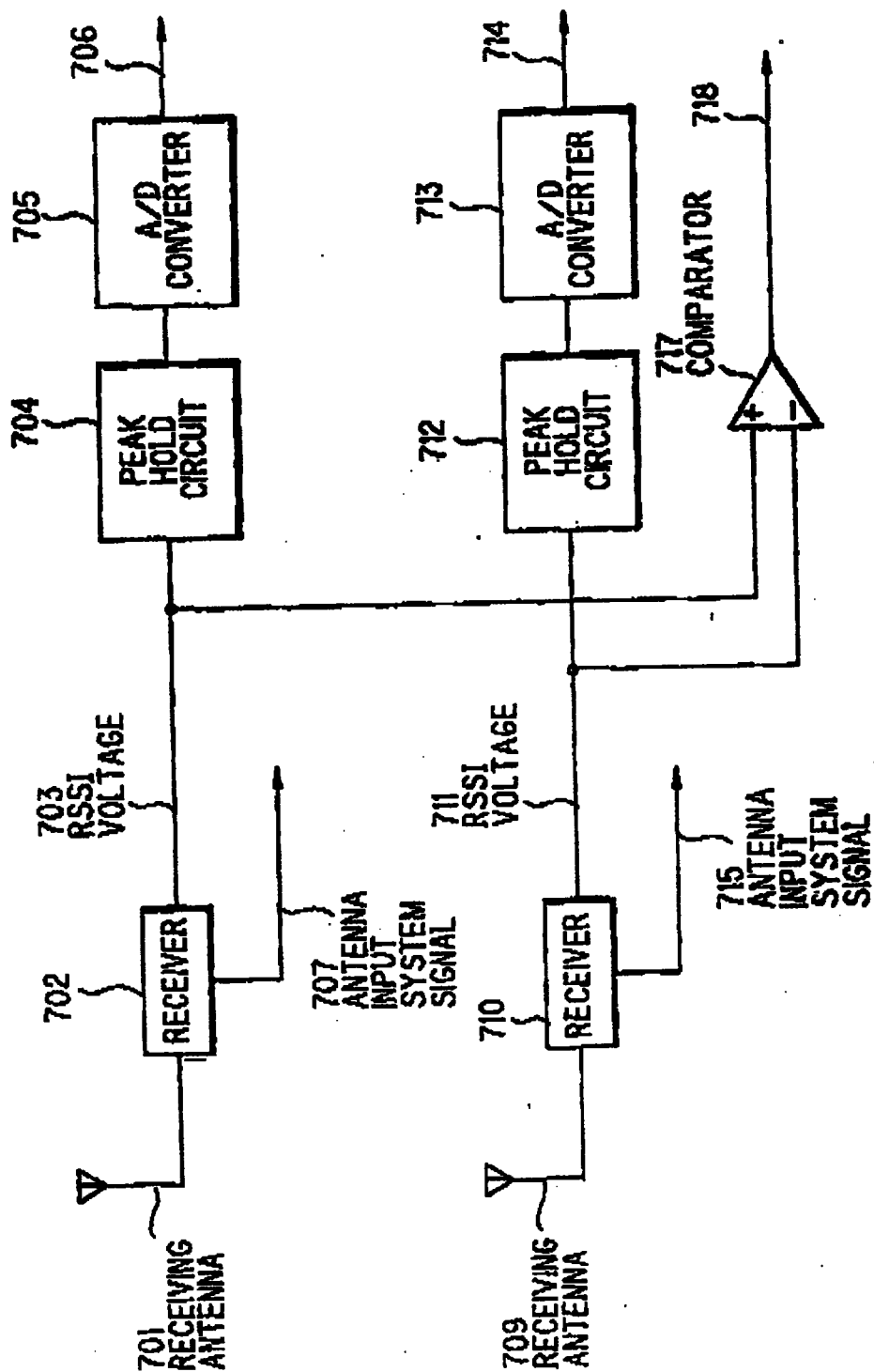


FIG. 2

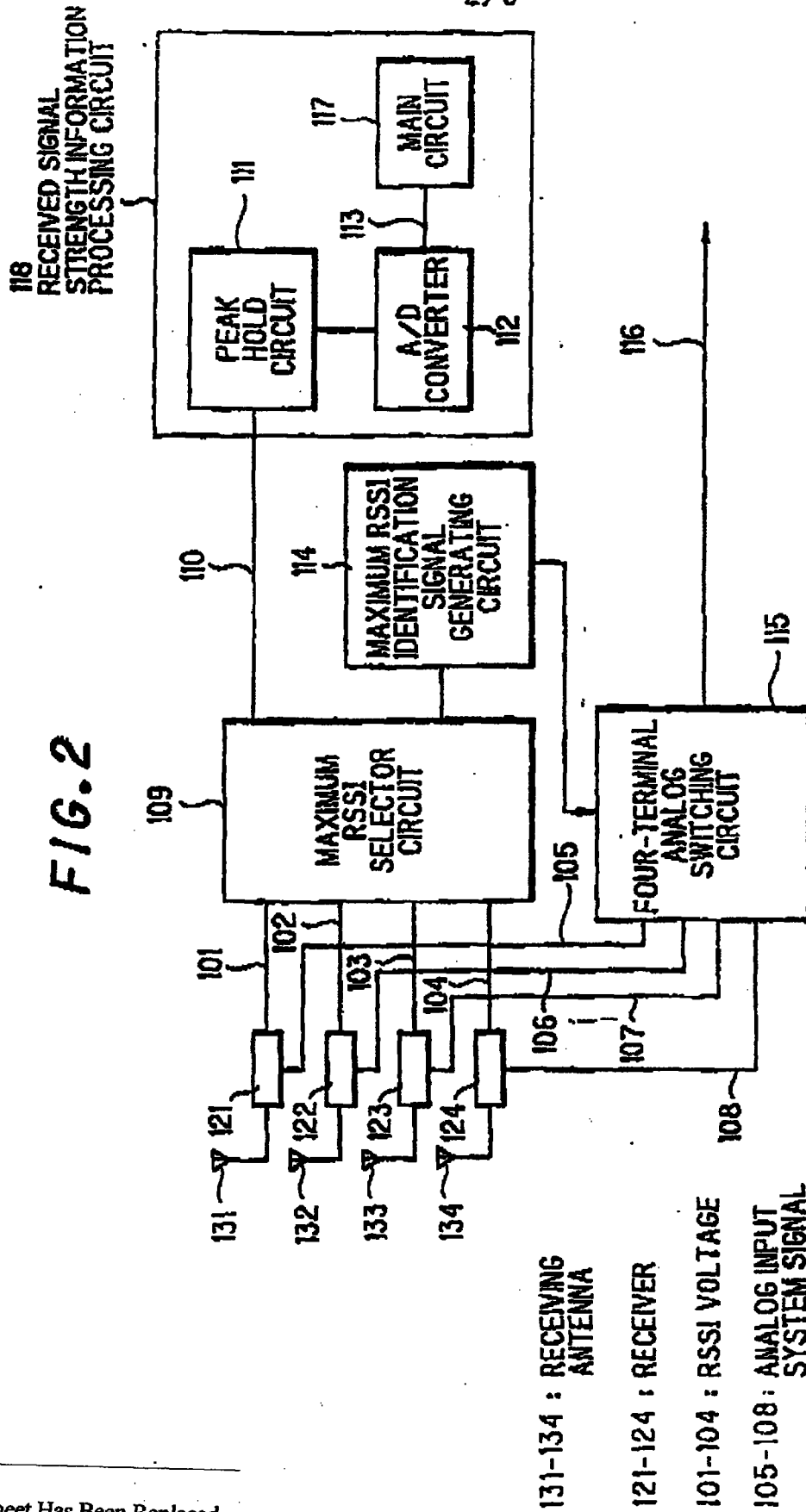


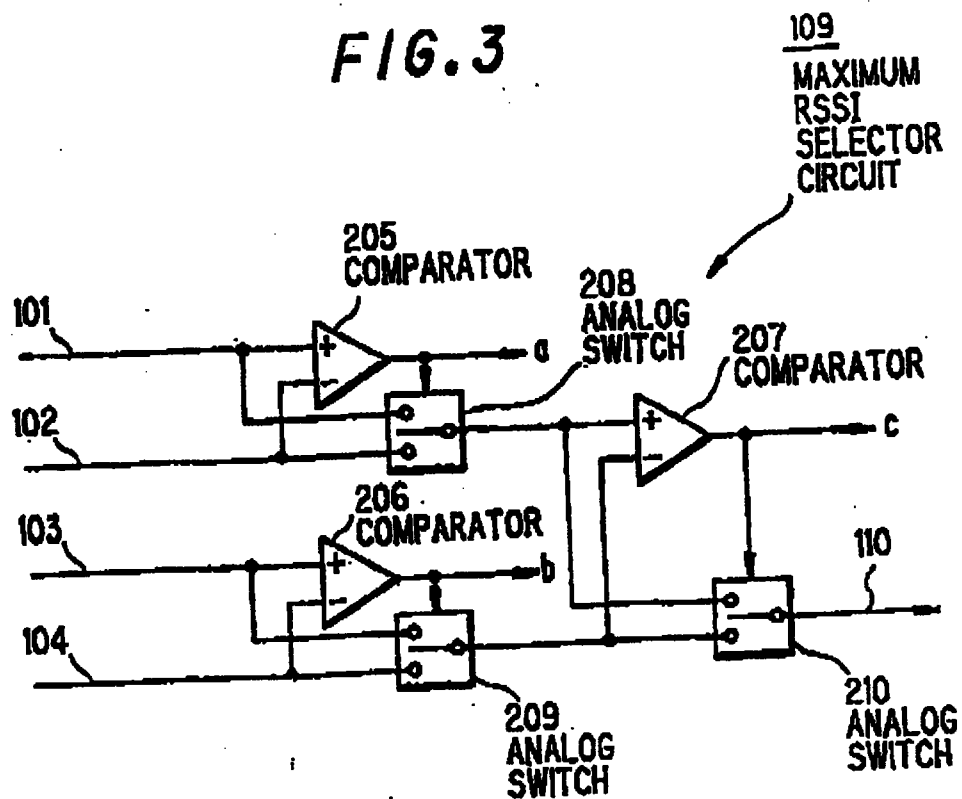
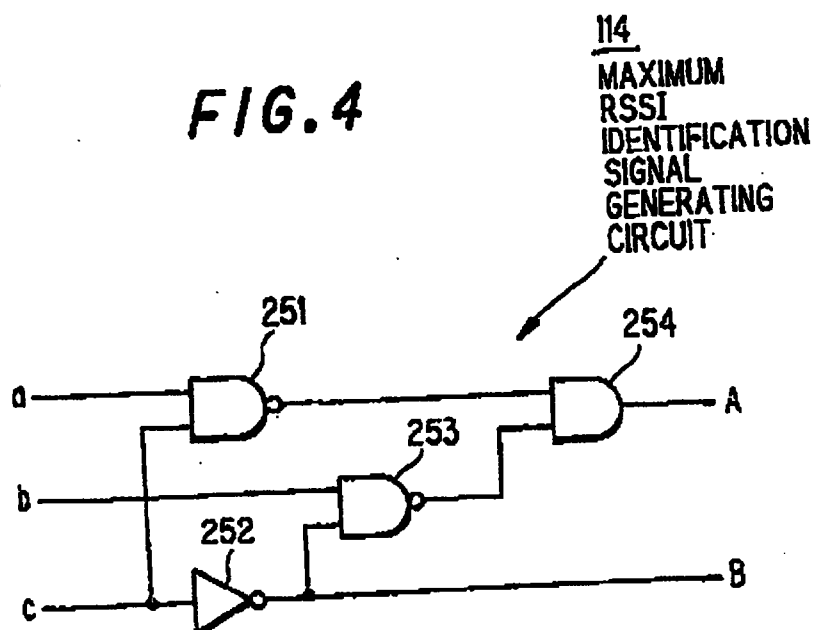
FIG. 3**FIG. 4**

FIG. 5

MAXIMUM SYSTEM	B	A
101	0	0
102	0	1
103	1	0
104	1	1

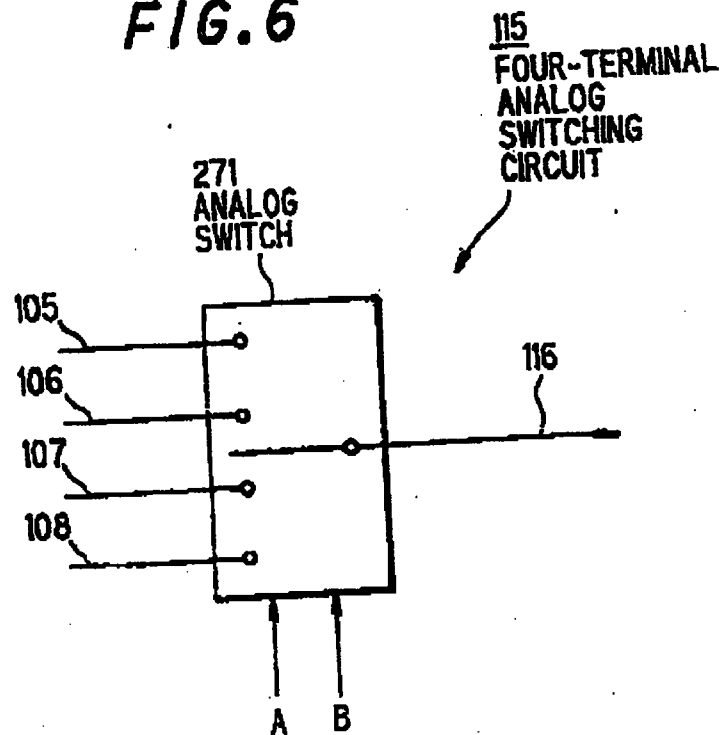
FIG. 6

FIG. 7

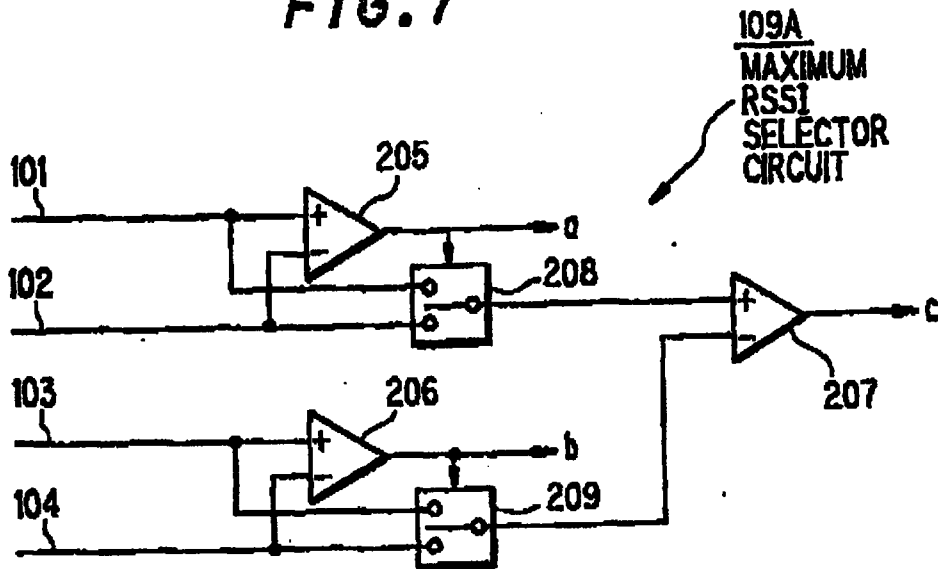
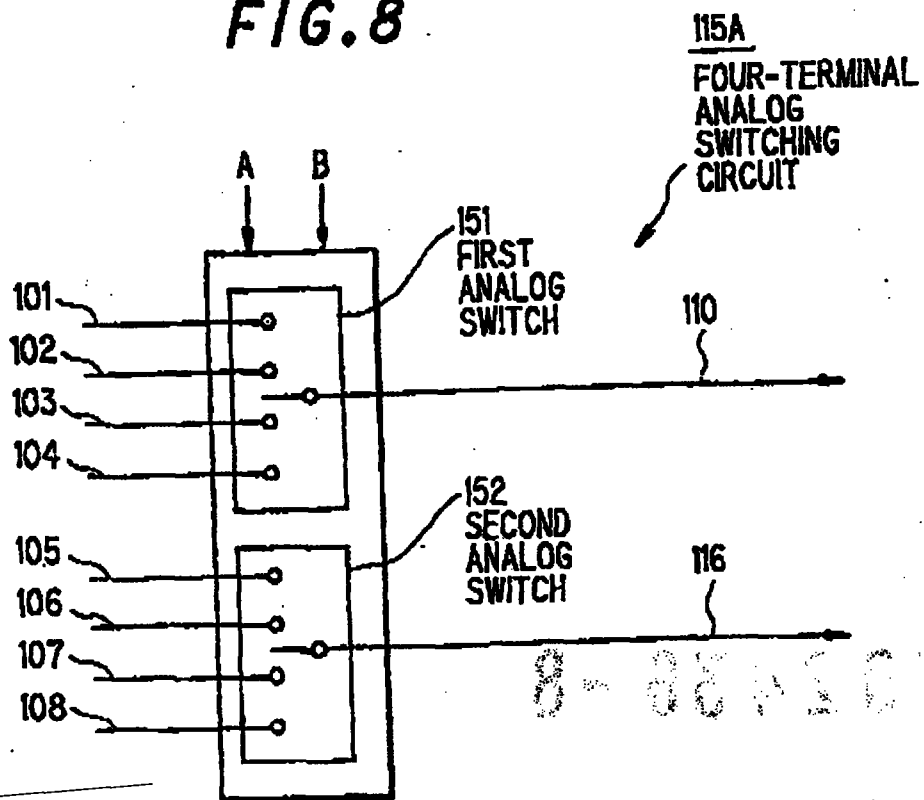


FIG. 8



DIVERSITY RECEIVER

FIELD OF THE INVENTION

This invention relates to a diversity receiver, and more particularly to, a diversity receiver where information of antenna's received signal strength is obtained based on one received signal strength indication(RSSI) voltage selected from some RSSI voltages.

BACKGROUND OF THE INVENTION

Conventional diversity receivers comprise a plurality of receivers, each of which provided with a receiving antenna, which output received signal strength indication(hereinafter referred to as 'RSSI') voltages, peak hold circuits for holding the respective RSSI voltages, analog-to-digital converters(hereinafter referred to as 'A/D converter(s)') for digital-converting the outputs of the peak hold circuits, and a comparator for comparing the RSSI voltages. The respective receivers also outputs antenna input system signals used as received data. The outputs of the A/D converters are input to a main circuit, where information of antenna's received signal strength is obtained based on the outputs.

In this diversity receiver, peak hold values of the RSSI voltages are obtained through the receivers, converted into digital signals by the A/D converters, then input to the main circuit, where information of antenna's received signal strength is obtained. On the other hand, the comparator determines which of the RSSI voltages is larger by comparative operation, and it outputs information of maximum antenna input system according to

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Date: 03 OCT 1997

REPLACEMENT SHEETS		SG
☒	Description : paged 1 to paged 8	
☒	Claim(s) : paged 9 to paged 10	
☒	Drawing(s) : paged 11 to paged 5	
☒	Abstract : paged 11 to paged 1	

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that determination.

However, in the conventional diversity receiver, there is a problem that the peak hold circuit and the A/D converter are necessary to process the RSSI voltage output from each of the receivers while only one maximum RSSI voltage is used as a detection data. Therefore, when the number of the receivers is increased to more than two, the number of the peak hold circuits and A/D converters has to be further increased. Namely, the integrated circuit must be so much enlarged, and it will be therefore complicated and costly.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the invention to provide a diversity receiver whose circuit composition is effectively simplified.

According to the invention, a diversity receiver, comprises:

a plurality of receivers, each of which having a receiving antenna;

a maximum received signal strength indication voltage selector circuit which outputs a maximum received signal strength indication voltage to be selected from received signal strength indication voltages to be obtained by the plurality of receivers; and

a received signal strength information processing circuit which processes information of antenna's received signal strength based on the maximum received signal strength indication voltage to be input from the maximum received signal strength indication voltage selector circuit.

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BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be explained in more detail in conjunction with the appended drawings, wherein:

FIG.1 is a block diagram showing main part of a conventional diversity receiver,

FIG.2 is a block diagram showing main part of a diversity receiver in a preferred embodiment according to the invention,

FIG.3 is a circuit diagram showing the details of a maximum RSSI selector circuit 109 in FIG.2,

FIG.4 is a circuit diagram showing the details of a maximum RSSI identification signal generating circuit 114 in FIG.2,

FIG.5 shows a truth table for identification signals A, B in FIG.4,

FIG.6 is a block diagram showing the details of a four-terminal analog switching circuit 115 in FIG.2,

FIG.7 is a circuit diagram showing another maximum RSSI selector circuit adaptable to the diversity receiver in FIG.2, and

FIG.8 is a block diagram showing another four-terminal analog switching circuit adaptable to the diversity receiver in FIG.2.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before explaining a diversity receiver in the preferred embodiment of the invention, the aforementioned conventional diversity receiver will be explained in FIG.1.

FIG.1 shows main part of a conventional diversity receiver,

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Date: 03 OCT 1997

where 701 and 709 are receiving antennas provided for receivers 702 and 710, respectively, 703 and 711 are received signal strength indication(hereinafter referred to as 'RSSI') voltages to be output from the receivers 702 and 710, respectively, 704 and 712 are peak hold circuits for the RSSI voltages, 705 and 713 are analog-to-digital converters(hereinafter referred to as 'A/D converter(s)') for digital-converting the outputs of the peak hold circuits 704 and 712, and 706 and 714 are outputs of the A/D converters which are input to a main circuit(not shown), where information of antenna's received signal strength is obtained based on the outputs. Also, 707 and 715 are antenna input system signals used as received data, 717 is a comparator for comparing the RSSI voltages, and 718 is an output of the comparator 717.

Next, a diversity receiver in the preferred embodiment of the invention will be explained in FIG.2.

In FIG.2, 101, 102, 103 and 104 are RSSI voltages output individually from four receivers 121, 122, 123 and 124 with receiving antennas 131, 132, 133 and 134, respectively, 105, 106, 107 and 108 are antenna input system signals which are radio-frequency data signals received by the receivers 121 to 124, 109 is a maximum RSSI(received signal strength indication) selector circuit which selects one maximum RSSI voltage from the RSSI voltages 101 to 104, 111 is a peak hold circuit which holds a peak value of the maximum RSSI voltage, 112 is an A/D converter which digital-converts the peak hold voltage and 113 is a 8-bit digital output which holds information of antenna's received signal strength. A received signal strength information

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Date: 03 OCT 1997

processing circuit 118 is composed of the peak hold circuit 111, the A/D converter 112 and a main circuit where the information of antenna's received signal strength is input.

On the other hand, 114 is a maximum RSSI identification signal generating circuit which outputs a digital signal for identifying a maximum antenna input system based on a 3-bit signal as RSSI selection information output from the maximum RSSI selector circuit 109. 115 is a four-terminal analog switching circuit which switches into and outputs one of the antenna input system signals 105 to 108 as a maximum antenna input system signal 116 based on a 2-bit output of the maximum RSSI identification signal generating circuit 114.

The maximum RSSI selector circuit 109 will be detailed in FIG.3. In this circuit, the two RSSI voltages 101, 102 are compared by a comparator 205, and then one of the RSSI voltages 101, 102 which has a greater level is output selectively by switching an analog switch 208 according to the result of that comparison. On the other hand, the other two RSSI voltages 103, 104 are compared by a comparator 206, and then one of the RSSI voltages 103, 104 which has a greater level is output selectively by switching an analog switch 209 according to the result of that comparison.

Then, the two RSSI voltages output through the analog switches 208, 209 are compared by a comparator 207, and then one of the two RSSI voltages which has a greater level is output selectively as the maximum RSSI voltage by switching an analog switch 210 according to the result of that comparison. In FIG.3, a, b and c are comparison result outputs(3 bits) from the

comparators 205, 206 and 207.

The maximum RSSI identification signal generating circuit 114 will be detailed in FIG.4. 251 is a NAND circuit where the two comparison result outputs a and c are input, 252 is an inverter for inverting the comparison result output c, 253 is a NAND circuit where the inverted output and the comparison result output b are input, and 254 is an AND circuit which conducts AND operation between the outputs of the NAND circuits 251, 253. The AND circuit 254 outputs an output A and the inverter 252 outputs an output B. FIG.5 is a truth table of the outputs A, B to the RSSI voltages.

FIG.6 shows the details of the four-terminal analog switching circuit 115, where a maximum one of the antenna input system signals 105 to 108 is selected by an analog switch 271 based on the outputs A, B and is output as the maximum antenna input signal 116.

As described above, in the diversity receiver in this embodiment, firstly, the maximum RSSI selector circuit 109 selects the maximum one of the four RSSI voltages output from the receivers 121 to 124 and outputs it as the maximum RSSI voltage 110. In detail, the four RSSI voltages are input to the comparators 205, 206, and then the greater ones of them are selected by the analog switches 208, 209 according to the comparison results and are again input to the comparator 207, and then the greater one is selected by the analog switch 210 according to the comparison result to output the maximum RSSI voltage 110. Namely, the RSSI voltages are compared in a tournament manner to obtain the maximum RSSI voltage.

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Date: 03 OCT 1997

Then, the maximum RSSI voltage 110 obtained is input through the peak hold circuit 111, A/D converter 112 as a 8-bit digital signal to the main circuit 117, where information of antenna's received signal strength is obtained based on the digital signal.

On the other hand, in the maximum RSSI identification signal generating circuit 114, the outputs a, b and c(3 bits) of the maximum RSSI selector circuit 109 as shown in FIG.3 are input to the logical circuit as shown in FIG.4, and then the 2-bit identification data A, B corresponding to the RSSI voltages as shown in FIG.5 are obtained. Also, the antenna input system signals 105 to 108 as the radio-frequency data signals are input to the four-terminal analog switching circuit 115. In the four-terminal analog switching circuit 115, the maximum antenna input system signal 116 which is the maximum one of the antenna input system signals 105 to 108 is selected according to the 2-bit identification data A, B and is output to a demodulator(not shown), where reception data is produced and output.

Thus, by selecting the maximum RSSI voltage to be used as data from the four RSSI voltages, the number of peak hold circuits and A/D converters, which were conventionally necessary to provide corresponding to the number of receivers, can be reduced. Namely, only the peak hold circuit 111 and A/D converter 113 are necessary. Therefore, the number of parts can be reduced, the entire circuit can be simplified, the number of interfaces to LSI can be reduced and the manufacturing cost can be reduced.

Meanwhile, as the four-terminal analog switching circuit 115, a double-circuit type is generally used other than the

single-circuit type as shown in FIG.6. In such a case, a maximum RSSI selector circuit 109A, where the analog switch 210 of the maximum RSSI selector circuit 109 as shown in FIG.3 is omitted, is used to provide outputs a, b and c(3 bits) as shown in FIG.7. Based on the outputs, the maximum RSSI identification signal generating circuit 114 generates the maximum RSSI identification signals A, B(2 bits).

On the other hand, based on the maximum RSSI identification signals A, B, a four-terminal analog switching circuit 115A, which has a first analog switch 151 and a second analog switch 152, as shown in FIG.8, outputs the maximum RSSI voltage 110 selected from the RSSI voltages 101 to 104 and outputs the maximum antenna input system signal 116 selected from the antenna input system signals 105 to 108. Thus, by using the four-terminal analog switching circuit 115A, the electric power loss can be saved since the RSSI voltage need only one analog switch.

Although the invention has been described with respect to specific embodiment for complete and clear disclosure, the appended claims are not to be thus limited but are to be construed as embodying all modification and alternative constructions that may be occurred to one skilled in the art which fairly fall within the basic teaching here is set forth.



Claims

1. A diversity receiver, comprising:

a plurality of receivers, each of which having a receiving antenna;

a maximum received signal strength indication voltage selector circuit which outputs a maximum received signal strength indication voltage to be selected from received signal strength indication voltages to be obtained by said plurality of receivers; and

a received signal strength information processing circuit which processes information of antenna's received signal strength based on said maximum received signal strength indication voltage to be input from said maximum received signal strength indication voltage selector circuit.

2. A diversity receiver, according to claim 1, wherein:

said maximum received signal strength indication voltage selector circuit comprises a plurality of comparators, each of which comparing two of said received signal strength indication voltages in a tournament manner, and a plurality of switches, each of which outputting greater one of said two received signal strength indication voltages according to a comparison result of said corresponding comparator and finally outputting said maximum received signal strength indication voltage through said tournament-manner comparative operation.

3. A diversity receiver, according to claim 2, further



comprising:

a maximum received signal strength indication voltage identification signal generating circuit which generates an identification signal of said maximum received signal strength indication voltage based on outputs of said comparators of said maximum received signal strength indication voltage selector circuit; and

an analog switching circuit which outputs a maximum antenna input system signal to be selected from antenna input system signals received by said receiving antenna based on said identification signal to be generated by said maximum received signal strength indication voltage identification signal generating circuit.

4. A diversity receiver, according to claim 3, wherein:

said analog switching circuit comprises a first analog switch which outputs said maximum received signal strength indication voltage to be selected from said plurality of received signal strength indication voltages based on said identification signal to be generated by said maximum received signal strength indication voltage identification signal generating circuit, and a second analog switch which outputs said maximum antenna input system signal to be selected from said antenna input system signals.

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DIVERSITY RECEIVER

ABSTRACT

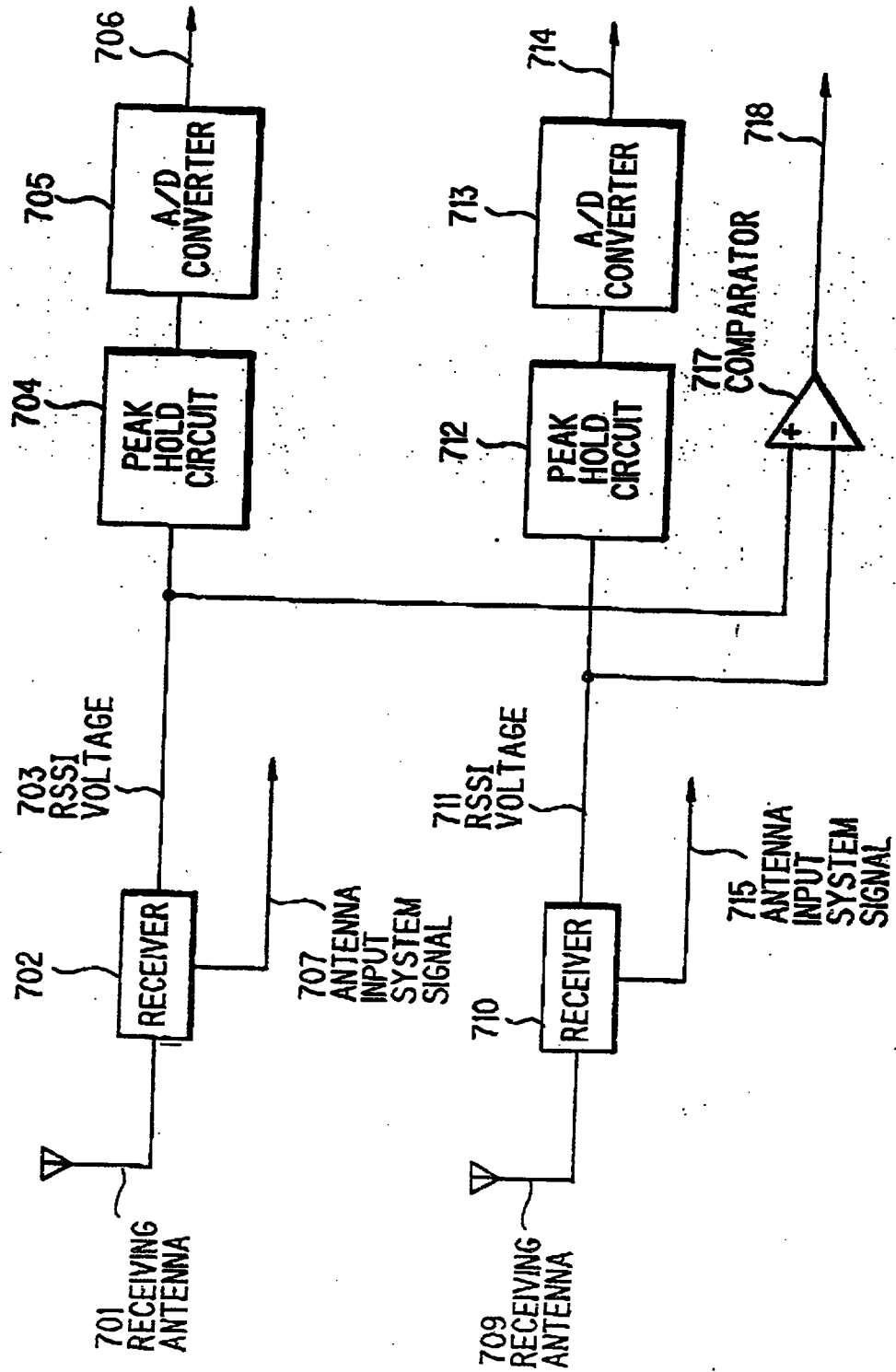
Disclosed is a diversity receiver which has: a plurality of receivers (121, 122, 123 and 124), each of which having a receiving antenna (131, 132, 133 and 134); a maximum received signal strength indication voltage selector circuit (109) which outputs a maximum received signal strength indication voltage to be selected from received signal strength indication voltages to be obtained by said plurality of receivers (121, 122, 123 and 124); and a received signal strength information processing circuit (118) which processes information of antenna's received signal strength based on said maximum received signal strength indication voltage to be input from said maximum received signal strength indication voltage selector circuit (109).

Fig. 2

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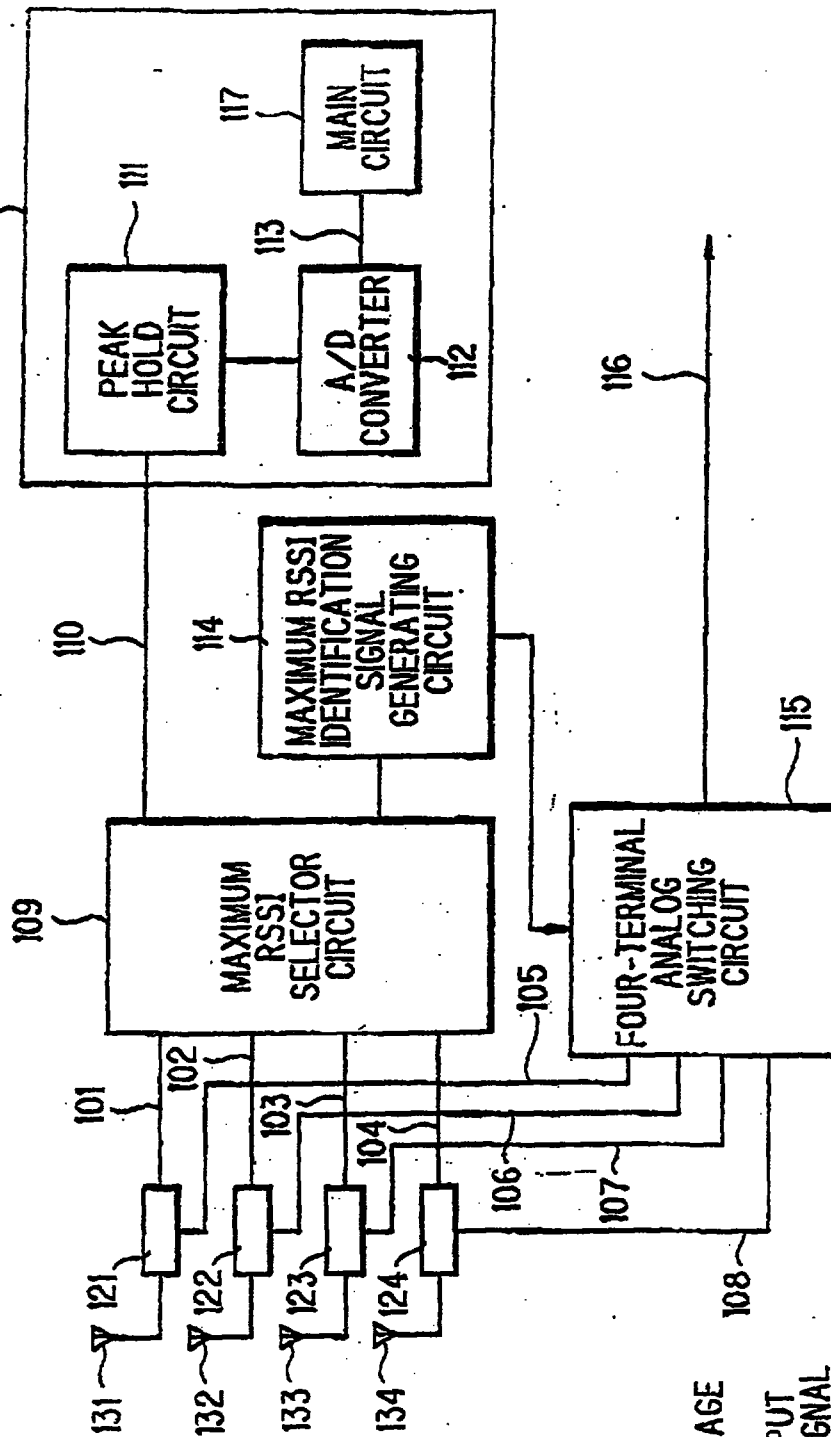
Date: 03 OCT 1997

FIG. 1 PRIOR ART



118
RECEIVED SIGNAL
STRENGTH INFORMATION
PROCESSING CIRCUIT

FIG. 2



131-134 : RECEIVING
ANTENNA

121-124 : RECEIVER

101-104 : RSSI VOLTAGE

105-108 : ANALOG INPUT
SYSTEM SIGNAL

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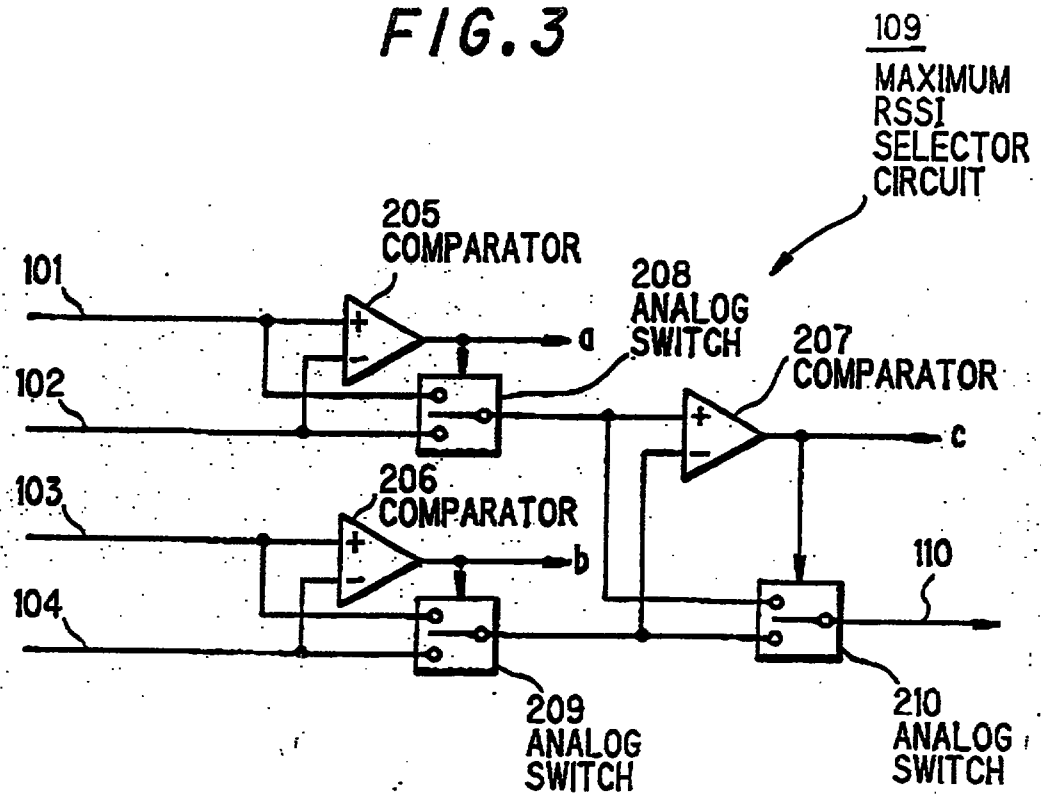
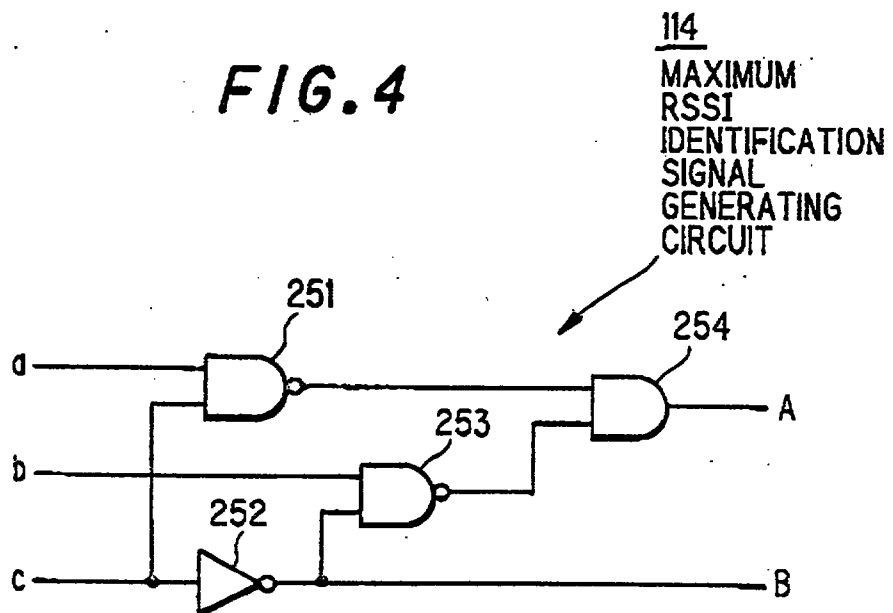
FIG. 3**FIG. 4**

FIG. 5

MAXIMUM SYSTEM	B	A
101	0	0
102	0	1
103	1	0
104	1	1

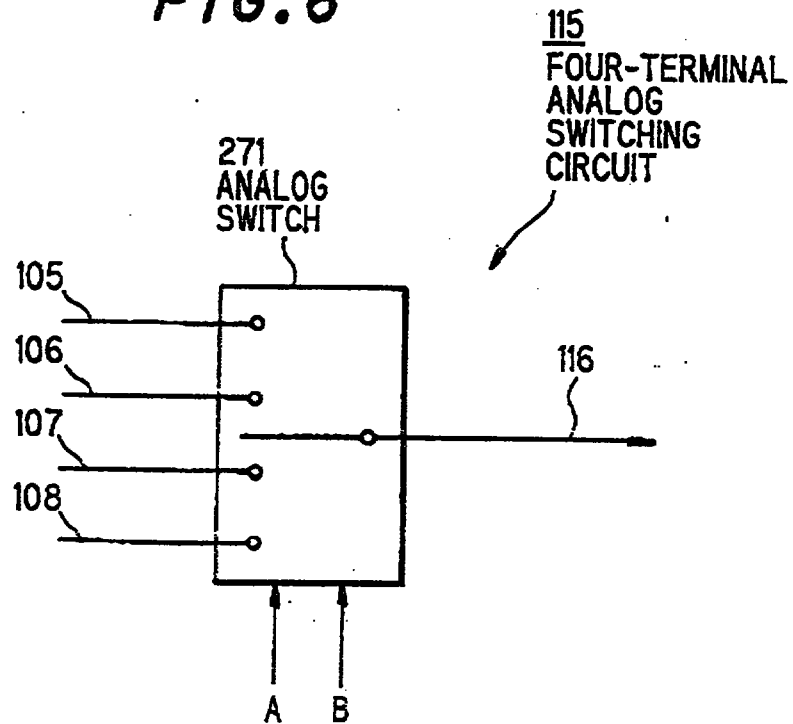
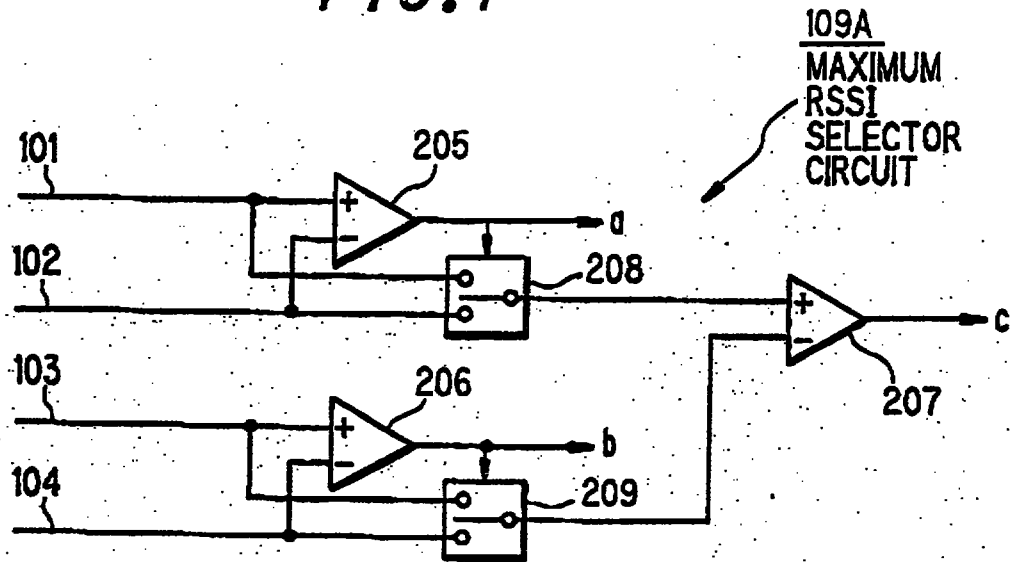
FIG. 6

FIG. 7**FIG. 8**