ABSTRACT

A clock gating cell including: a first circuit configured to receive an enable signal and an inverted output clock signal and generate a first signal through a first node; a second circuit configured to receive the first signal and generate an inverted first signal; a third circuit configured to receive the first signal, the inverted first signal, and an input clock signal, generate the first signal by being connected to the first circuit through the first node, and generate the inverted output clock signal through a second node; and a fourth circuit configured to receive the first signal, generate the inverted output clock signal by being connected to the third circuit through the second node, and generate the output clock signal, wherein the third circuit includes a pair of transistors receiving the input clock signal.

FIG. 1