

ABSTRACT

An embodiment provides a data processing circuit and a device. The circuit includes: a first bank group 201 and a second bank group 202; a write circuit 203; and a read circuit 204. The write circuit 203 includes a write input cache circuit 2031, and is configured to: receive stored data from a write bus 206 through the write input cache circuit 2031, write the stored data into the first bank group 201 through a first read-write bus 207, and write the stored data into the second bank group 202 through a second read-write bus 208. The read circuit 204 includes a read output cache circuit 2041, and is configured to: read the stored data from the first bank group 201 through the first read-write bus 207, and read the stored data from the second bank group 202 through the second read-write bus 208. In the embodiment of the present disclosure, each write circuit includes a write input cache circuit, and each read circuit includes a read output cache circuit, to reduce circuit size.