

**PACKAGE SUBSTRATE, PACKAGE SUBSTRATE PROCESSING METHOD,
AND PACKAGED CHIP**

ABSTRACT

A package substrate includes a metallic lead frame that includes first frame portions in a lattice shape along planned dividing lines and a plurality of first electrode portions extending from each of the first frame portions, a connection frame that includes second frame portions in a lattice shape along the planned dividing lines and a plurality of second electrode portions extending from each of the second frame portions, the connection frame being superposed on a side of the lead frame on which a device chip is disposed, and a mold resin that covers the device chip and the connection frame. Distal ends of the second electrode portions are formed in a protruding shape and connected to the first electrode portions, and the connection frame forms an electrode when electroplating processing is applied to sections of the first electrode portions.

[FIG.10]