

POWER AMPLIFIERS WITH ADAPTIVE BIAS FOR ENVELOPE TRACKING APPLICATIONS

BACKGROUND

Field

5 **[0001]** Embodiments of the invention relate to electronic systems, and in particular, to power amplifiers for use in radio frequency (RF) electronics.

Description of the Related Technology

10 **[0002]** Power amplifiers are used in radio frequency (RF) communication systems to amplify RF signals for transmission via antennas. It is important to manage the power of RF signal transmissions to prolong battery life and/or provide a suitable transmit power level.

15 **[0003]** Examples of RF communication systems with one or more power amplifiers include, but are not limited to, mobile phones, tablets, base stations, network access points, customer-premises equipment (CPE), laptops, and wearable electronics. For example, in wireless devices that communicate using a cellular standard, a wireless local area network (WLAN) standard, and/or any other suitable communication standard, a power amplifier can be used for RF signal amplification. An RF signal can have a frequency in the range of about 30 kHz to 300 GHz, for instance, in the range of about 410 MHz to about 7.125 GHz for Fifth Generation (5G) cellular communications in Frequency Range 1 (FR1) or in the range of about 20 24.250 GHz to about 52.600 GHz for Frequency Range 2 (FR2) of the 5G communication standard.

SUMMARY

25 **[0004]** In certain embodiments, the present disclosure relates to a mobile device. The mobile device includes a transceiver configured to generate a radio frequency signal, a power management system including an envelope tracker configured to generate a power amplifier supply voltage that changes in relation to an envelope of the radio frequency signal, and a front end system including a power amplifier configured to amplify the radio frequency 30 signal and to receive power from the power amplifier supply voltage. The power amplifier

includes a current mirror having an input configured to receive a reference current and an output electrically connected to the power amplifier supply voltage, and a field-effect transistor configured to amplify the radio frequency signal and having a gate biased based on an internal voltage of the current mirror.

5 **[0005]** In various embodiments, the internal voltage of the current mirror increases in response to a decrease of the power amplifier supply voltage, and decreases in response to an increase of the power amplifier supply voltage.

[0006] In a number of embodiments, the field-effect transistor is a short channel metal oxide semiconductor transistor.

10 **[0007]** In several embodiments, the power amplifier further includes a choke inductor electrically connected between the power amplifier supply voltage a drain of the field-effect transistor.

[0008] In some embodiments, the current mirror is a Wilson current mirror.

[0009] In various embodiments, the power amplifier further includes a buffer
15 configured to buffer the internal voltage of the current mirror to generate a gate bias voltage of the field-effect transistor. According to a number of embodiments, the buffer includes a first depletion-mode transistor and a second depletion-mode transistor configured to provide buffering with a zero shift.

[0010] In several embodiments, the current mirror includes a first mirror transistor
20 having a drain configured to output the internal voltage, a second mirror transistor, a third mirror transistor, and a fourth mirror transistor, the third mirror transistor and the first mirror transistor connected in series between the input of the current mirror and a ground voltage, and the fourth mirror transistor and the second mirror transistor connected in series between the output of the current mirror and the ground voltage. According to a number of embodiments,
25 a gate of the first mirror transistor is connected to a gate of the second mirror transistor, and a gate of the third mirror transistor is connected to a gate of the fourth mirror transistor. In accordance with various embodiments, a drain of the second mirror transistor is connected to the gate of the second mirror transistor, and a drain of the third mirror transistor is connected to the gate of the third mirror transistor.

30 **[0011]** In several embodiments, the power amplifier further includes a current source configured to generate the reference current.

[0012] In some embodiments, the envelope tracker includes a DC-to-DC converter configured to output a plurality of regulated voltages, a modulator configured to generate a modulator output voltage at an output based on the plurality of regulated voltages and the envelope of the radio frequency signal, and a modulator output filter coupled between the
5 output of the modulator and the power amplifier supply voltage.

[0013] In various embodiments, the envelope tracker includes a DC-to-DC converter and an error amplifier configured to operate in parallel with one another to generate the power amplifier supply voltage.

[0014] In certain embodiments, the present disclosure relates to an envelope
10 tracking system. The envelope tracking system includes an envelope tracker configured to generate a power amplifier supply voltage that changes in relation to an envelope of a radio frequency signal, and a power amplifier configured to amplify the radio frequency signal and to receive power from the power amplifier supply voltage. The power amplifier includes a current mirror having an input configured to receive a reference current and an output
15 electrically connected to the power amplifier supply voltage, and a field-effect transistor configured to amplify the radio frequency signal and having a gate biased based on an internal voltage of the current mirror.

[0015] In various embodiments, the internal voltage of the current mirror increases in response to a decrease of the power amplifier supply voltage, and decreases in response to
20 an increase of the power amplifier supply voltage.

[0016] In several embodiments, the field-effect transistor is a short channel metal oxide semiconductor transistor.

[0017] In some embodiments, the power amplifier further includes a choke inductor electrically connected between the power amplifier supply voltage and a drain of the field-
25 effect transistor.

[0018] In various embodiments, the current mirror is a Wilson current mirror.

[0019] In several embodiments, the power amplifier further includes a buffer configured to buffer the internal voltage of the current mirror to generate a gate bias voltage of the field-effect transistor. According to a number of embodiments, the buffer includes a first
30 depletion-mode transistor and a second depletion-mode transistor configured to provide buffering with a zero shift.

[0020] In some embodiments, the current mirror includes a first mirror transistor having a drain configured to output the internal voltage, a second mirror transistor, a third mirror transistor, and a fourth mirror transistor, the third mirror transistor and the first mirror transistor connected in series between the input of the current mirror and a ground voltage, and
5 the fourth mirror transistor and the second mirror transistor connected in series between the output of the current mirror and the ground voltage. According to a number of embodiments, a gate of the first mirror transistor is connected to a gate of the second mirror transistor, and a gate of the third mirror transistor is connected to a gate of the fourth mirror transistor. In various embodiments, a drain of the second mirror transistor is connected to the gate of the
10 second mirror transistor, and a drain of the third mirror transistor is connected to the gate of the third mirror transistor.

[0021] In several embodiments, the power amplifier further includes a current source configured to generate the reference current.

[0022] In some embodiments, the envelope tracker includes a DC-to-DC converter
15 configured to output a plurality of regulated voltages, a modulator configured to generate a modulator output voltage at an output based on the plurality of regulated voltages and the envelope of the radio frequency signal, and a modulator output filter coupled between the output of the modulator and the power amplifier supply voltage.

[0023] In several embodiments, the envelope tracker includes a DC-to-DC
20 converter and an error amplifier configured to operate in parallel with one another to generate the power amplifier supply voltage.

[0024] In certain embodiments, the present disclosure relates to a method of radio frequency signal amplification in a mobile device. The method includes generating a power amplifier supply voltage that changes in relation to an envelope of a radio frequency signal
25 using an envelope tracker, powering a power amplifier using the power amplifier supply voltage, amplifying the radio frequency signal using a field-effect transistor of the power amplifier, and generating a gate bias voltage of the field-effect transistor using an internal voltage of a current mirror of the power amplifier, including providing a reference current to an input of the current mirror and providing the power amplifier supply voltage to an output of
30 the current mirror.

[0025] In various embodiments, the method includes increasing the internal voltage of the current mirror in response to a decrease of the power amplifier supply voltage, and decreasing the internal voltage of the current mirror in response to an increase of the power amplifier supply voltage.

5 [0026] In several embodiments, the field-effect transistor is a short channel metal oxide semiconductor transistor.

[0027] In a number of embodiments, the method further includes providing the power amplifier supply voltage to a drain of the field-effect transistor using a choke inductor.

[0028] In some embodiments, the current mirror is a Wilson current mirror.

10 [0029] In various embodiments, the method further includes buffering the internal voltage of the current mirror to generate the gate bias voltage of the field-effect transistor.

[0030] In a number of embodiments, the method further includes generating the reference current using a current source.

[0031] In several embodiments, generating the power amplifier supply voltage
15 includes outputting a plurality of regulated voltages from a DC-to-DC converter, generating a modulator output voltage based on the plurality of regulated voltages and the envelope of the radio frequency signal using a modulator, and filtering the modulator output voltage to generate the power amplifier supply voltage using a modulator output filter.

[0032] In some embodiments, generating the power amplifier supply voltage
20 includes tracking the envelope using a DC-to-DC converter and an error amplifier operating in parallel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] Figure 1 is a schematic diagram of one embodiment of a mobile device.

25 [0034] Figure 2 is a schematic diagram of one embodiment of a transmit system for transmitting radio frequency (RF) signals from a mobile device.

[0035] Figure 3 is a schematic diagram of a power amplifier according to one embodiment.

[0036] Figure 4A is a graph of one example of power gain versus output power for
30 a power amplifier without adaptive bias.

[0037] Figure 4B is a graph of one example of power gain versus output power for a power amplifier with adaptive bias.

[0038] Figure 4C is a graph of one example of quiescent drain current versus supply voltage for a power amplifier without adaptive bias.

5 [0039] Figure 4D is a graph of one example of quiescent drain current versus supply voltage for a power amplifier with adaptive bias.

[0040] Figure 5 is a schematic diagram of a power amplifier according to another embodiment.

10 [0041] Figure 6A is a graph of one example of amplitude distortion versus load power for a power amplifier with adaptive bias but without a buffer.

[0042] Figure 6B is a graph of one example of amplitude distortion versus load power for a power amplifier with adaptive bias and with a buffer.

[0043] Figure 6C is a graph of one example of phase distortion versus load power for a power amplifier with adaptive bias but without a buffer.

15 [0044] Figure 6D is a graph of one example of phase distortion versus load power for a power amplifier with adaptive bias and with a buffer.

[0045] Figure 7A is a graph of one example of drain current versus drain voltage for a short channel metal oxide semiconductor (MOS) transistor.

20 [0046] Figure 7B is a graph of one example of drain current versus gate voltage for a short channel MOS transistor.

[0047] Figure 8A is a graph of one example of a power amplifier supply voltage versus time.

[0048] Figure 8B is a graph of another example of a power amplifier supply voltage versus time.

25 [0049] Figure 9A is a schematic diagram of an envelope tracking system according to one embodiment.

[0050] Figure 9B is a schematic diagram of an envelope tracking system according to another embodiment.

30 [0051] Figure 10 is a schematic diagram of an envelope tracking system according to another embodiment.

[0052] Figure 11A is a schematic diagram of one embodiment of a packaged module.

[0053] Figure 11B is a schematic diagram of a cross-section of the packaged module of Figure 11A taken along the lines 11B–11B.

5 [0054] Figure 12 is a schematic diagram of one embodiment of a phone board.

DETAILED DESCRIPTION OF EMBODIMENTS

[0055] The following detailed description of certain embodiments presents various descriptions of specific embodiments. However, the innovations described herein can be embodied in a multitude of different ways, for example, as defined and covered by the claims. In this description, reference is made to the drawings where like reference numerals can indicate identical or functionally similar elements. It will be understood that elements illustrated in the figures are not necessarily drawn to scale. Moreover, it will be understood that certain embodiments can include more elements than illustrated in a drawing and/or a subset of the elements illustrated in a drawing. Further, some embodiments can incorporate any suitable combination of features from two or more drawings.

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[0056] Figure 1 is a schematic diagram of one example of a mobile device 100. The mobile device 100 includes a baseband system 1, a transceiver 2, a front end system 3, antennas 4, a power management system 5, a memory 6, a user interface 7, and a battery 8.

20 [0057] The mobile device 100 can be used communicate using a wide variety of communications technologies, including, but not limited to, 2G, 3G, 4G (including LTE, LTE-Advanced, and LTE-Advanced Pro), 5G, WLAN (for instance, Wi-Fi), WPAN (for instance, Bluetooth and ZigBee), WMAN (for instance, WiMax), and/or GPS technologies.

[0058] The transceiver 2 generates RF signals for transmission and processes incoming RF signals received from the antennas 4. It will be understood that various functionalities associated with the transmission and receiving of RF signals can be achieved by one or more components that are collectively represented in Figure 1 as the transceiver 2. In one example, separate components (for instance, separate circuits or dies) can be provided for handling certain types of RF signals.

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30 [0059] The front end system 3 aids in conditioning signals transmitted to and/or received from the antennas 4. In the illustrated embodiment, the front end system 3 includes

power amplifiers (PAs) 11, low noise amplifiers (LNAs) 12, filters 13, switches 14, and duplexers 15. However, other implementations are possible.

[0060] For example, the front end system 3 can provide a number of functionalities, including, but not limited to, amplifying signals for transmission, amplifying received signals, 5 filtering signals, switching between different bands, switching between different power modes, switching between transmission and receiving modes, duplexing of signals, multiplexing of signals (for instance, diplexing or triplexing), or some combination thereof.

[0061] In certain implementations, the mobile device 100 supports carrier aggregation, thereby providing flexibility to increase peak data rates. Carrier aggregation can 10 be used for both Frequency Division Duplexing (FDD) and Time Division Duplexing (TDD), and may be used to aggregate a plurality of carriers or channels. Carrier aggregation includes contiguous aggregation, in which contiguous carriers within the same operating frequency band are aggregated. Carrier aggregation can also be non-contiguous, and can include carriers separated in frequency within a common band and/or in different bands.

15 [0062] The antennas 4 can include antennas used for a wide variety of types of communications. For example, the antennas 4 can include antennas associated transmitting and/or receiving signals associated with a wide variety of frequencies and communications standards.

[0063] In certain implementations, the antennas 4 support MIMO communications 20 and/or switched diversity communications. For example, MIMO communications use multiple antennas for communicating multiple data streams over a single radio frequency channel. MIMO communications benefit from higher signal to noise ratio, improved coding, and/or reduced signal interference due to spatial multiplexing differences of the radio environment. Switched diversity refers to communications in which a particular antenna is selected for 25 operation at a particular time. For example, a switch can be used to select a particular antenna from a group of antennas based on a variety of factors, such as an observed bit error rate and/or a signal strength indicator.

[0064] The mobile device 100 can operate with beamforming in certain implementations. For example, the front end system 3 can include phase shifters having 30 variable phase controlled by the transceiver 2. Additionally, the phase shifters are controlled to provide beam formation and directivity for transmission and/or reception of signals using

the antennas 4. For example, in the context of signal transmission, the phases of the transmit signals provided to the antennas 4 are controlled such that radiated signals from the antennas 4 combine using constructive and destructive interference to generate an aggregate transmit signal exhibiting beam-like qualities with more signal strength propagating in a given direction. In the context of signal reception, the phases are controlled such that more signal energy is received when the signal is arriving to the antennas 4 from a particular direction. In certain implementations, the antennas 4 include one or more arrays of antenna elements to enhance beamforming.

[0065] The baseband system 1 is coupled to the user interface 7 to facilitate processing of various user input and output (I/O), such as voice and data. The baseband system 1 provides the transceiver 2 with digital representations of transmit signals, which the transceiver 2 processes to generate RF signals for transmission. The baseband system 1 also processes digital representations of received signals provided by the transceiver 2. As shown in Figure 1, the baseband system 1 is coupled to the memory 6 of facilitate operation of the mobile device 100.

[0066] The memory 6 can be used for a wide variety of purposes, such as storing data and/or instructions to facilitate the operation of the mobile device 100 and/or to provide storage of user information.

[0067] The power management system 5 provides a number of power management functions of the mobile device 100. The power management system 5 of Figure 1 includes an envelope tracker 60. As shown in Figure 1, the power management system 5 receives a battery voltage form the battery 8. The battery 8 can be any suitable battery for use in the mobile device 100, including, for example, a lithium-ion battery.

[0068] The mobile device 100 of Figure 1 illustrates one example of an RF communication system that can include power amplifier(s) implemented in accordance with one or more features of the present disclosure. However, the teachings herein are applicable to RF communication systems implemented in a wide variety of ways.

[0069] Figure 2 is a schematic diagram of one embodiment of a transmit system 130 for transmitting RF signals from a mobile device. The transmit system 130 includes a battery 101, an envelope tracker 102, a power amplifier 103, a directional coupler 104, a duplexing and switching circuit 105, an antenna 106, a baseband processor 107, a signal delay

circuit 108, a digital pre-distortion (DPD) circuit 109, an I/Q modulator 110, an observation receiver 111, an intermodulation detection circuit 112, an envelope delay circuit 121, a coordinate rotation digital computation (CORDIC) circuit 122, a shaping circuit 123, a digital-to-analog converter 124, and a reconstruction filter 125.

5 **[0070]** The transmit system 130 of Figure 2 illustrates one example of an RF communication system that can include power amplifier(s) implemented in accordance with one or more features of the present disclosure. However, the teachings herein are applicable to RF communication systems implemented in a wide variety of ways.

10 **[0071]** The baseband processor 107 operates to generate an I signal and a Q signal, which correspond to signal components of a sinusoidal wave or signal of a desired amplitude, frequency, and phase. For example, the I signal can be used to represent an in-phase component of the sinusoidal wave and the Q signal can be used to represent a quadrature-phase component of the sinusoidal wave, which can be an equivalent representation of the sinusoidal wave. In certain implementations, the I and Q signals are provided to the I/Q modulator 110
15 in a digital format. The baseband processor 107 can be any suitable processor configured to process a baseband signal. For instance, the baseband processor 107 can include a digital signal processor, a microprocessor, a programmable core, or any combination thereof.

[0072] The signal delay circuit 108 provides adjustable delay to the I and Q signals to aid in controlling relative alignment between the envelope signal and the RF signal RF_{IN} .
20 The amount of delay provided by the signal delay circuit 108 is controlled based on amount of intermodulation detected by the intermodulation detection circuit 112.

[0073] The DPD circuit 109 operates to provide digital shaping to the delayed I and Q signals from the signal delay circuit 108 to generate digitally pre-distorted I and Q signals. In the illustrated embodiment, the DPD provided by the DPD circuit 109 is controlled based
25 on amount of intermodulation detected by the intermodulation detection circuit 112. The DPD circuit 109 serves to reduce a distortion of the power amplifier 103 and/or to increase the efficiency of the power amplifier 103.

[0074] The I/Q modulator 110 receives the digitally pre-distorted I and Q signals, which are processed to generate an RF signal RF_{IN} . For example, the I/Q modulator 110 can
30 include DACs configured to convert the digitally pre-distorted I and Q signals into an analog format, mixers for upconverting the analog I and Q signals to radio frequency, and a signal

combiner for combining the upconverted I and Q signals into an RF signal suitable for amplification by the power amplifier 103. In certain implementations, the I/Q modulator 110 can include one or more filters configured to filter frequency content of signals processed therein.

5 **[0075]** The envelope delay circuit 121 delays the I and Q signals from the baseband processor 107. Additionally, the CORDIC circuit 122 processes the delayed I and Q signals to generate a digital envelope signal representing an envelope of the RF signal RF_{IN} . Although Figure 2 illustrates an implementation using the CORDIC circuit 122, an envelope signal can be obtained in other ways.

10 **[0076]** The shaping circuit 123 operates to shape the digital envelope signal to enhance the performance of the transmit system 130. In certain implementations, the shaping circuit 123 includes a shaping table that maps each level of the digital envelope signal to a corresponding shaped envelope signal level. Envelope shaping can aid in controlling linearity, distortion, and/or efficiency of the power amplifier 103.

15 **[0077]** In the illustrated embodiment, the shaped envelope signal is a digital signal that is converted by the DAC 124 to an analog envelope signal. Additionally, the analog envelope signal is filtered by the reconstruction filter 125 to generate an envelope signal suitable for use by the envelope tracker 102. In certain implementations, the reconstruction filter 125 includes a low pass filter.

20 **[0078]** With continuing reference to Figure 2, the envelope tracker 102 receives the envelope signal from the reconstruction filter 125 and a battery voltage V_{BATT} from the battery 101, and uses the envelope signal to generate a power amplifier supply voltage V_{PA} for the power amplifier 103 that changes in relation to the envelope of the RF signal RF_{IN} . The power amplifier 103 receives the RF signal RF_{IN} from the I/Q modulator 110, and provides an
25 amplified RF signal RF_{OUT} to the antenna 106 through the duplexing and switching circuit 105, in this example.

[0079] The directional coupler 104 is positioned between the output of the power amplifier 103 and the input of the duplexing and switching circuit 105, thereby allowing a measurement of output power of the power amplifier 103 that does not include insertion loss
30 of the duplexing and switching circuit 105. The sensed output signal from the directional coupler 104 is provided to the observation receiver 111, which can include mixers for down

converting I and Q signal components of the sensed output signal, and DACs for generating I and Q observation signals from the downconverted signals.

[0080] The intermodulation detection circuit 112 determines an intermodulation product between the I and Q observation signals and the I and Q signals from the baseband processor 107. Additionally, the intermodulation detection circuit 112 controls the DPD provided by the DPD circuit 109 and/or a delay of the signal delay circuit 108 to control relative alignment between the envelope signal and the RF signal RF_{IN} .

[0081] By including a feedback path from the output of the power amplifier 103 and baseband, the I and Q signals can be dynamically adjusted to optimize the operation of the transmit system 130. For example, configuring the transmit system 130 in this manner can aid in providing power control, compensating for transmitter impairments, and/or in performing DPD.

[0082] Although illustrated as a single stage, the power amplifier 103 can include one or more stages. Furthermore, RF communication systems such as mobile devices can include multiple power amplifiers. In such implementations, separate envelope trackers can be provided for different power amplifiers and/or one or more shared envelope trackers can be used.

Adaptive Bias for Power Amplifiers operating with Envelope Tracking

[0083] Envelope tracking is a technique that can be used to increase power added efficiency (PAE) of a power amplifier by efficiently controlling a voltage level of a power amplifier supply voltage in relation to an envelope of the RF signal amplified by the power amplifier. Thus, when the envelope of the RF signal increases, the voltage supplied to the power amplifier can be increased. Likewise, when the envelope of the RF signal decreases, the voltage supplied to the power amplifier can be decreased to reduce power consumption.

[0084] In one example, an envelope tracker includes a DC-to-DC converter that operates in combination with an error amplifier to generate a power amplifier supply voltage based on an envelope signal. For example, the DC-to-DC converter and the error amplifier can be electrically connected in parallel with one another, and the DC-to-DC converter can track low frequency components of the envelope signal while the error amplifier can track high frequency components of the envelope signal. For example, the DC-to-DC converter's

switching frequency can be reduced to be less than a maximum frequency component of the envelope signal, and the error amplifier can operate to smooth gaps in the converter's output to generate the power amplifier supply voltage. In certain implementations, the DC-to-DC converter and error amplifier are combined via a combiner.

5 **[0085]** In another example, an envelope tracker includes a multi-output boost switcher for generating regulated voltages of different voltage levels, a bank of switches for controlling selection of a suitable regulated voltage over time based on the envelope signal, and a filter for filtering the output of the switch bank to generate the power amplifier supply voltage.

10 **[0086]** Power amplifiers with adaptive bias for envelope tracking applications are provided herein. In certain embodiments, an envelope tracking system includes a power amplifier that amplifies an RF signal and that receives power from a power amplifier supply voltage, and an envelope tracker that generates the power amplifier supply voltage based on an envelope of the RF signal. The power amplifier includes a field-effect transistor (FET) for
15 amplifying the RF signal, and a current mirror including an input that receives a reference current and an output connected to the power amplifier supply voltage. An internal voltage of the current mirror is used to bias the gate of the FET to compensate the FET for changes in the power amplifier supply voltage arising from envelope tracking.

[0087] By implementing the power amplifier with adaptive bias, non-idealities of
20 the power amplifier's FET are compensated for. For example, such adaptive biasing aids in compensating for channel length modulation and/or drain induced barrier lowering that would otherwise give rise to high variation in RF gain versus power amplifier supply voltage.

[0088] In certain implementations, the FET is implemented as a short channel metal oxide semiconductor (MOS) transistor. Although short channel MOS transistors suffer
25 from a number of transistor non-idealities, adaptive biasing provides compensation that enables the short channel MOS transistor to be used in the power amplifier without significantly degrading the power amplifier's performance. Since short channel MOS transistors can be fabricated in processes that are low cost and/or enable high degrees of integration, it is desirable to implement a power amplifier using a short channel MOS transistor
30 in a number of applications.

[0089] In certain implementations, a buffer is further included for buffering the internal voltage of the current mirror to generate the gate bias voltage of the FET. Including the buffer can enhance the bandwidth and speed-up the transient response of the power amplifier's biasing, thereby improving amplitude and phase distortion.

5 [0090] The current mirror can be implemented in a wide variety of ways. In certain implementations, the current mirror is implemented as a Wilson current mirror. For example, the current mirror can be implemented using n-type field-effect transistors (NFETs) arranged as a four transistor Wilson current mirror. For example, the drain-to-source voltage of a first NFET of the four transistor Wilson mirror can increase as voltage of the output decreases, and
10 is well-suited for increasing the power amplifier's gain as power amplifier supply voltage decreases.

[0091] Figure 3 is a schematic diagram of a power amplifier 250 according to one embodiment. The power amplifier 250 includes an NFET 231, a Wilson current mirror 232, an input DC blocking capacitor 233, an output DC blocking capacitor 234, a choke inductor
15 235, and a reference current source 236.

[0092] Although Figure 3 depicts one embodiment of a power amplifier with adaptive bias, the teachings herein are applicable to power amplifiers implemented in a wide variety of ways.

[0093] The power amplifier 250 receives an RF input signal RF_{IN} at an RF input
20 terminal, and provides an amplified RF output signal RF_{OUT} to an RF output terminal. In the illustrated embodiment, the input DC blocking capacitor 233 is connected between the RF input terminal and the gate of the NFET 231 to allow biasing of the gate voltage of the NFET 231 separately from the DC voltage of the RF input terminal. Additionally, the output DC blocking capacitor 234 is connected between the drain of the NFET 231 and the RF output
25 terminal to decouple the drain voltage of the NFET 231 from the DC voltage of the RF output terminal.

[0094] As shown in Figure 3, the choke inductor 235 provides the power amplifier supply voltage V_{PA} to the drain of the NFET 231. The power amplifier supply voltage V_{PA} can be generated by an envelope tracker including, but not limited to, any of the envelope
30 trackers disclosed herein.

[0095] The NFET 231 amplifies the RF input signal RF_{IN} to generate the RF output signal RF_{OUT} . Additionally, the gate of the NFET 231 is biased by an internal voltage of the Wilson current mirror 232. Furthermore, the source of the NFET 231 receives a ground voltage (ground), while the drain of the NFET 231 receives the power amplifier supply voltage V_{PA} from the choke inductor 235. In certain implementations, the NFET 231 is implemented as an n-type metal oxide semiconductor (NMOS) transistor. For example, the NFET 231 can be a short channel NMOS transistor.

[0096] The Wilson current mirror 232 includes an input that receives a reference current I_{REF} from a reference current source 236, and an output connected to the power amplifier supply voltage V_{PA} . The Wilson current mirror 232 includes a first current mirror NFET 241, a second current mirror NFET 242, a third current mirror NFET 243, and a fourth current mirror NFET 244.

[0097] As shown in Figure 3, the first current mirror NFET 241 and the second current mirror 242 each include a source connected to ground. Additionally, a gate of the first current mirror NFET 241 is connected to a gate and a drain of the second current mirror NFET 242 as well as to a source of the fourth current mirror NFET 244. Additionally, the output of the Wilson current mirror 232 is connected to the drain of the fourth current mirror NFET 244, while the input of the Wilson current mirror 232 is connected to a gate of the fourth current mirror NFET 244 and to a gate and a drain of the third current mirror NFET 243. Furthermore, the drain of the first current mirror NFET 241 and the drain of the third current mirror NFET 243 are connected to one another.

[0098] In the illustrated embodiment, an internal voltage of the Wilson current mirror 232 is provided to the gate of the NFET 231 to provide adaptive biasing. The internal voltage corresponds to the drain voltage of the first current mirror NFET 241, in this embodiment.

[0099] The Wilson current mirror 232 operates to mirror the reference current I_{REF} received at the input to generate an output current provided at the output. As the power amplifier supply voltage V_{PA} changes due to envelope tracking, the drain voltage of the first current mirror NFET 241 also changes such that the output current tracks the input current. The regulation of the Wilson current mirror 232 results in the drain-to-source voltage of the first current source NFET 241 increasing as the power amplifier supply voltage V_{PA} decreases.

[0100] The drain voltage of the first current mirror NFET 241 is well-suited for increasing the power amplifier's gain as the power amplifier supply voltage V_{PA} decreases, and for decreasing the power amplifier's gain as the power amplifier supply voltage V_{PA} increases. Thus, the Wilson current mirror 232 provides adaptive biasing to the NFET 231 to
5 compensate for gain variation arising from power supply variation. Such adaptive biasing is well-suited for compensating for short channel effects (for instance, channel length modulation and/or drain-induced barrier lowering) when the NFET 231 is implemented as a short channel NMOS transistor.

[0101] Figure 4A is a graph of one example of power gain versus output power for
10 a power amplifier without adaptive bias.

[0102] Figure 4B is a graph of one example of power gain versus output power for a power amplifier with adaptive bias.

[0103] As shown by a comparison of Figure 4A and Figure 4B, adaptive biasing reduces variation in gain (for instance, from about 15 dB to about 3 dB, in this example).

[0104] Figure 4C is a graph of one example of quiescent drain current versus supply
15 voltage for a power amplifier without adaptive bias.

[0105] Figure 4D is a graph of one example of quiescent drain current versus supply voltage for a power amplifier with adaptive bias.

[0106] As shown by a comparison of Figure 4C and Figure 4D, adaptive biasing
20 reduces variation in quiescent drain current (for instance, from about 12x to about 1.25x, in this example).

[0107] Figure 5 is a schematic diagram of a power amplifier 280 according to another embodiment. The power amplifier 280 includes an NFET 231, a Wilson current mirror 232, an input DC blocking capacitor 233, an output DC blocking capacitor 234, a choke
25 inductor 235, a reference current source 236, and a buffer 270.

[0108] The power amplifier 280 of Figure 5 is similar to the power amplifier 250 of Figure 3, except that the power amplifier 280 further includes the buffer 270 for buffering the drain voltage of the first current mirror NFET 241 to generate the gate bias voltage of the NFET 231.

[0109] In the illustrated embodiment, the buffer 270 is implemented as a zero shift
30 buffer including a first depletion mode (d-mode) FET 271 and a second d-mode FET 272,

which can be, for example, junction field-effect transistors (JFETs) or Schottky gate FETs. The drain of the first d-mode FET 271 receives a battery voltage V_{BATT} , while a gate of the first d-mode FET 271 receives the internal voltage of the Wilson current mirror 232. Additionally, the gate and source of the second d-mode FET 272 are connected to ground, while the drain of the second d-mode FET 272 is connected to a source of the first d-mode FET 271 at a node that outputs the gate bias voltage for biasing the power amplifier's NFET 231.

[0110] By including the buffer 270, enhanced bandwidth and improved transient response of the power amplifier's biasing circuitry is achieved.

[0111] Figure 6A is a graph of one example of amplitude distortion versus load power for a power amplifier with adaptive bias but without a buffer.

[0112] Figure 6B is a graph of one example of amplitude distortion versus load power for a power amplifier with adaptive bias and with a buffer.

[0113] As shown by a comparison of Figure 6A and Figure 6B, using a buffer in combination with adaptive biasing reduces amplitude distortion (AM-to-AM).

[0114] Figure 6C is a graph of one example of phase distortion versus load power for a power amplifier with adaptive bias but without a buffer.

[0115] Figure 6D is a graph of one example of phase distortion versus load power for a power amplifier with adaptive bias and with a buffer.

[0116] As shown by a comparison of Figure 6C and Figure 6D, using a buffer in combination with adaptive biasing reduces phase distortion (AM-to-PM).

[0117] Figure 7A is a graph of one example of drain current versus drain voltage for a short channel MOS transistor. Various plots are depicted of drain current versus drain voltage at different gate-to-source voltages of the short channel MOS transistor. Plots are included both without taking into account channel length modulation (dashed line plots) and with taking into account channel length modulation (solid line plots).

[0118] Figure 7B is a graph of one example of drain current versus gate voltage for a short channel MOS transistor. The graph depicts one example of a shift in transistor threshold voltage arising from drain-induced barrier lowering.

[0119] Figures 8A-8B show two examples of power amplifier supply voltage versus time.

[0120] In Figure 8A, a graph 447 illustrates one example of the voltage of an RF signal 441 and a power amplifier supply voltage 443 versus time. The RF signal 441 has an envelope 442.

[0121] It can be important that the power amplifier supply voltage 443 of a power amplifier has a voltage greater than that of the RF signal 441. For example, powering a power amplifier using a power amplifier supply voltage that has a magnitude less than that of the RF signal can clip the RF signal, thereby creating signal distortion and/or other problems. Thus, it can be important the power amplifier supply voltage 443 be greater than that of the envelope 442. However, it can be desirable to reduce a difference in voltage between the power amplifier supply voltage 443 and the envelope 442 of the RF signal 441, as the area between the power amplifier supply voltage 443 and the envelope 442 can represent lost energy, which can reduce battery life and increase heat generated in a wireless device.

[0122] In Figure 8B, a graph 448 illustrates another example of the voltage of an RF signal 441 and a power amplifier supply voltage 444 versus time. In contrast to the power amplifier supply voltage 443 of Figure 8A, the power amplifier supply voltage 444 of Figure 8B changes in relation to the envelope 442 of the RF signal 441. The area between the power amplifier supply voltage 444 and the envelope 442 in Figure 8B is less than the area between the power amplifier supply voltage 443 and the envelope 442 in Figure 8A, and thus the graph 448 of Figure 8B can be associated with a power amplifier having greater energy efficiency.

[0123] Figure 9A is a schematic diagram of an envelope tracking system 500 according to one embodiment. The envelope tracking system 500 includes a power amplifier 501 and an envelope tracker 502. The power amplifier 501 provides amplification to a radio frequency signal 503.

[0124] The envelope tracker 502 receives an envelope signal 504 corresponding to an envelope of the radio frequency signal 503. Additionally, the envelope tracker 502 generates a power amplifier supply voltage V_{PA} , which supplies power to the power amplifier 501.

[0125] The illustrated envelope tracker 502 includes a DC-to-DC converter 511 and an error amplifier 512 that operate in combination with one another to generate the power amplifier supply voltage V_{PA} based on the envelope signal 504. In the illustrated embodiment,

an output of the DC-to-DC converter 511 and an output of the error amplifier 512 are combined using a combiner 515.

5 **[0126]** The envelope tracker 502 of Figure 9A illustrates one example of analog envelope tracking, in which a switching regulator operate in parallel with one another to track an envelope of an RF signal.

[0127] Figure 9B is a schematic diagram of an envelope tracking system 540 according to another embodiment. The envelope tracking system 540 includes a power amplifier 501 and an envelope tracker 532. The power amplifier 501 provides amplification to a radio frequency signal 503.

10 **[0128]** The envelope tracker 532 receives an envelope signal 504 corresponding to an envelope of the radio frequency signal 503. Additionally, the envelope tracker 532 generates a power amplifier supply voltage V_{PA} , which supplies power to the power amplifier 501.

[0129] The illustrated envelope tracker 532 includes a multi-level switching circuit 15 535. In certain implementations, the multi-level switching circuit includes a multi-output DC-to-DC converter for generating regulated voltages of different voltage levels, switches for controlling selection of a suitable regulated voltage over time based on the envelope signal, and a filter for filtering the output of the switches to generate the power amplifier supply voltage.

20 **[0130]** The envelope tracker 532 of Figure 9B illustrates one example of MLS envelope tracking.

[0131] Figure 10 is a schematic diagram of an envelope tracking system 600 according to another embodiment. The envelope tracking system 600 includes a power amplifier 501 and an envelope tracker 602. The power amplifier 501 provides amplification 25 to a radio frequency signal 503.

[0132] The envelope tracker 602 receives an envelope signal corresponding to an envelope of the radio frequency signal 503. In this example, the envelope signal is differential. Additionally, the envelope tracker 602 generates a power amplifier supply voltage V_{PA} , which supplies power to the power amplifier 501.

30 **[0133]** The illustrated envelope tracker 602 includes an envelope amplifier 611, a first comparator 621, a second comparator 622, a third comparator 623, a coding and dithering

circuit 624, a multi-output boost switcher 625, a filter 626, a switch bank 627, and a capacitor bank 630. The capacitor bank 630 includes a first capacitor 631, a second capacitor 632, and a third capacitor 633. Additionally, the switch bank 627 includes a first switch 641, a second switch 642, and a third switch 643.

5 **[0134]** The envelope amplifier 611 amplifies the envelope signal to provide an amplified envelope signal to the first to third comparators 621-623. The first to third comparators 621-623 compare the amplified envelope signal to a first threshold T1, a second threshold T2, and a third threshold T3, respectively. The results of the comparisons are provided to the coding and dithering circuit 624, which processes the results to control
10 selection of switches of the switch bank 627. The coding and dithering circuit 624 can activate the switches while using coding and/or dithering to reduce artifacts arising from opening and closing the switches.

[0135] Although an example with three comparators is shown, more or fewer comparators can be used. Furthermore, the coding and dithering circuit 624 can be omitted in
15 favor of controlling the switch bank in other ways. In a first example, coding but not dithering is used. In a second example, dithering but not coding is used. In a third example, neither coding nor dithering is used.

[0136] The multi-output boost switcher 625 generates a first regulated voltage V_{MLS1} , a second regulated voltage V_{MLS2} , and a third regulated voltage V_{MLS3} based on
20 providing DC-to-DC conversion of a battery voltage V_{BATT} . Although an example with three regulated voltages is shown, the multi-output boost switcher 625 can generate more or fewer regulated voltages. In certain implementations, at least a portion of the regulated voltages are boosted relative to the battery voltage V_{BATT} . In some configurations, one or more of the regulated voltages is a buck voltage having a voltage lower than the battery voltage V_{BATT} .

25 **[0137]** The capacitor bank 630 aids in stabilizing the regulated voltages generated by the multi-output boost switcher 625. For example, the capacitors 631-633 operate as decoupling capacitors.

[0138] The filter 626 processes the output of the switch bank 627 to generate the power amplifier supply voltage V_{PA} . By controlling the selection of the switches 641-643 over
30 time based on the envelope signal, the power amplifier supply voltage V_{PA} is generated to track the envelope signal.

[0139] Figure 11A is a schematic diagram of one embodiment of a packaged module 800. Figure 11B is a schematic diagram of a cross-section of the packaged module 800 of Figure 11A taken along the lines 11B–11B.

5 [0140] The packaged module 800 includes an IC or die 801, surface mount components 803, wirebonds 808, a package substrate 820, and encapsulation structure 840. The package substrate 820 includes pads 806 formed from conductors disposed therein. Additionally, the die 801 includes pads 804, and the wirebonds 808 have been used to electrically connect the pads 804 of the die 801 to the pads 806 of the package substrate 801.

10 [0141] The die 801 includes a power amplifier 846, which can be implemented in accordance with any of the embodiments herein.

[0142] The packaging substrate 820 can be configured to receive a plurality of components such as the die 801 and the surface mount components 803, which can include, for example, surface mount capacitors and/or inductors.

15 [0143] As shown in Figure 11B, the packaged module 800 is shown to include a plurality of contact pads 832 disposed on the side of the packaged module 800 opposite the side used to mount the die 801. Configuring the packaged module 800 in this manner can aid in connecting the packaged module 800 to a circuit board such as a phone board of a wireless device. The example contact pads 832 can be configured to provide RF signals, bias signals, power low voltage(s) and/or power high voltage(s) to the die 801 and/or the surface mount
20 components 803. As shown in Figure 11B, the electrically connections between the contact pads 832 and the die 801 can be facilitated by connections 833 through the package substrate 820. The connections 833 can represent electrical paths formed through the package substrate 820, such as connections associated with vias and conductors of a multilayer laminated package substrate.

25 [0144] In some embodiments, the packaged module 800 can also include one or more packaging structures to, for example, provide protection and/or facilitate handling of the packaged module 800. Such a packaging structure can include overmold or encapsulation structure 840 formed over the packaging substrate 820 and the components and die(s) disposed thereon.

30 [0145] It will be understood that although the packaged module 800 is described in the context of electrical connections based on wirebonds, one or more features of the present

disclosure can also be implemented in other packaging configurations, including, for example, flip-chip configurations.

[0146] Figure 12 is a schematic diagram of one embodiment of a phone board 900. The phone board 900 includes the module 800 shown in Figures 10A-10B attached thereto. Although not illustrated in Figure 12 for clarity, the phone board 800 can include additional components and structures.

Applications

[0147] Some of the embodiments described above have provided examples in connection with wireless devices or mobile phones. However, the principles and advantages of the embodiments can be used for any other systems or apparatus that have needs for power amplifiers.

[0148] Such envelope trackers can be implemented in various electronic devices. Examples of the electronic devices can include, but are not limited to, consumer electronic products, parts of the consumer electronic products, electronic test equipment, etc. Examples of the electronic devices can also include, but are not limited to, memory chips, memory modules, circuits of optical networks or other communication networks, and disk driver circuits. The consumer electronic products can include, but are not limited to, a mobile phone, a telephone, a television, a computer monitor, a computer, a hand-held computer, a personal digital assistant (PDA), a microwave, a refrigerator, an automobile, a stereo system, a cassette recorder or player, a DVD player, a CD player, a VCR, an MP3 player, a radio, a camcorder, a camera, a digital camera, a portable memory chip, a washer, a dryer, a washer/dryer, a copier, a facsimile machine, a scanner, a multi-functional peripheral device, a wrist watch, a clock, etc. Further, the electronic devices can include unfinished products.

Conclusion

[0149] Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word “coupled”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more

intermediate elements. Likewise, the word “connected”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words “herein,” “above,” “below,” and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word “or” in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0150] Moreover, conditional language used herein, such as, among others, "can," "could," "might," "can," "e.g.," "for example," "such as" and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0151] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0152] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0153] While certain embodiments of the inventions have been described, these
5 embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are
10 intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. A mobile device comprising:

a transceiver configured to generate a radio frequency signal;

5 a power management system including an envelope tracker configured to generate a power amplifier supply voltage that changes in relation to an envelope of the radio frequency signal; and

a front end system including a power amplifier configured to amplify the radio frequency signal and to receive power from the power amplifier supply voltage, the power amplifier including a current mirror having an input configured to receive a reference current and an output electrically connected to the power amplifier supply voltage, and a field-effect transistor configured to amplify the radio frequency signal and having a gate biased based on an internal voltage of the current mirror.

15 2. The mobile device of claim 1 wherein the internal voltage of the current mirror increases in response to a decrease of the power amplifier supply voltage, and decreases in response to an increase of the power amplifier supply voltage.

20 3. The mobile device of claim 1 wherein the field-effect transistor is a short channel metal oxide semiconductor transistor.

4. The mobile device of claim 1 wherein the power amplifier further includes a choke inductor electrically connected between the power amplifier supply voltage and a drain of the field-effect transistor.

25 5. The mobile device of claim 1 wherein the current mirror is a Wilson current mirror.

30 6. The mobile device of claim 1 wherein the power amplifier further includes a buffer configured to buffer the internal voltage of the current mirror to generate a gate bias voltage of the field-effect transistor.

7. The mobile device of claim 6 wherein the buffer includes a first depletion-mode transistor and a second depletion-mode transistor configured to provide buffering with a zero shift.

5 8. The mobile device of claim 1 wherein the current mirror includes a first mirror transistor having a drain configured to output the internal voltage, a second mirror transistor, a third mirror transistor, and a fourth mirror transistor, the third mirror transistor and the first mirror transistor connected in series between the input of the current mirror and a ground voltage, and the fourth mirror transistor and the second mirror transistor connected in series
10 between the output of the current mirror and the ground voltage.

 9. The mobile device of claim 8 wherein a gate of the first mirror transistor is connected to a gate of the second mirror transistor, and a gate of the third mirror transistor is connected to a gate of the fourth mirror transistor.

15 10. The mobile device of claim 9 wherein a drain of the second mirror transistor is connected to the gate of the second mirror transistor, and a drain of the third mirror transistor is connected to the gate of the third mirror transistor.

20 11. The mobile device of claim 1 wherein the power amplifier further includes a current source configured to generate the reference current.

 12. An envelope tracking system comprising:

 an envelope tracker configured to generate a power amplifier supply voltage
25 that changes in relation to an envelope of a radio frequency signal; and

 a power amplifier configured to amplify the radio frequency signal and to receive power from the power amplifier supply voltage, the power amplifier including a current mirror having an input configured to receive a reference current and an output electrically connected to the power amplifier supply voltage, and a field-effect
30 transistor configured to amplify the radio frequency signal and having a gate biased based on an internal voltage of the current mirror.

13. The envelope tracking system of claim 12 wherein the internal voltage of the current mirror increases in response to a decrease of the power amplifier supply voltage, and decreases in response to an increase of the power amplifier supply voltage.

5 14. The envelope tracking system of claim 12 wherein the field-effect transistor is a short channel metal oxide semiconductor transistor.

15. The envelope tracking system of claim 12 wherein the current mirror is a Wilson current mirror.

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16. The envelope tracking system of claim 12 wherein the power amplifier further includes a buffer configured to buffer the internal voltage of the current mirror to generate a gate bias voltage of the field-effect transistor.

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17. The envelope tracking system of claim 12 wherein the current mirror includes a first mirror transistor having a drain configured to output the internal voltage, a second mirror transistor, a third mirror transistor, and a fourth mirror transistor, the third mirror transistor and the first mirror transistor connected in series between the input of the current mirror and a ground voltage, and the fourth mirror transistor and the second mirror transistor connected in series between the output of the current mirror and the ground voltage.

20

18. A method of radio frequency signal amplification in a mobile device, the method comprising:

25

generating a power amplifier supply voltage that changes in relation to an envelope of a radio frequency signal using an envelope tracker;

powering a power amplifier using the power amplifier supply voltage;

amplifying the radio frequency signal using a field-effect transistor of the power amplifier; and

30

generating a gate bias voltage of the field-effect transistor using an internal voltage of a current mirror of the power amplifier, including providing a reference current to an input of the current mirror and providing the power amplifier supply voltage to an output of the current mirror.

19. The method of claim 18 further comprising increasing the internal voltage of the current mirror in response to a decrease of the power amplifier supply voltage, and decreasing the internal voltage of the current mirror in response to an increase of the power amplifier supply voltage.

5

20. The method of claim 18 further comprising buffering the internal voltage of the current mirror to generate the gate bias voltage of the field-effect transistor.