FIG. 1

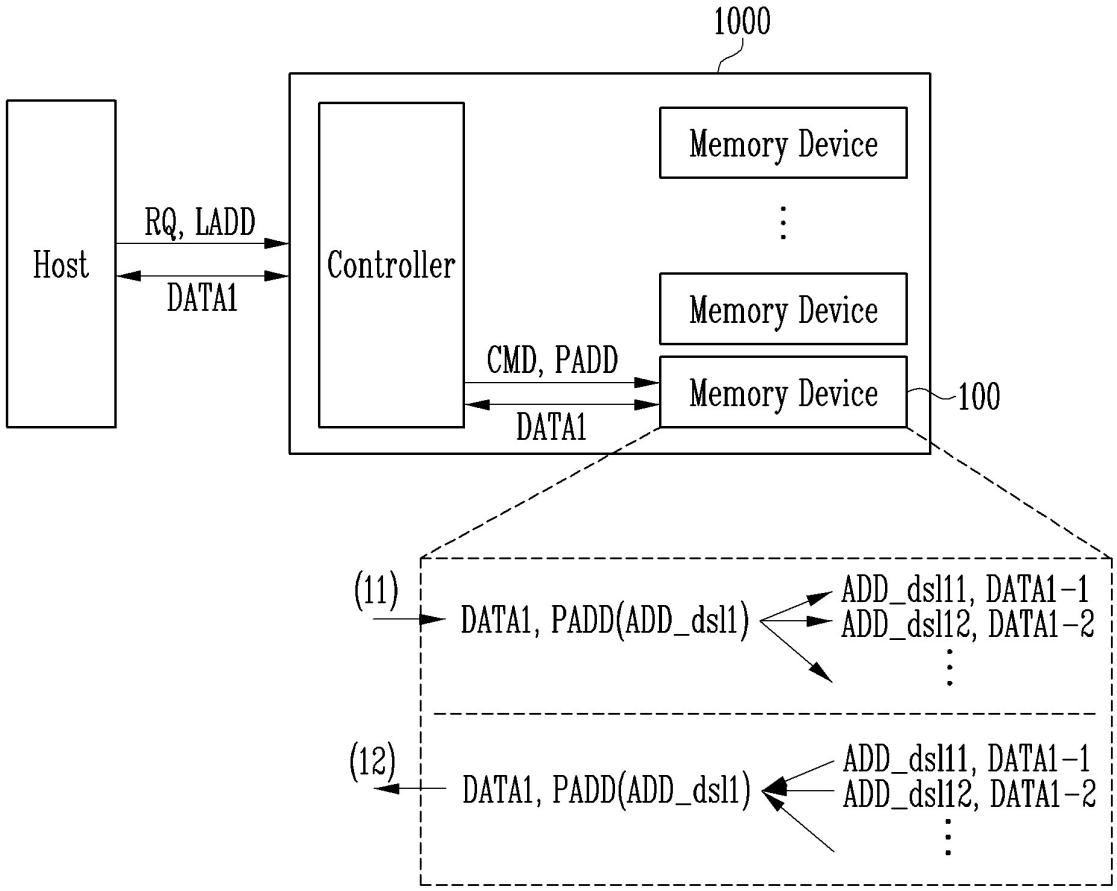

1000
Host
RQ, LADD
DATA1
Controller
Memory Device
Memory Device
Memory Device
CMD, PADD
DATA1
100
(11)
DATA1, PADD(ADD_dsl1)
ADD_dsl11, DATA1-1
ADD_dsl12, DATA1-2
(12)
DATA1, PADD(ADD_dsl1)
ADD_dsl11, DATA1-1
ADD_dsl12, DATA1-2

FIG. 2

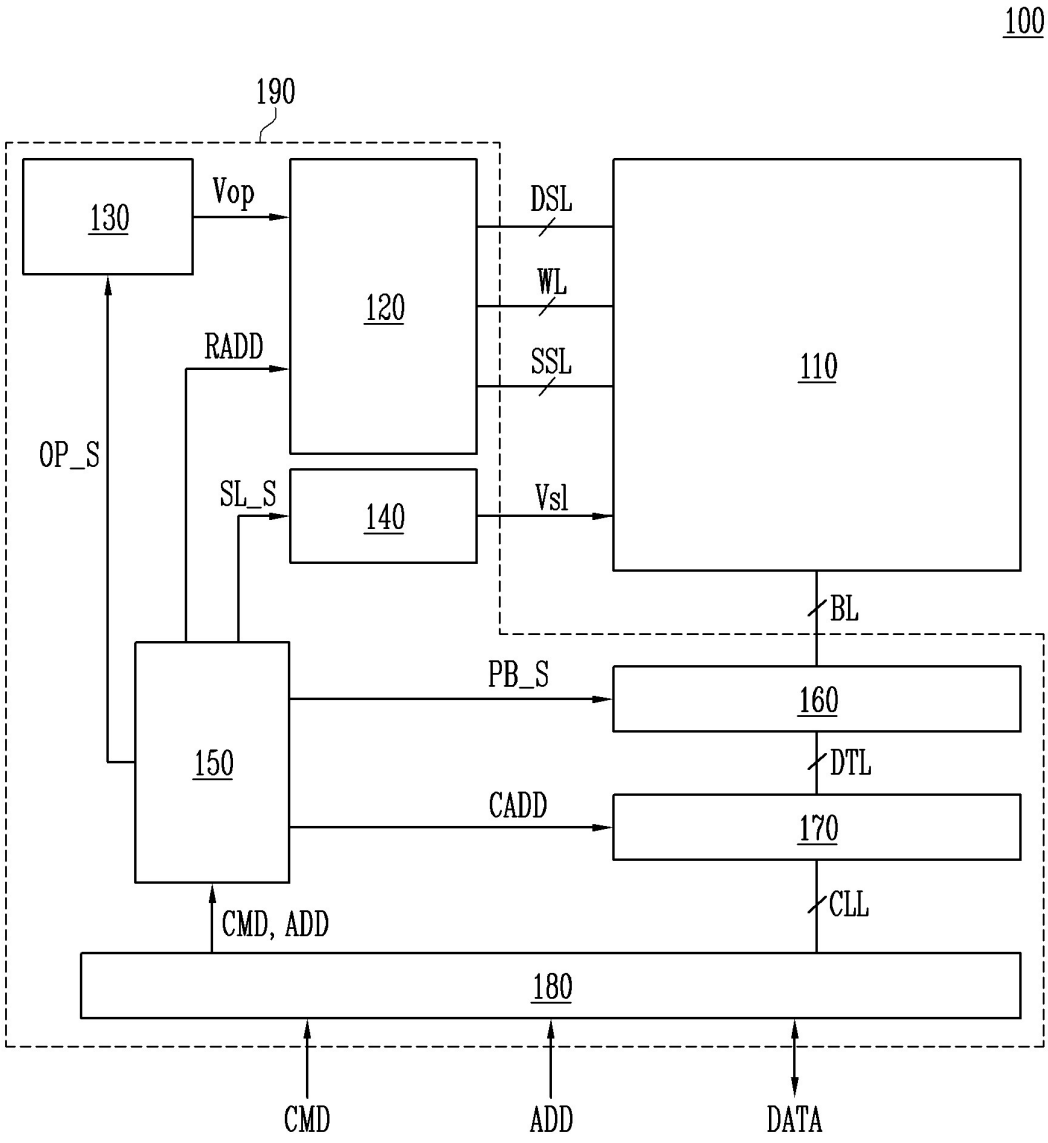

100
190
130
Vop
120
DSL
WL
SSL
110
RADD
OP_S
SL_S
140
Vsl
BL
PB_S
160
150
DTL
CADD
170
CLL
CMD, ADD
180
CMD
ADD
DATA

FIG. 3

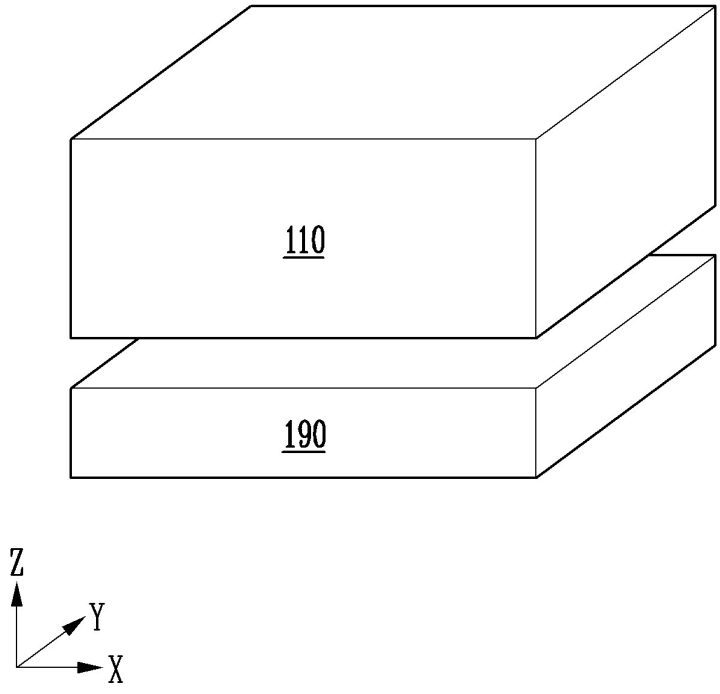


FIG. 4

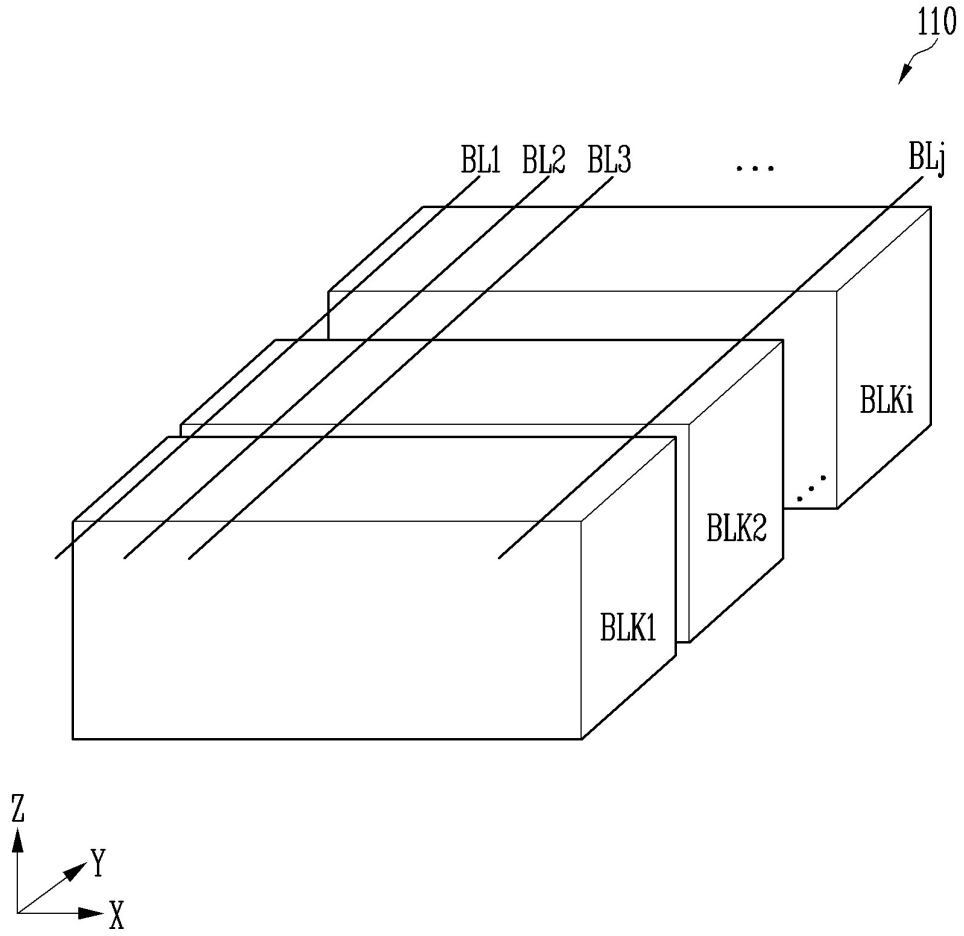


FIG. 5

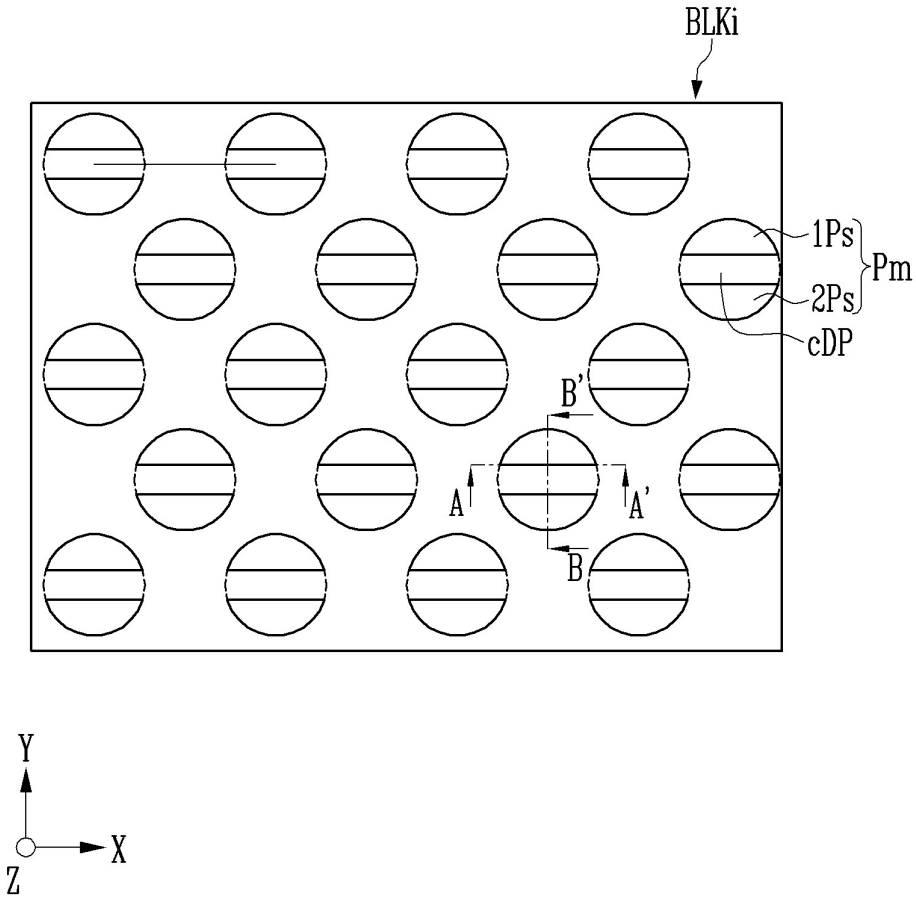


FIG. 6

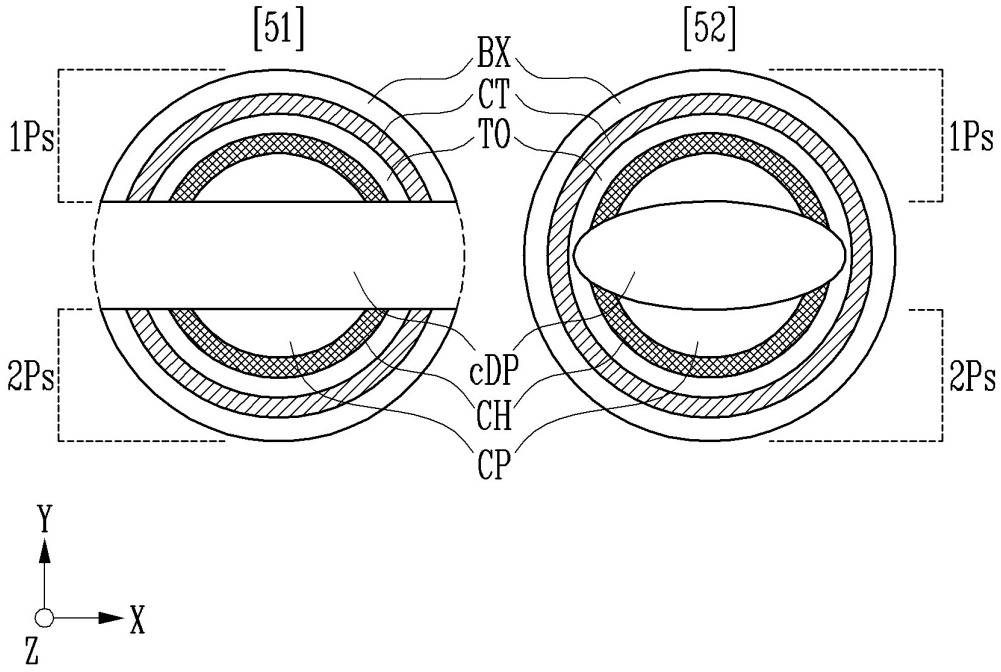


FIG. 7

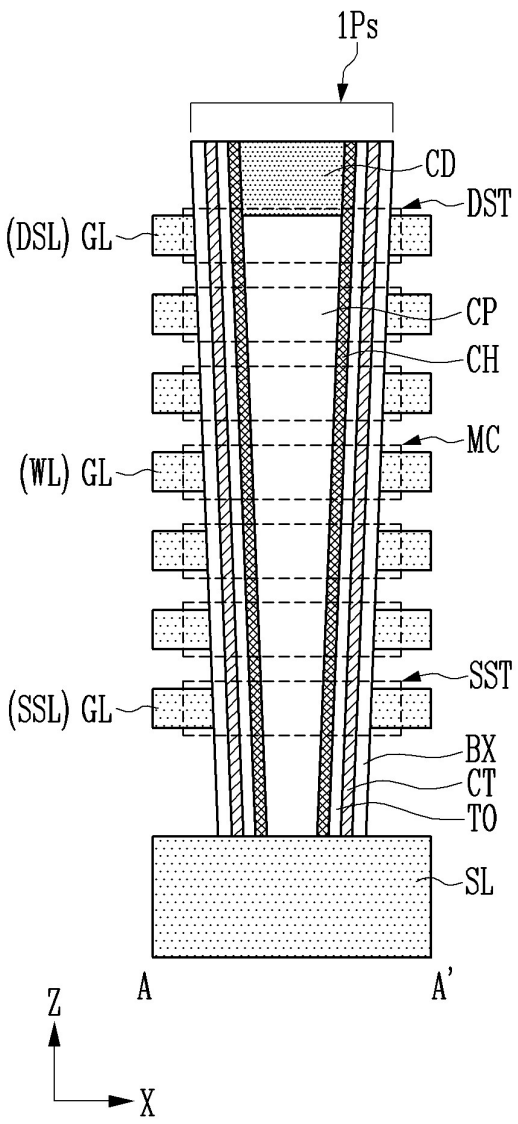

1Ps
CD
DST
(DSL) GL
CP
CH
MC
(WL) GL
SST
(SSL) GL
BX
CT
TO
SL
A
A'
Z
X

FIG. 8

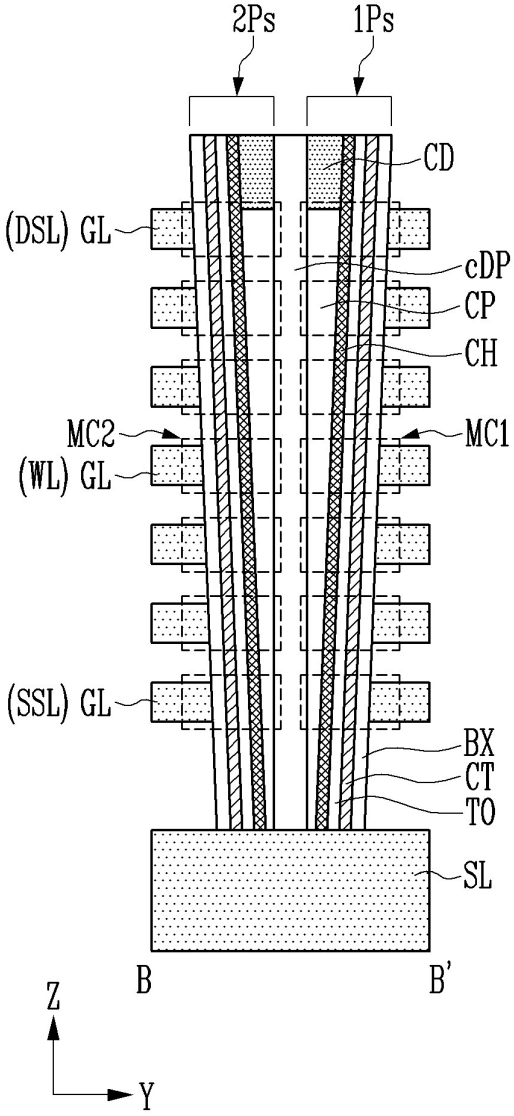

2Ps
1Ps
CD
(DSL) GL
cDP
CP
CH
MC2
MC1
(WL) GL
(SSL) GL
BX
CT
TO
SL
B
B'
Z
Y

FIG. 9

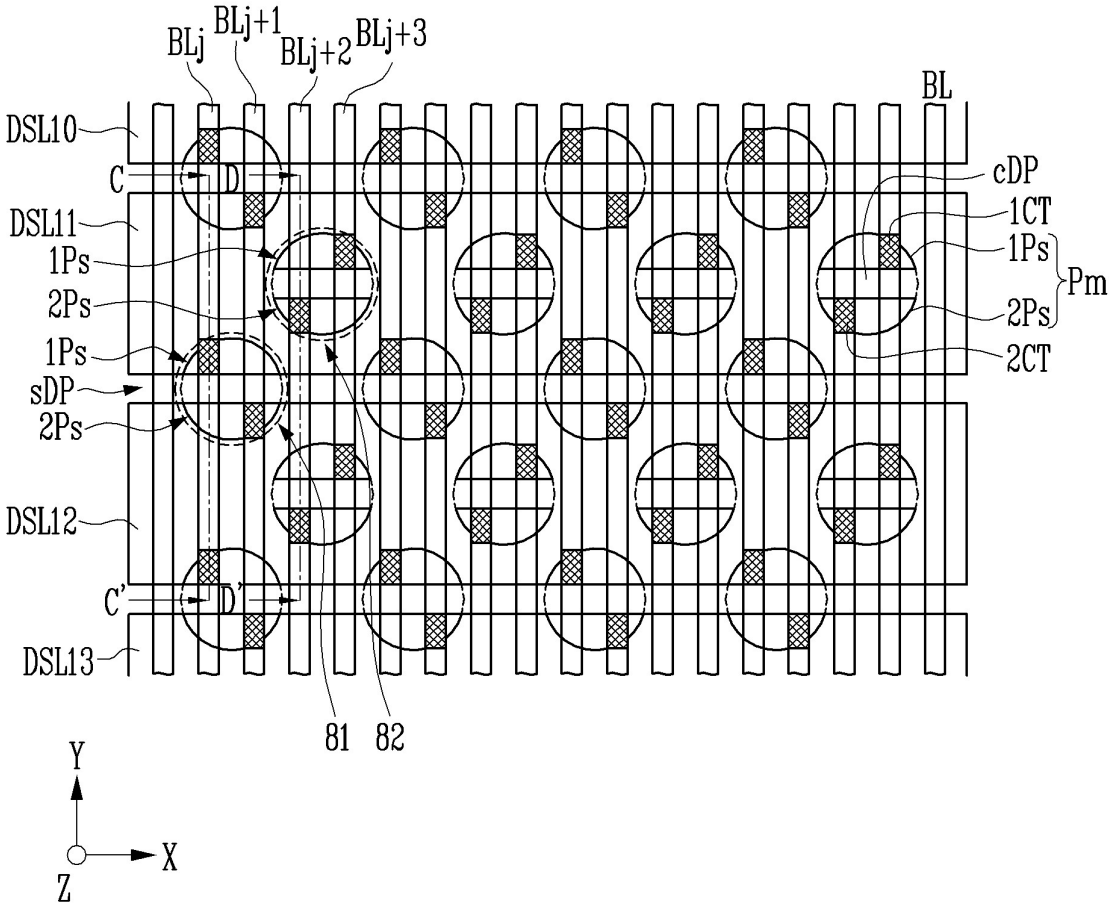

BLj
BLj+1
BLj+2
BLj+3
BL
DSL10
C
D
cDP
1CT
DSL11
1Ps
1Ps
Pm
2Ps
2Ps
1Ps
2CT
sDP
2Ps
DSL12
C'
D'
DSL13
81
82
Y
X
Z

FIG. 10

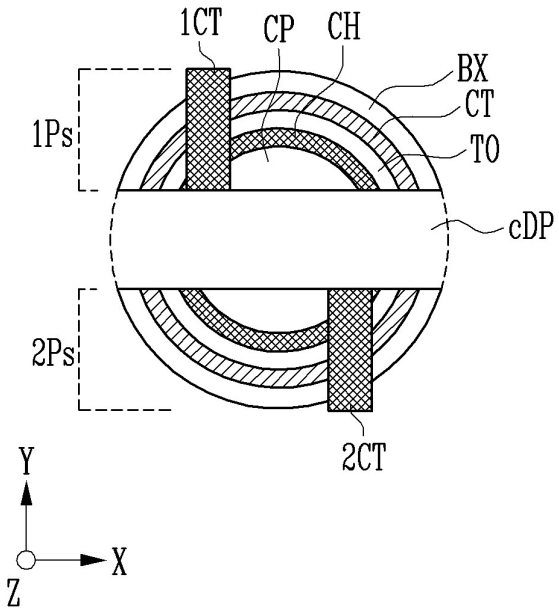


FIG. 11A

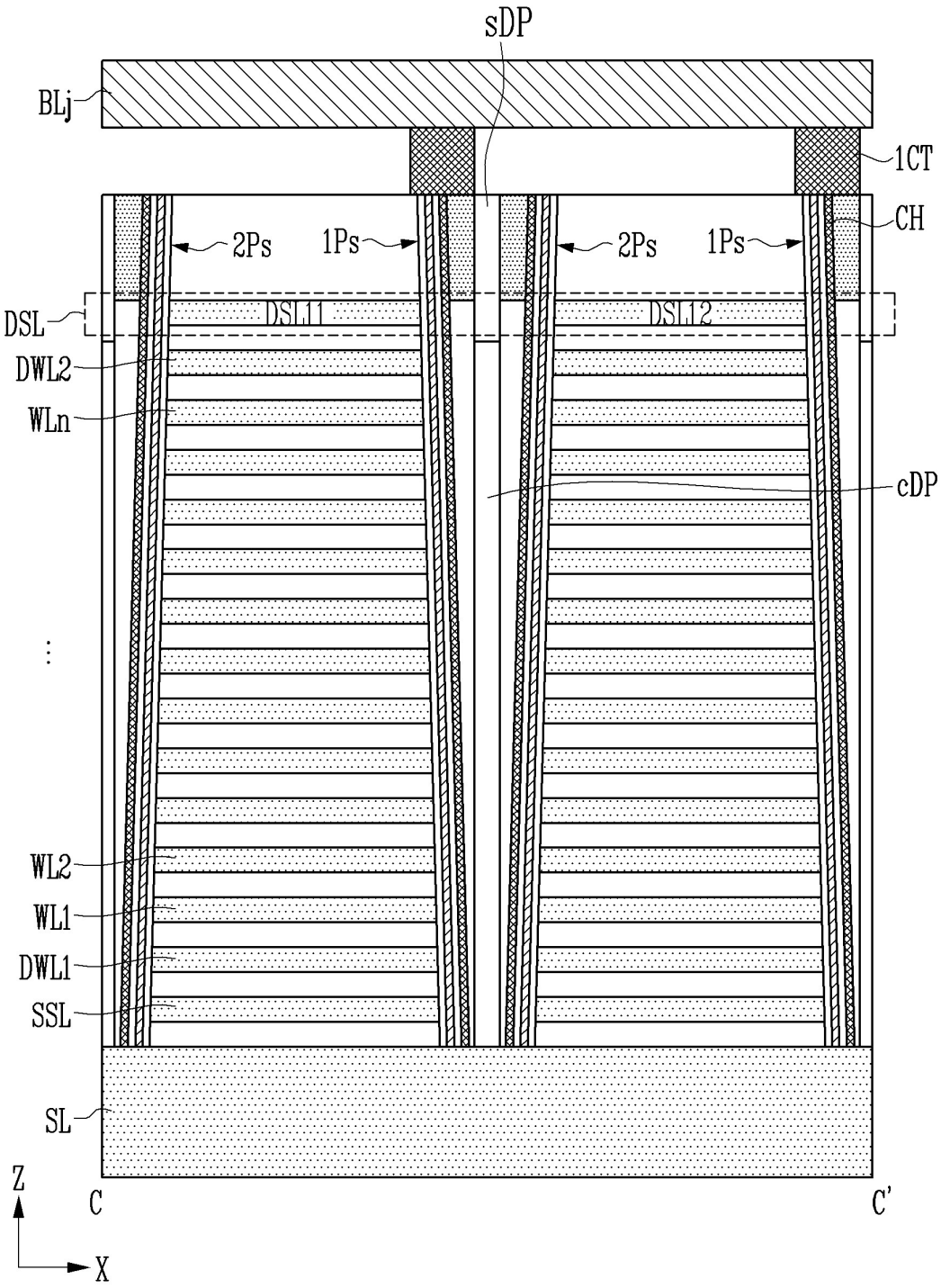

sDP
BLj
1CT
CH
2Ps
1Ps
2Ps
1Ps
DSL
DSL11
DSL12
DWL2
WLn
cDP
WL2
WL1
DWL1
SSL
SL
Z
C
C'
X

FIG. 11B

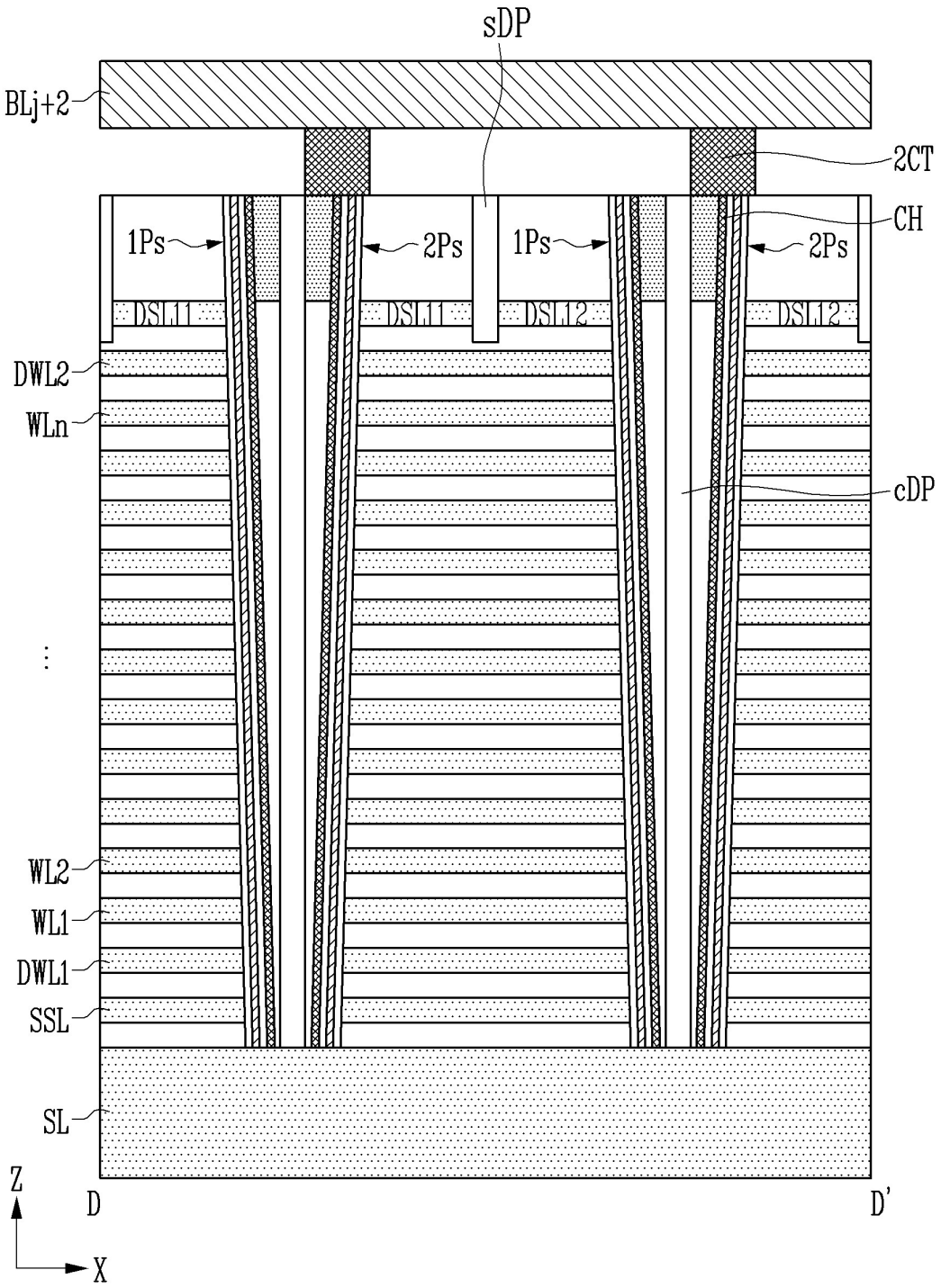

sDP
BLj+2
2CT
CH
1Ps
2Ps
1Ps
2Ps
DSL11
DSL11
DSL12
DSL12
DWL2
WLn
cDP
WL2
WL1
DWL1
SSL
SL
Z
X
D
D'

FIG. 12

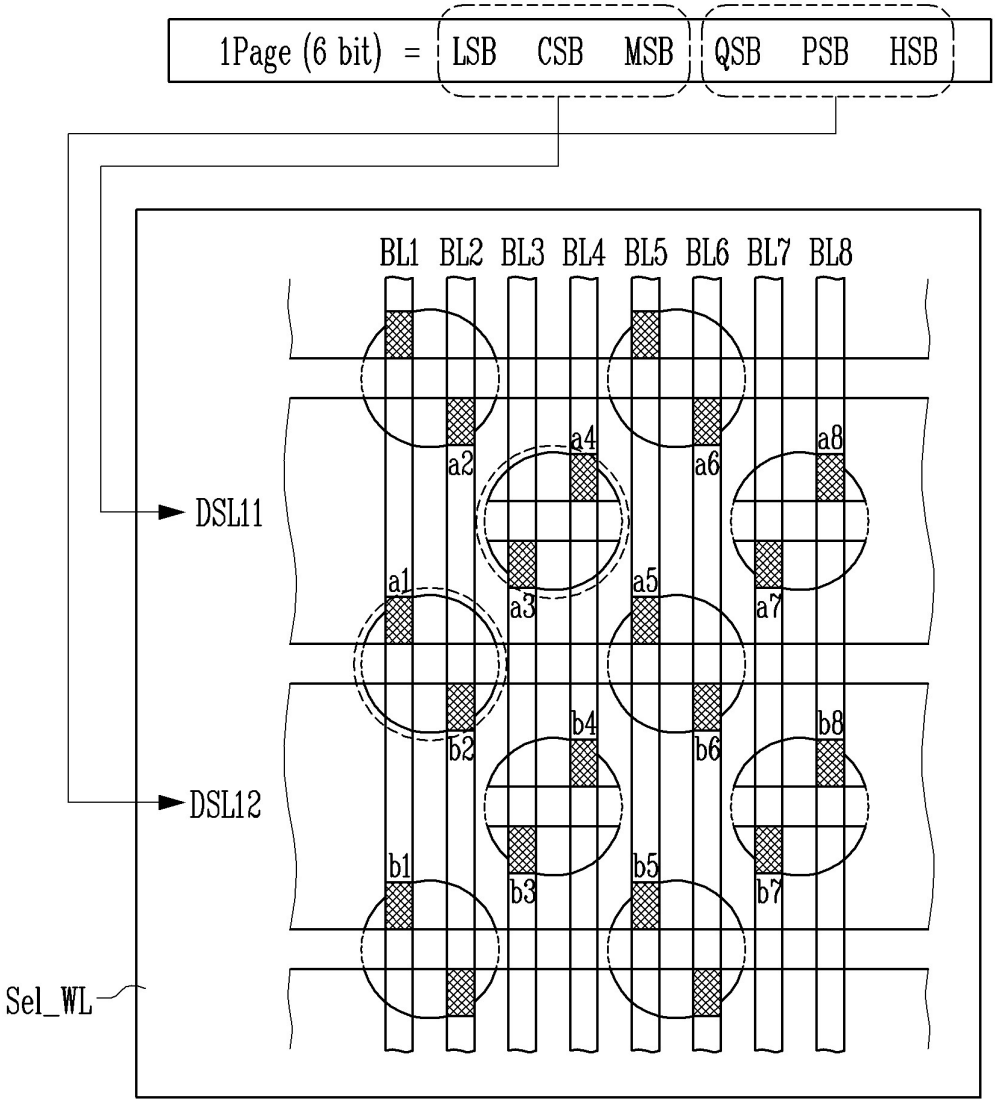

1Page (6 bit) = LSB CSB MSB QSB PSB HSB
BL1 BL2 BL3 BL4 BL5 BL6 BL7 BL8
DSL11
DSL12
Sel_WL
a1
a2
a3
a4
a5
a6
a7
a8
b1
b2
b3
b4
b5
b6
b7
b8

FIG. 13

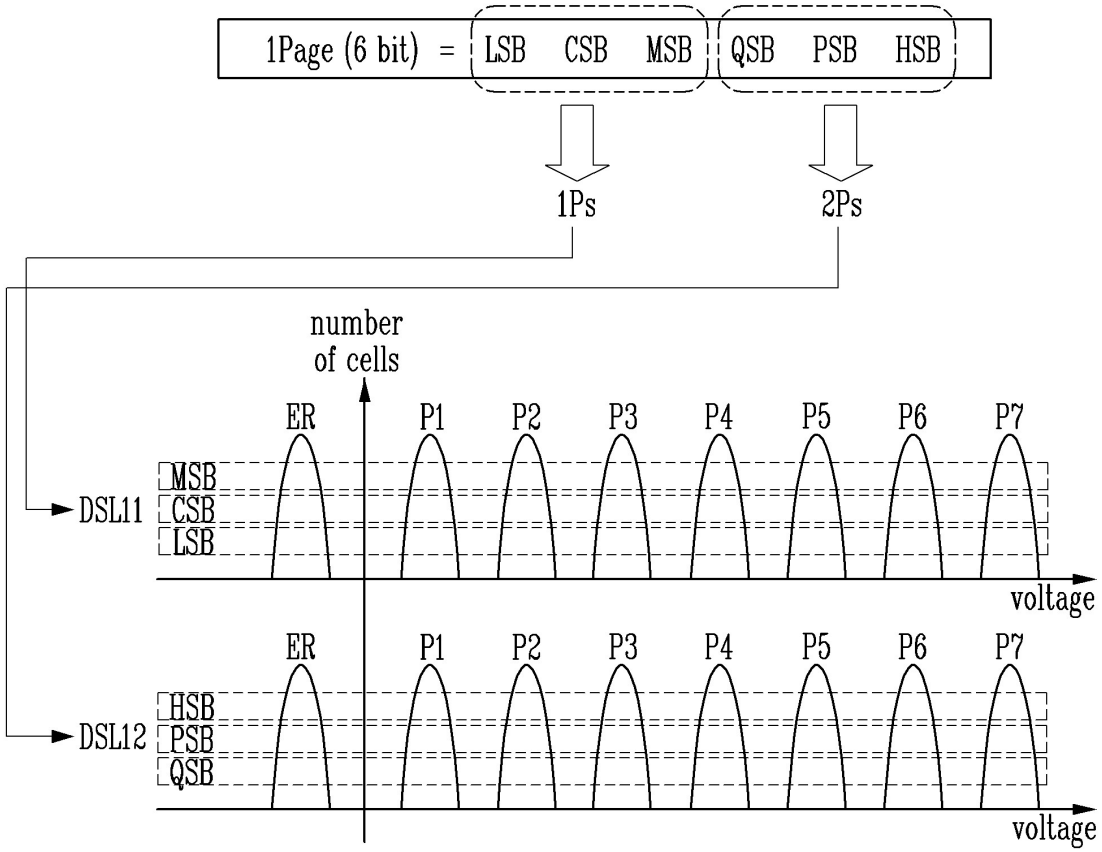

1Page (6 bit) = LSB CSB MSB QSB PSB HSB
1Ps
2Ps
number of cells
ER P1 P2 P3 P4 P5 P6 P7
MSB
CSB
LSB
DSL11
voltage
ER P1 P2 P3 P4 P5 P6 P7
HSB
PSB
QSB
DSL12
voltage

FIG. 14

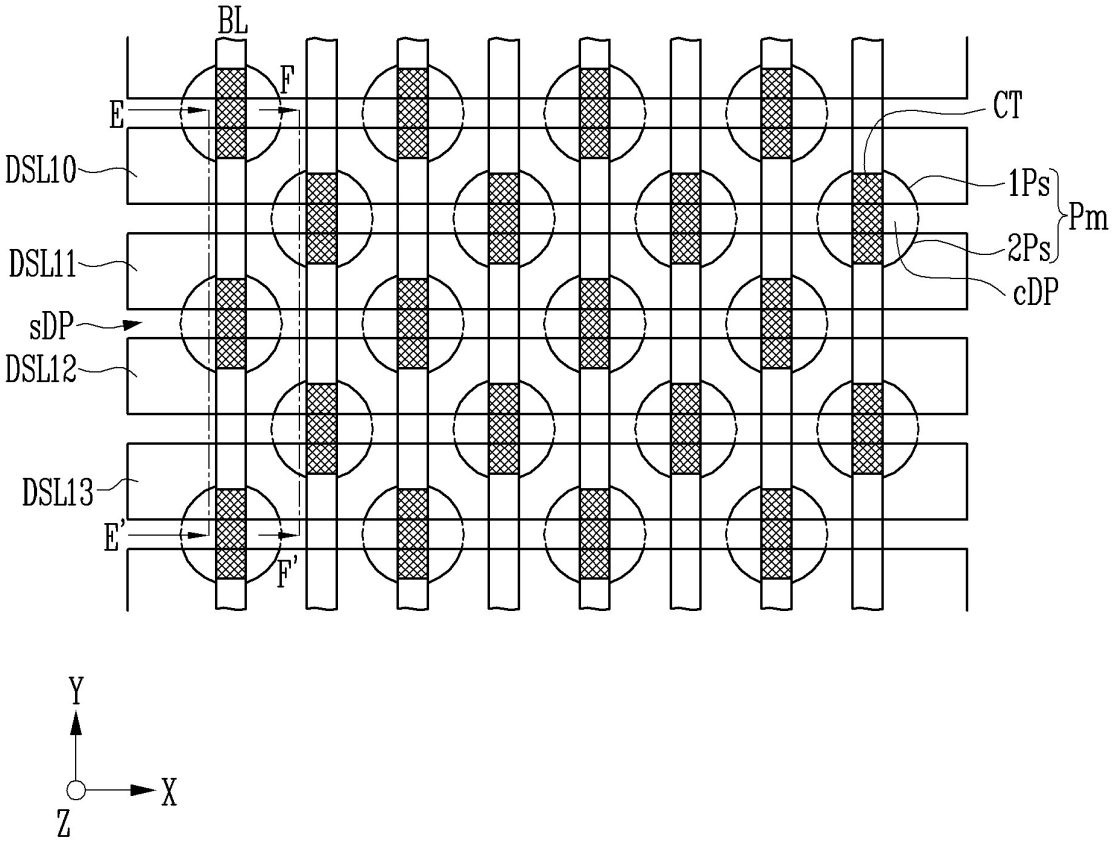


FIG. 15

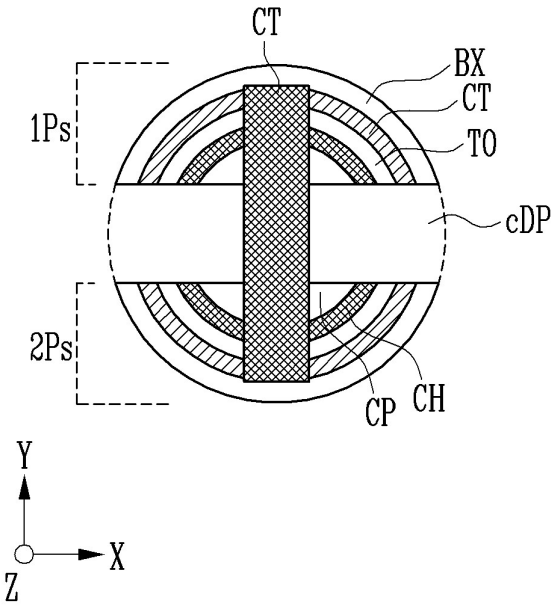


FIG. 16A

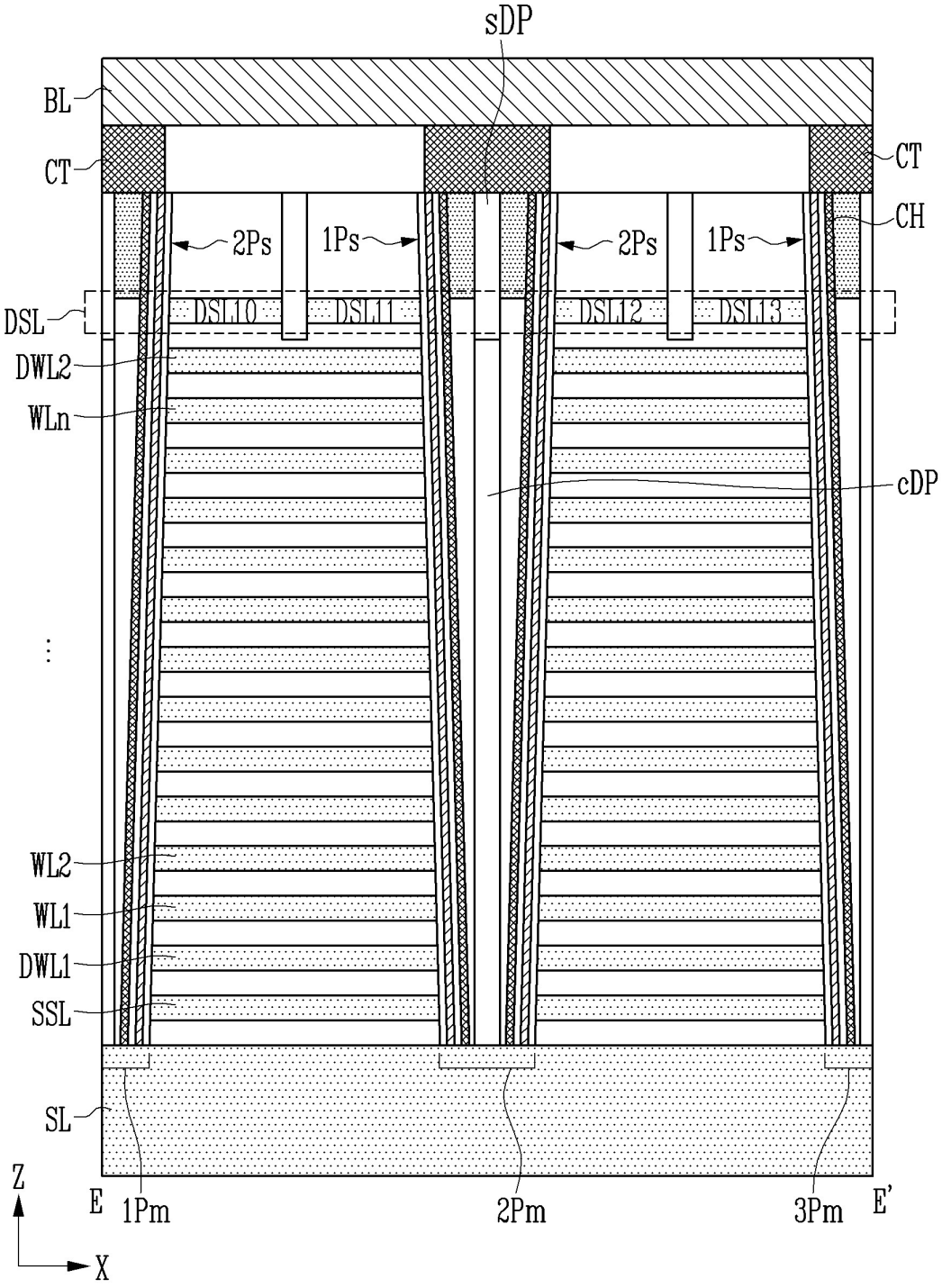

sDP
BL
CT
CT
CH
2Ps
1Ps
2Ps
1Ps
DSL
DSL10
DSL11
DSL12
DSL13
DWL2
WLn
cDP
WL2
WL1
DWL1
SSL
SL
Z
X
E
1Pm
2Pm
3Pm
E'

FIG. 16B

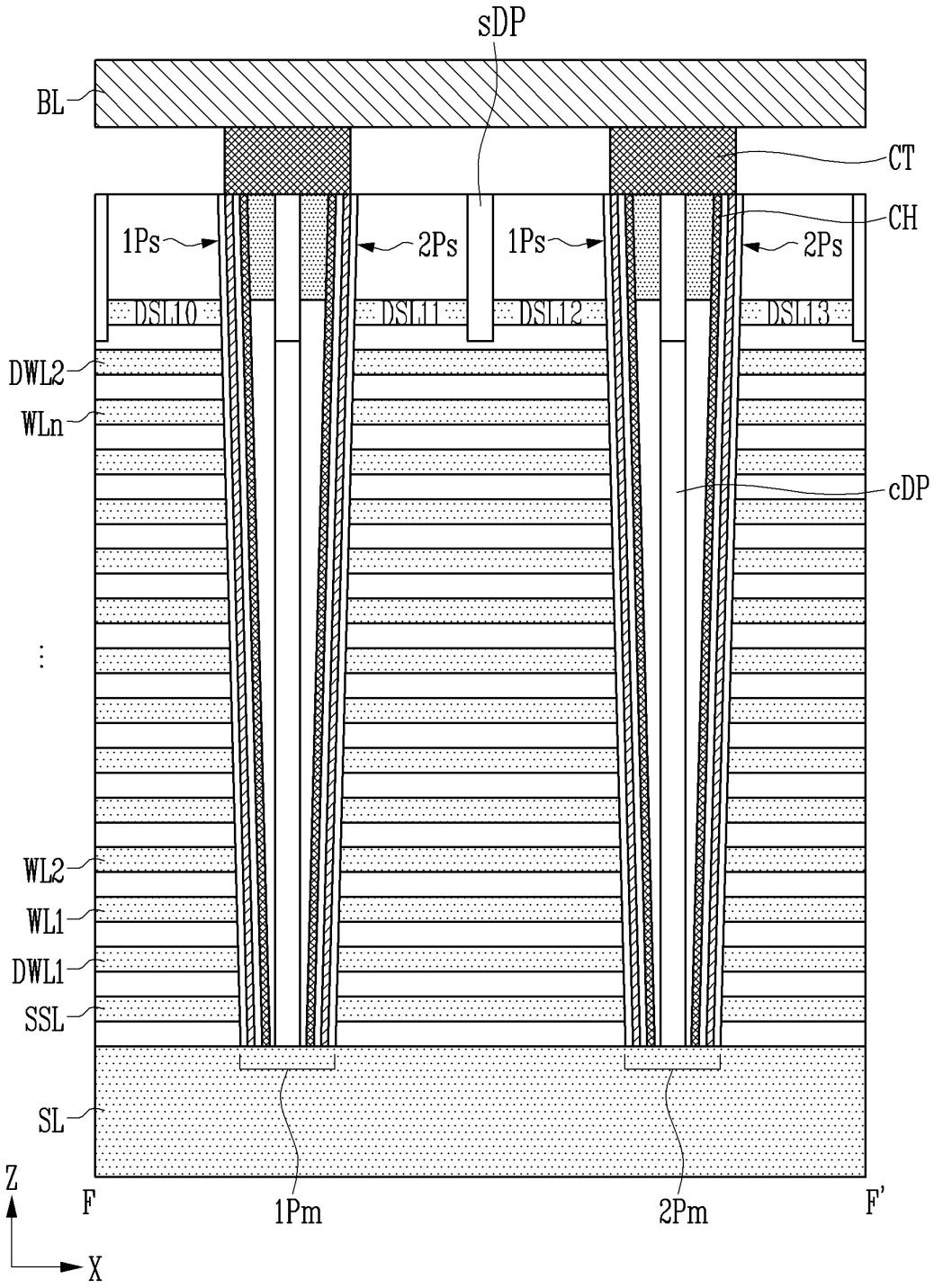

sDP
BL
CT
CH
1Ps
2Ps
1Ps
2Ps
DSL10
DSL11
DSL12
DSL13
DWL2
WLn
cDP
WL2
WL1
DWL1
SSL
SL
Z
X
F
1Pm
2Pm
F'

FIG. 17

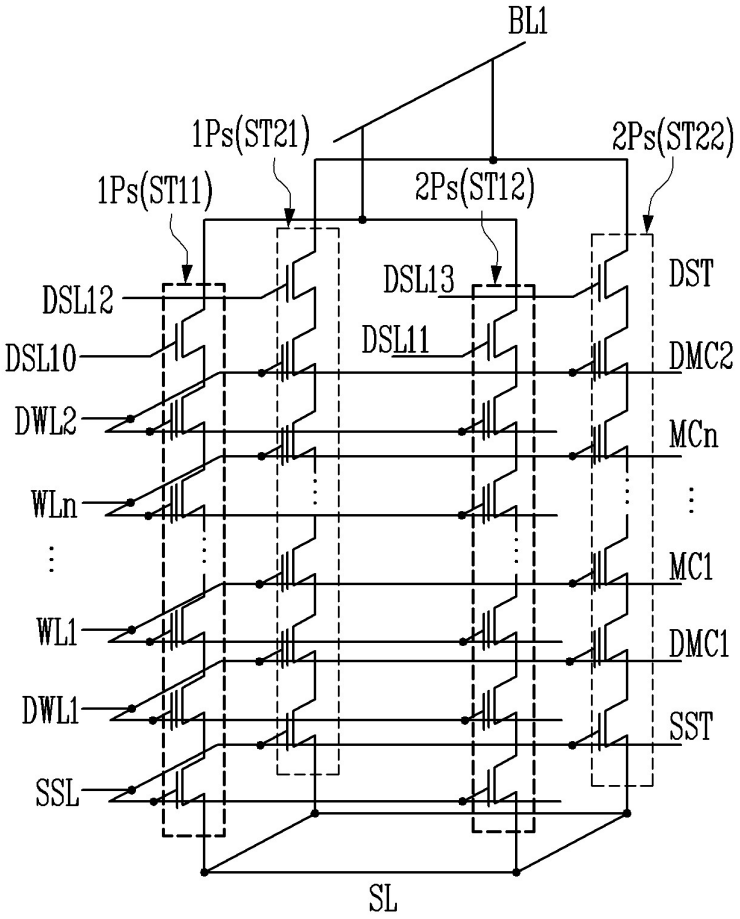

BL1
1Ps(ST21)
2Ps(ST22)
1Ps(ST11)
2Ps(ST12)
DSL12
DSL13
DST
DSL10
DSL11
DMC2
DWL2
MCn
WLn
MC1
WL1
DMC1
DWL1
SST
SSL
SL

FIG. 18

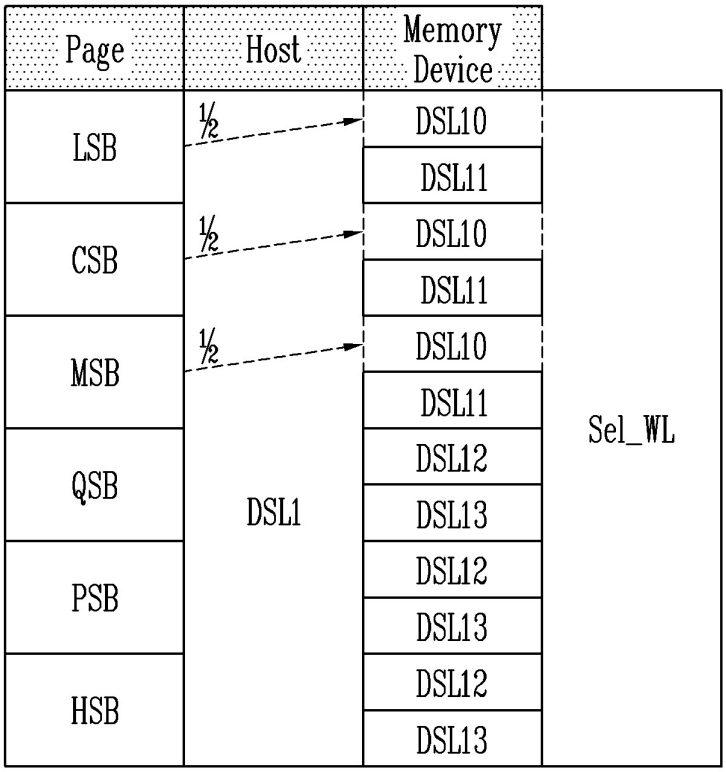

Page
Host
Memory Device
LSB
CSB
MSB
QSB
PSB
HSB
½
DSL1
DSL10
DSL11
DSL12
DSL13
Sel_WL

FIG. 19

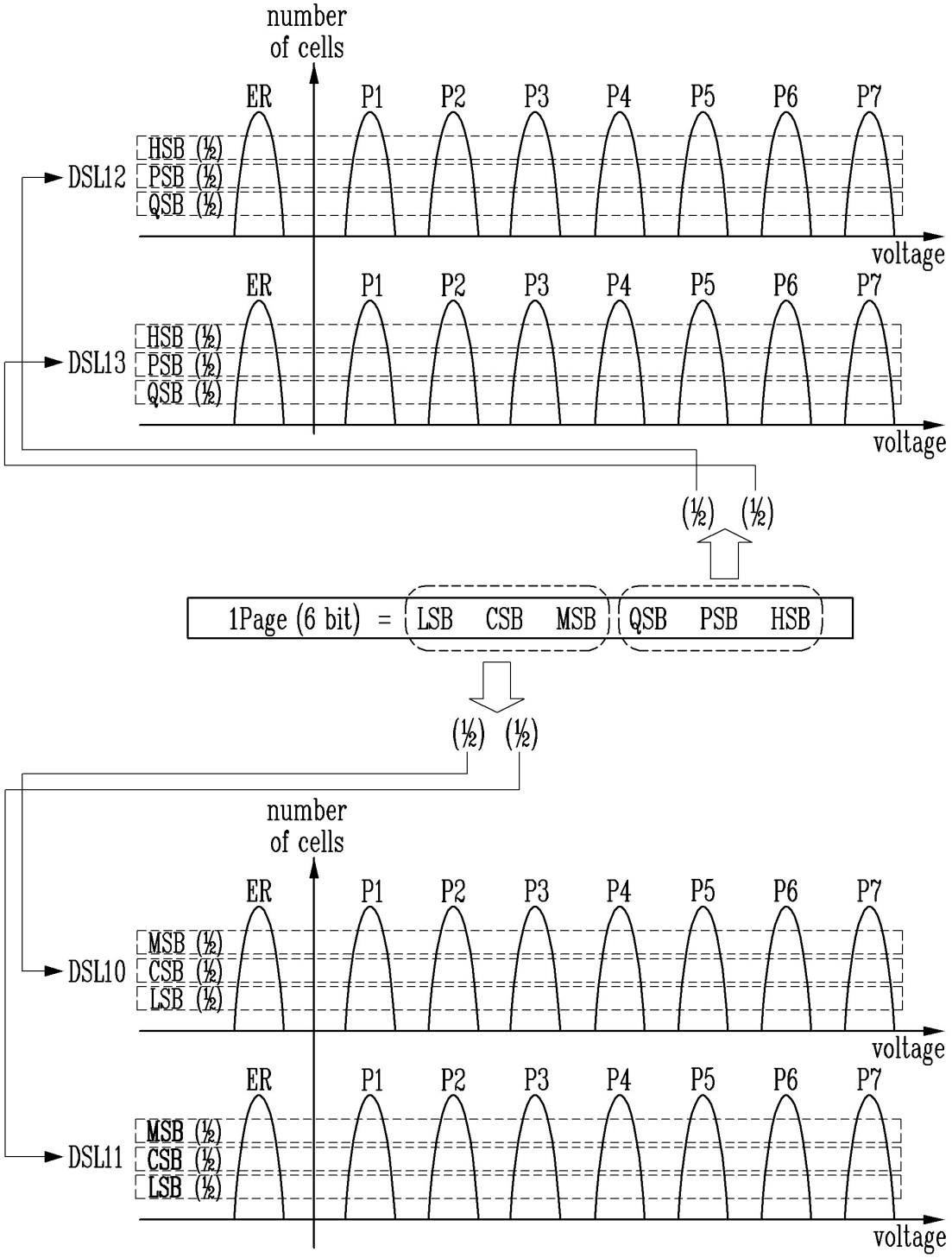

number of cells
ER
P1
P2
P3
P4
P5
P6
P7
HSB (½)
PSB (½)
QSB (½)
DSL12
voltage
DSL13
(½) (½)
1Page (6 bit) = LSB CSB MSB QSB PSB HSB
MSB (½)
CSB (½)
LSB (½)
DSL10
DSL11

FIG. 20

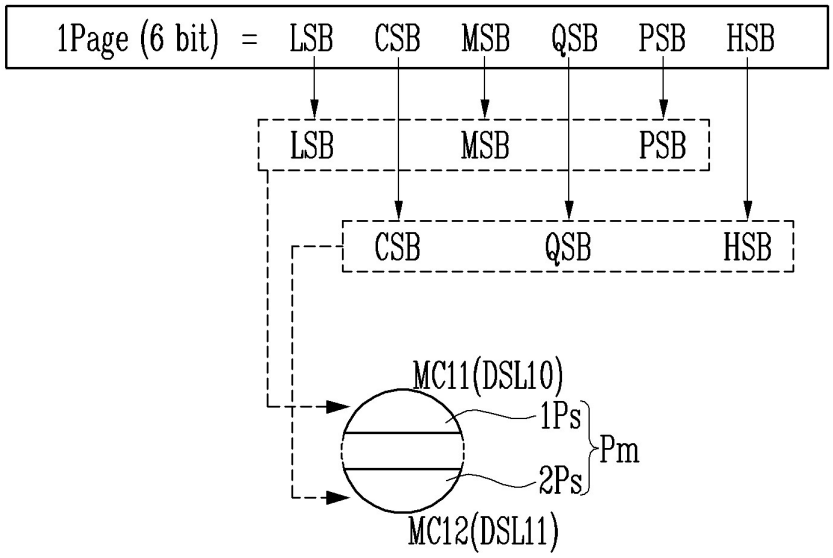

1Page (6 bit) = LSB CSB MSB QSB PSB HSB
LSB MSB PSB
CSB QSB HSB
MC11(DSL10)
1Ps
2Ps
Pm
MC12(DSL11)

FIG. 21

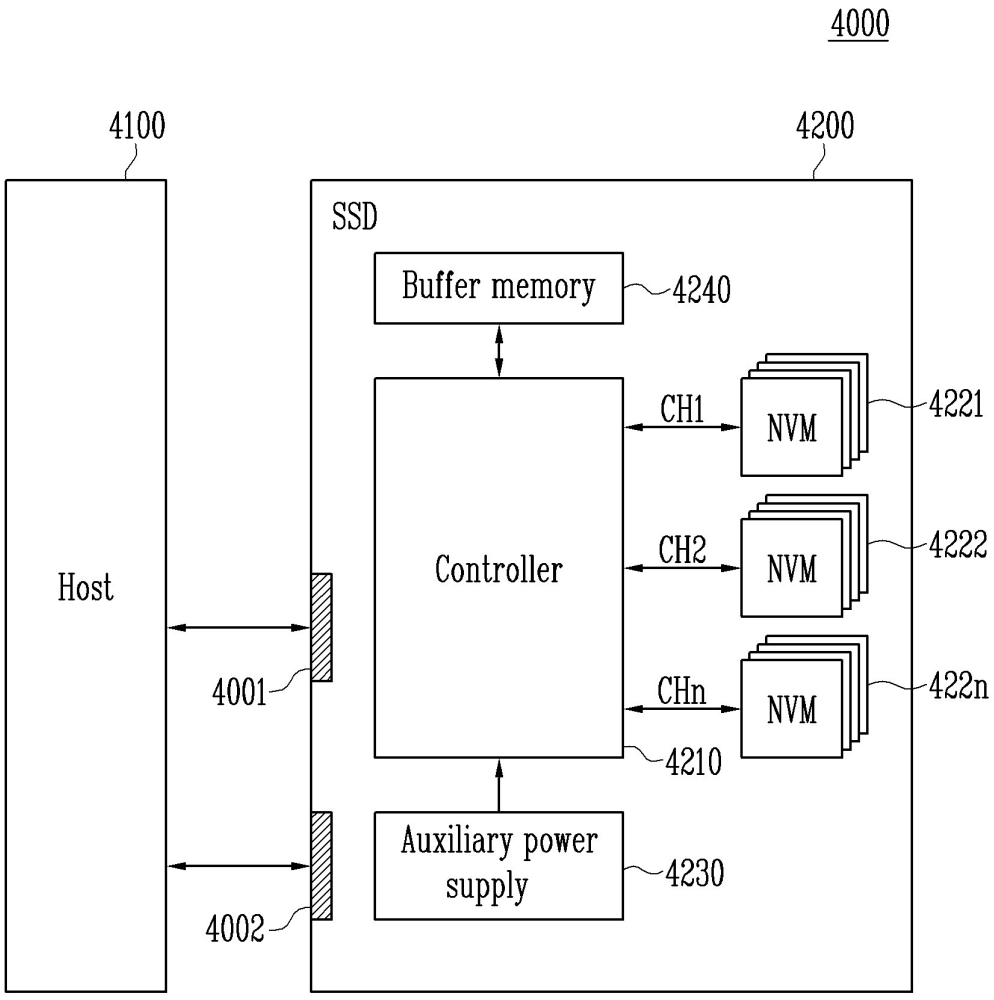
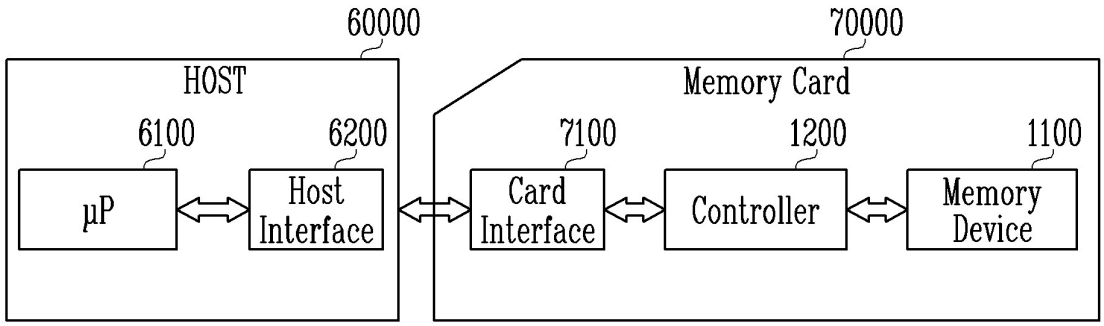

4000
4100
4200
SSD
Buffer memory
4240
Controller
CH1
NVM
4221
CH2
NVM
4222
CHn
NVM
422n
4210
Host
4001
4002
Auxiliary power supply
4230

FIG. 22


60000
70000
HOST
Memory Card
6100
6200
7100
1200
1100
µP
Host Interface
Card Interface
Controller
Memory Device