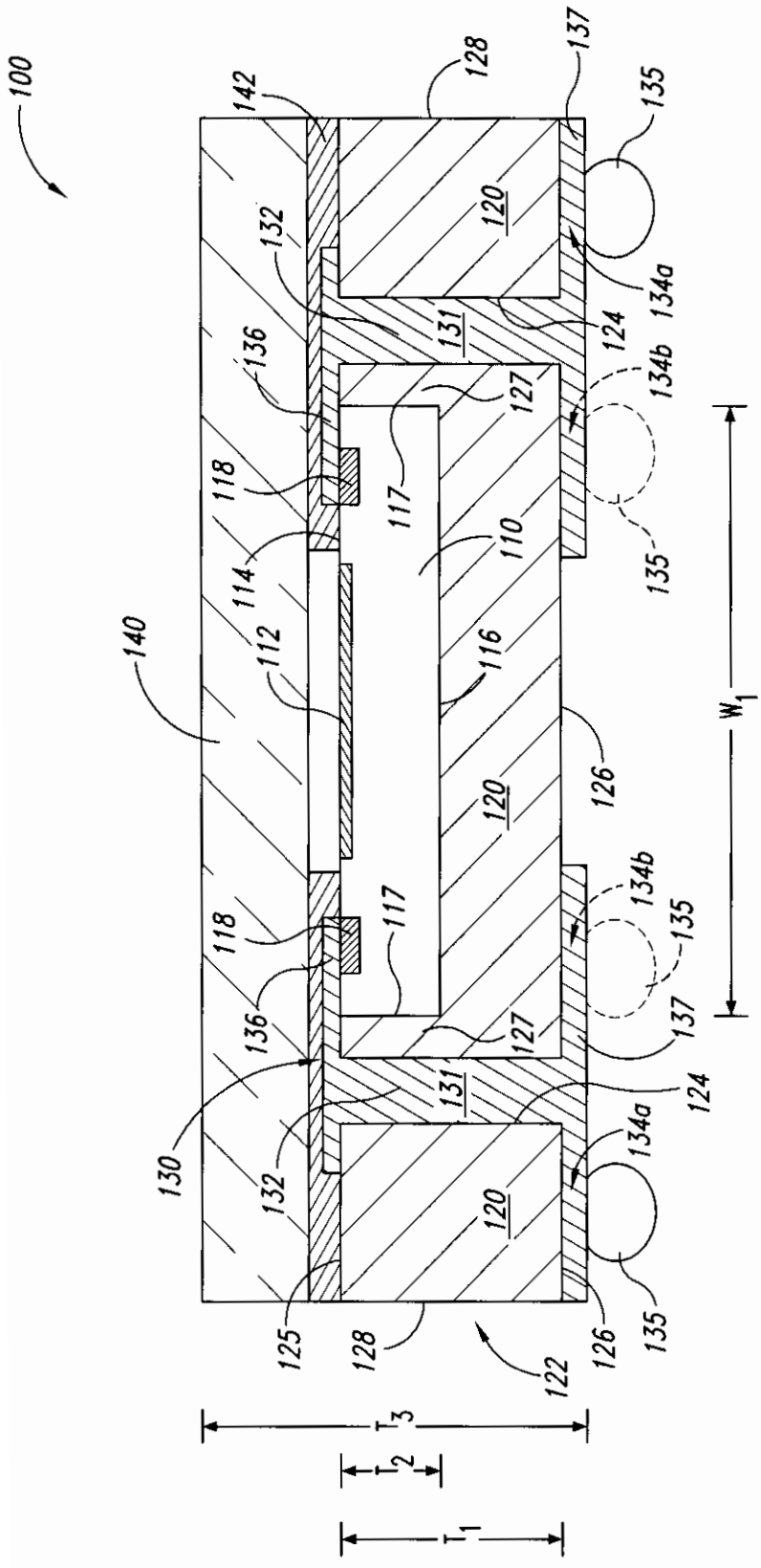

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126
135
T3
T2
T1
W1

Fig. 1

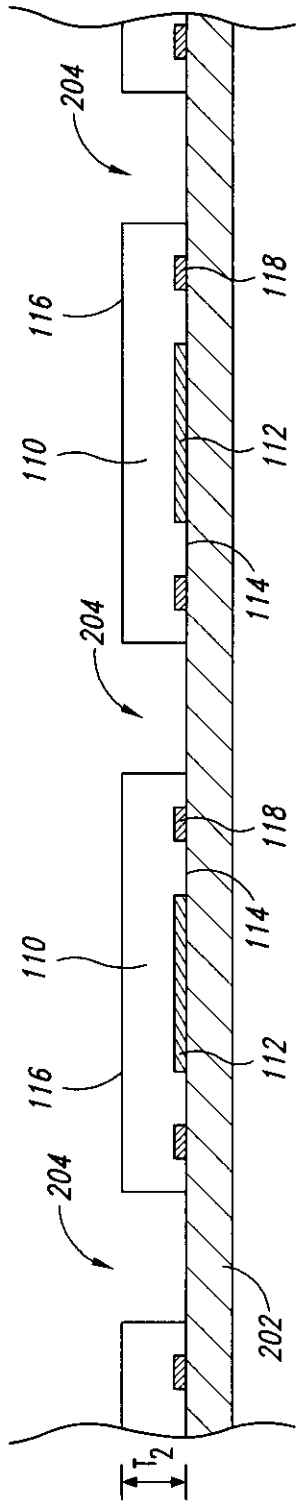

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Fig. 2A

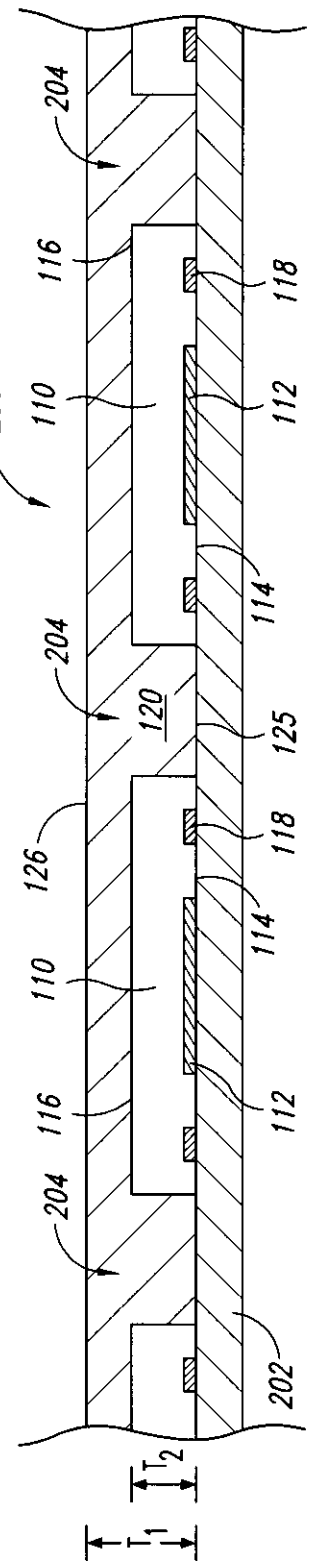

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118
114
110
116
112
204
202
T_2
T_1

Fig. 2B

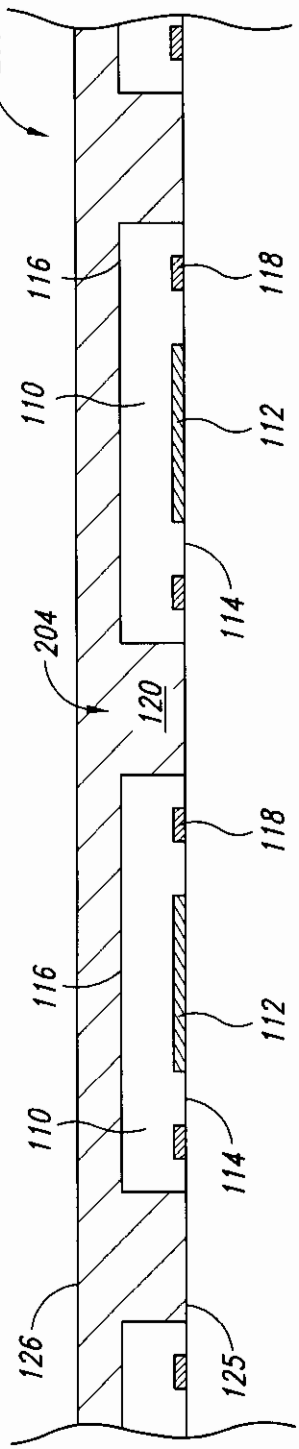


Fig. 2C

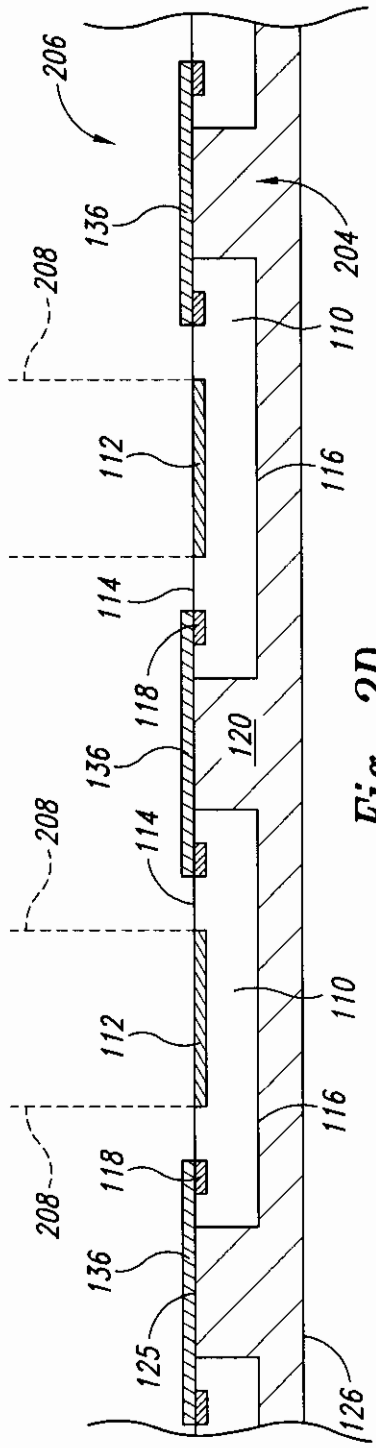


Fig. 2D

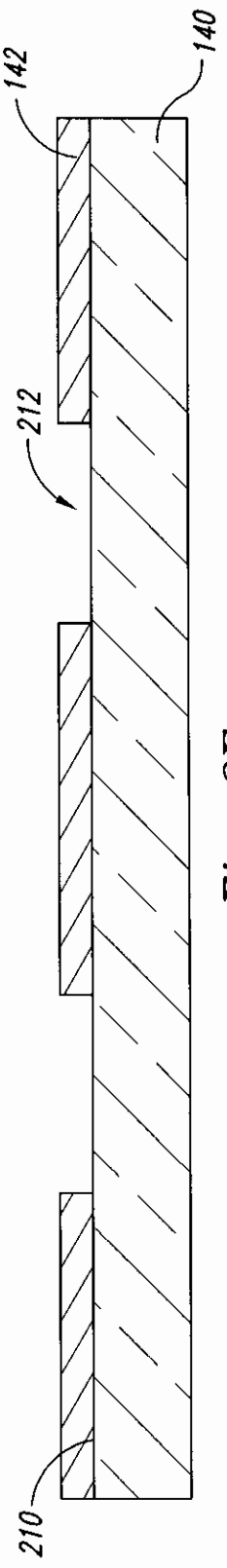


Fig. 2E

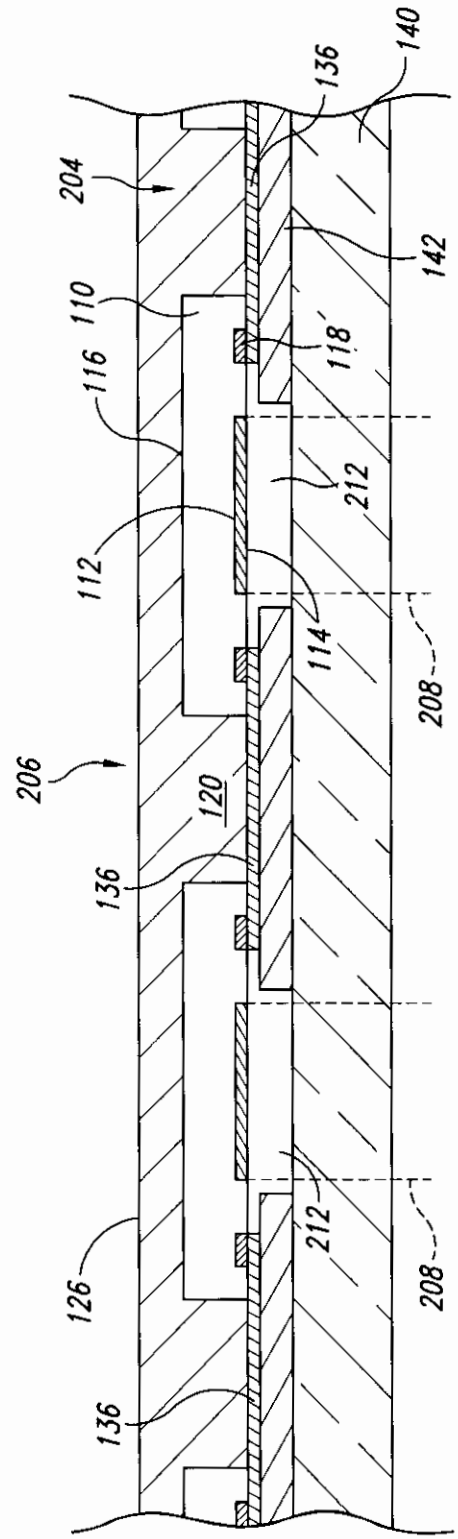

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Fig. 2F

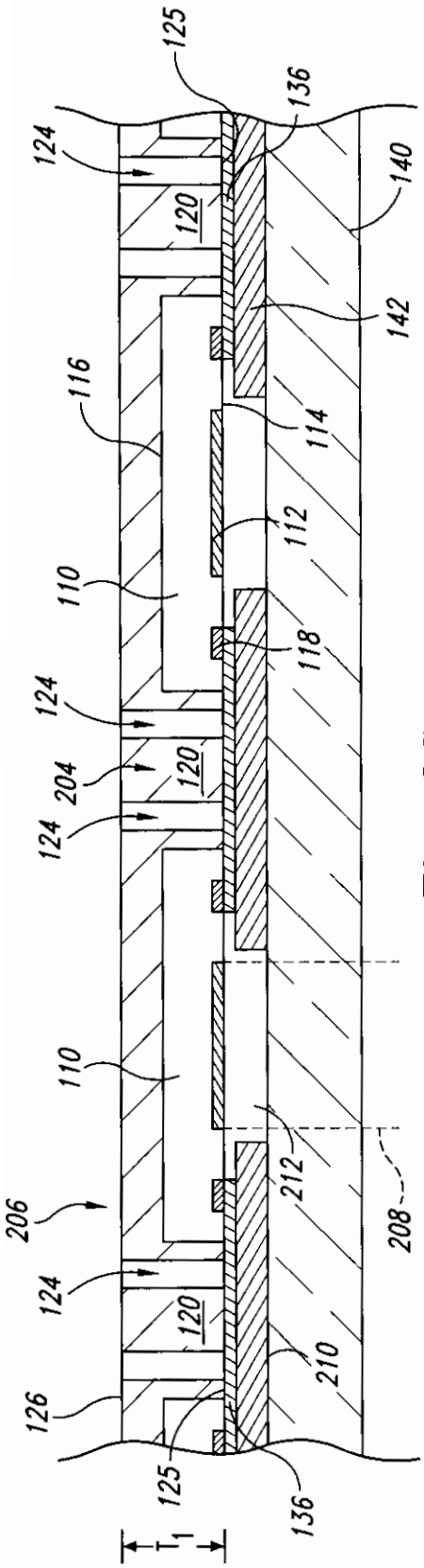

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208
210
T_1

Fig. 2G

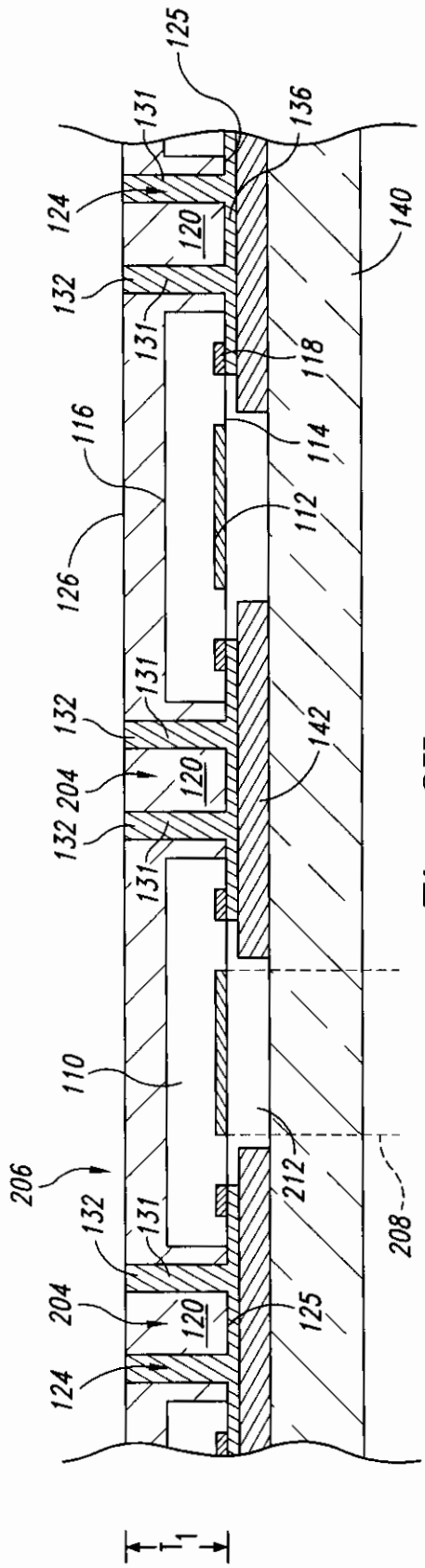

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204
120
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124
T_1

Fig. 2H

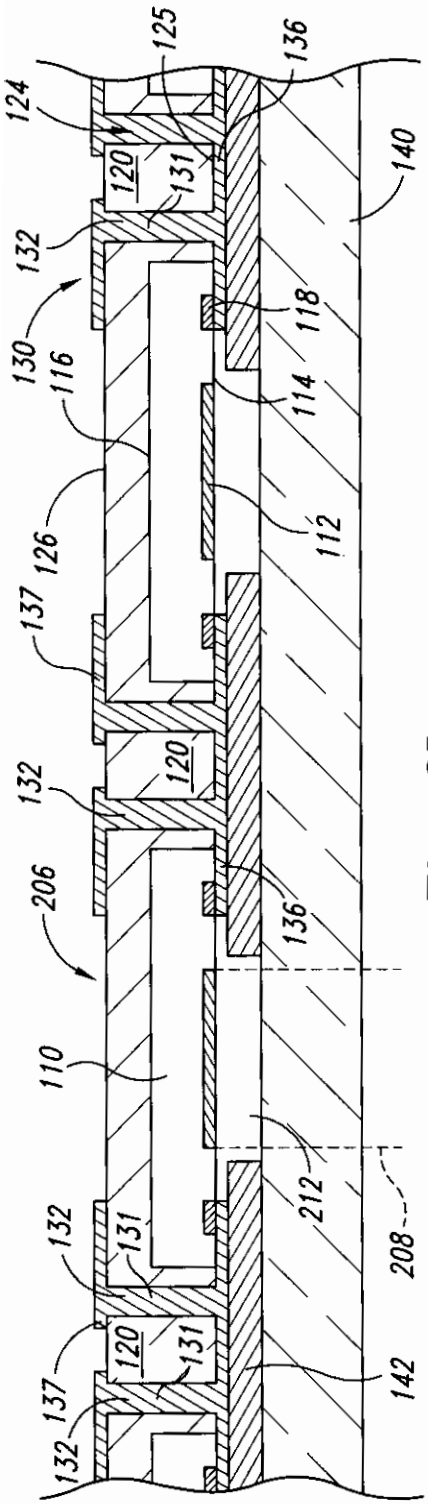

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142

Fig. 2I

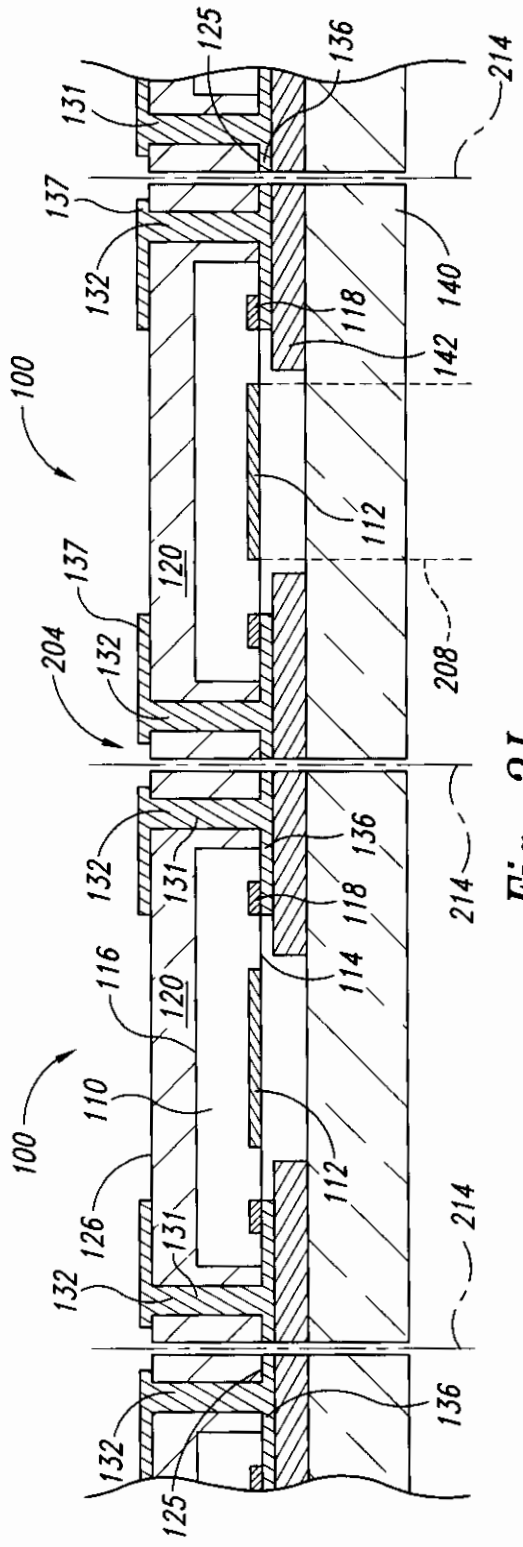

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Fig. 2J

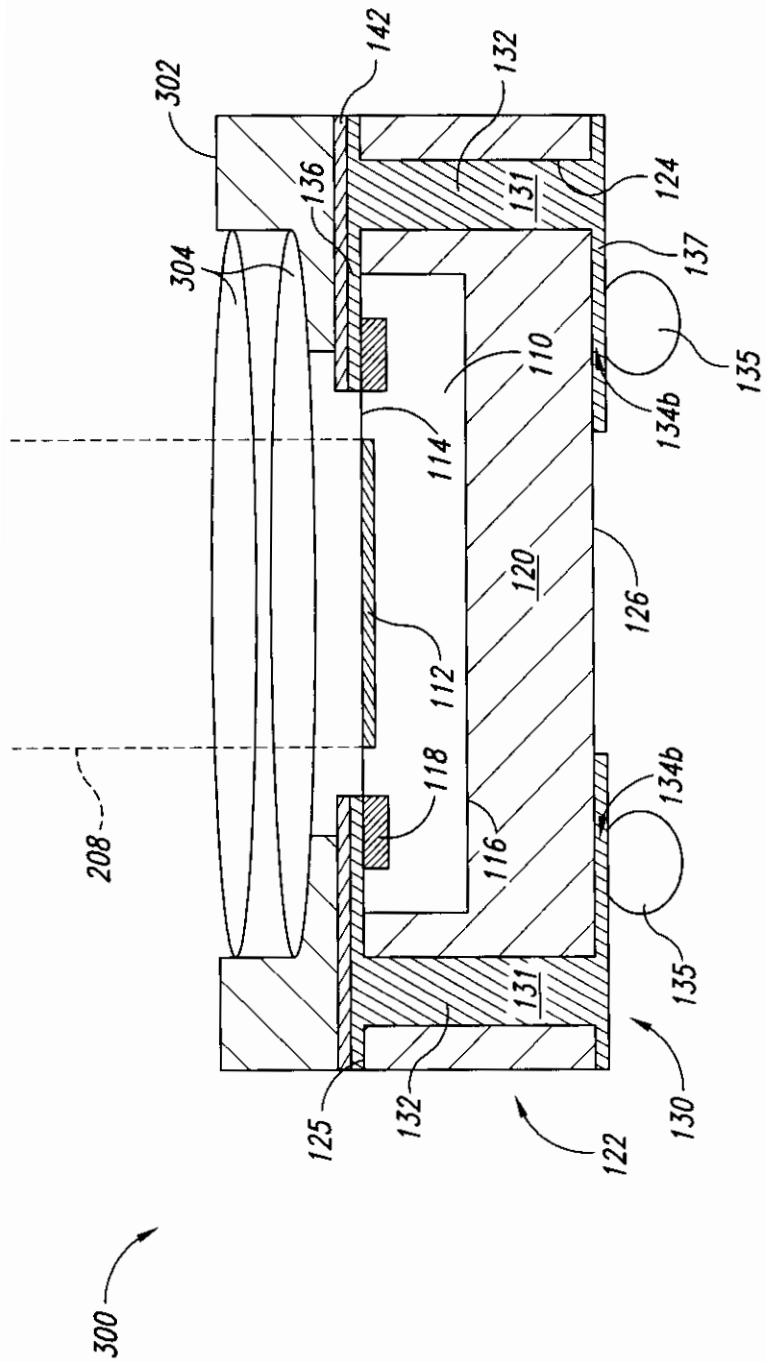

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Fig. 3

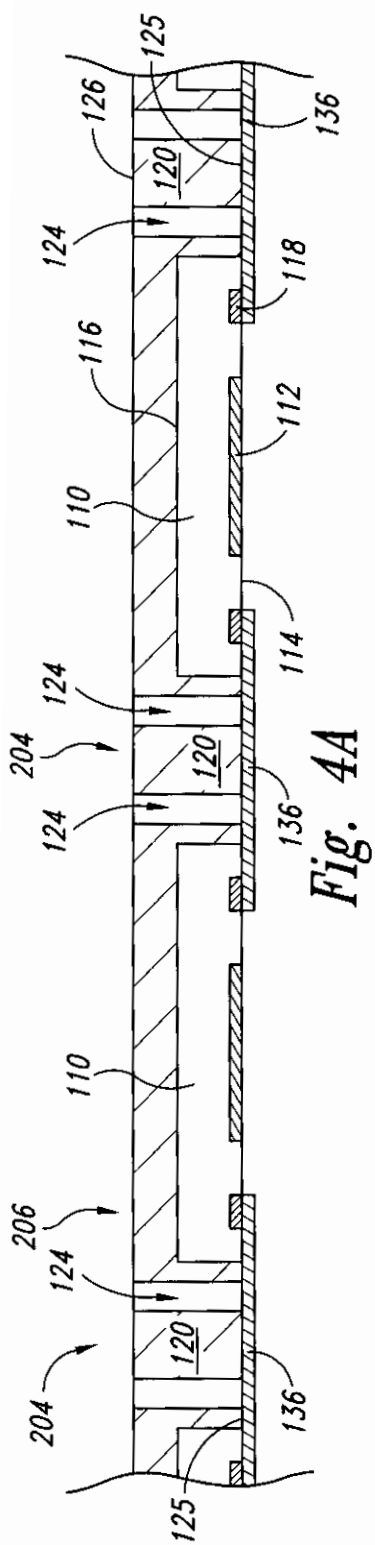


Fig. 4A

Fig. 4B

Fig. 4C

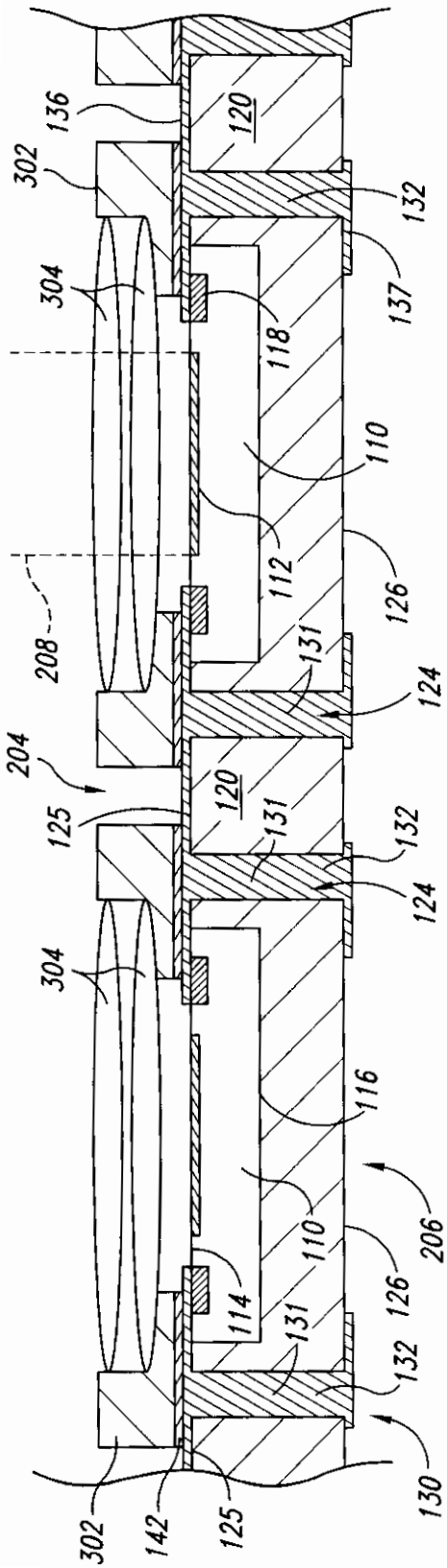

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Fig. 4D

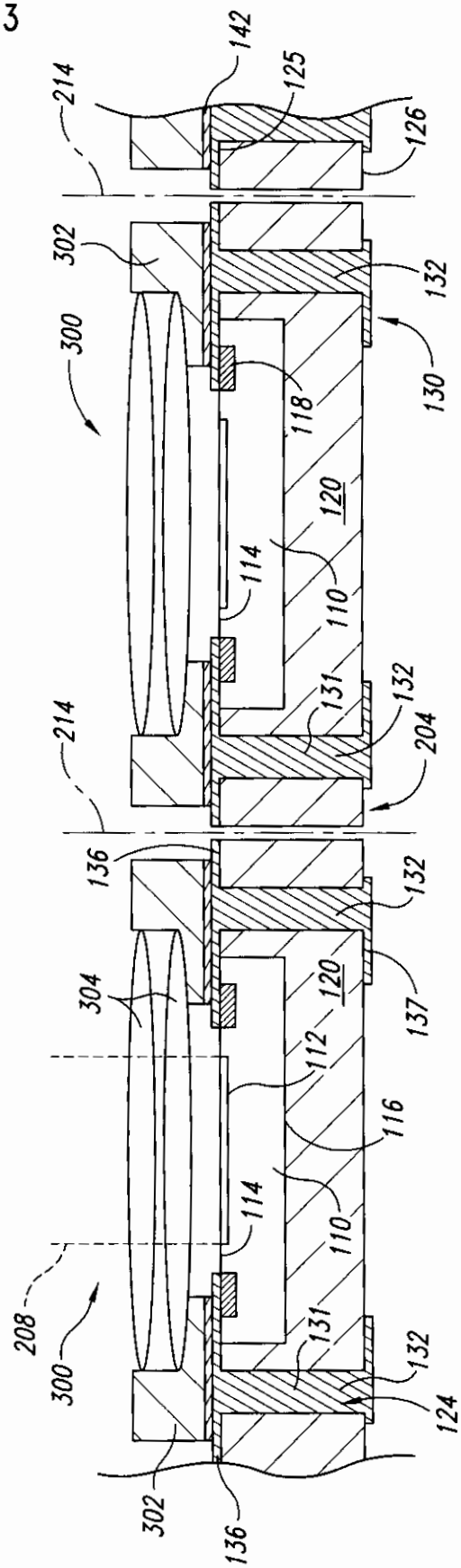

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Fig. 4E

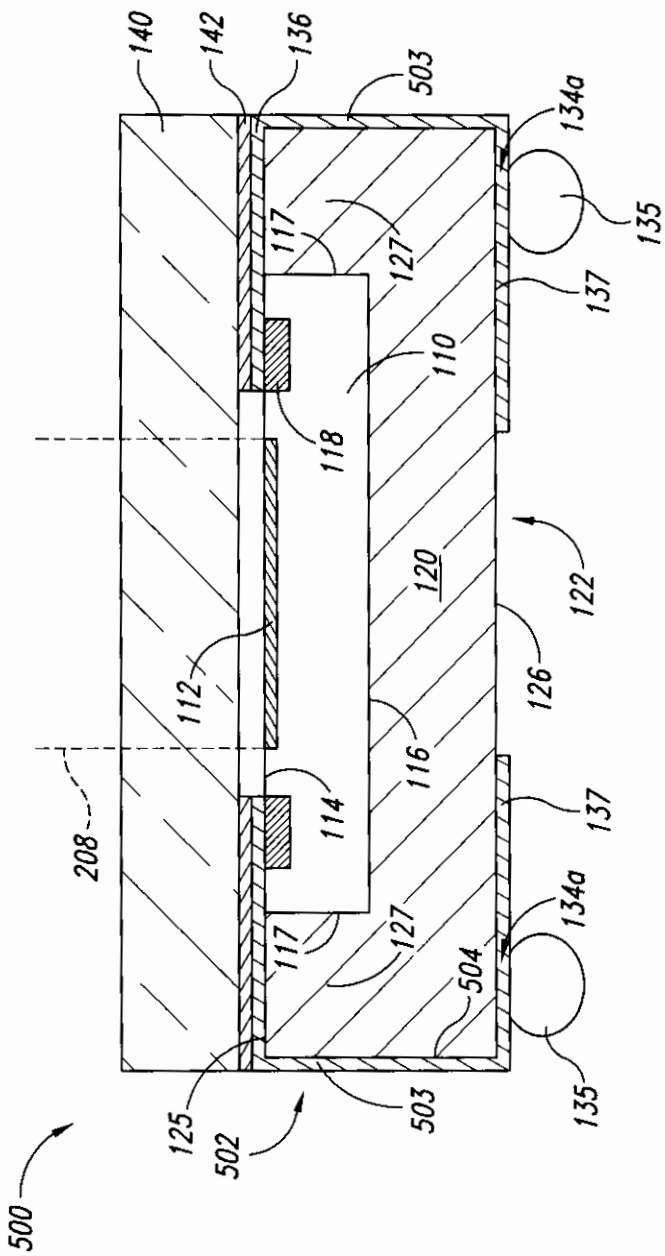

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134a
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Fig. 5

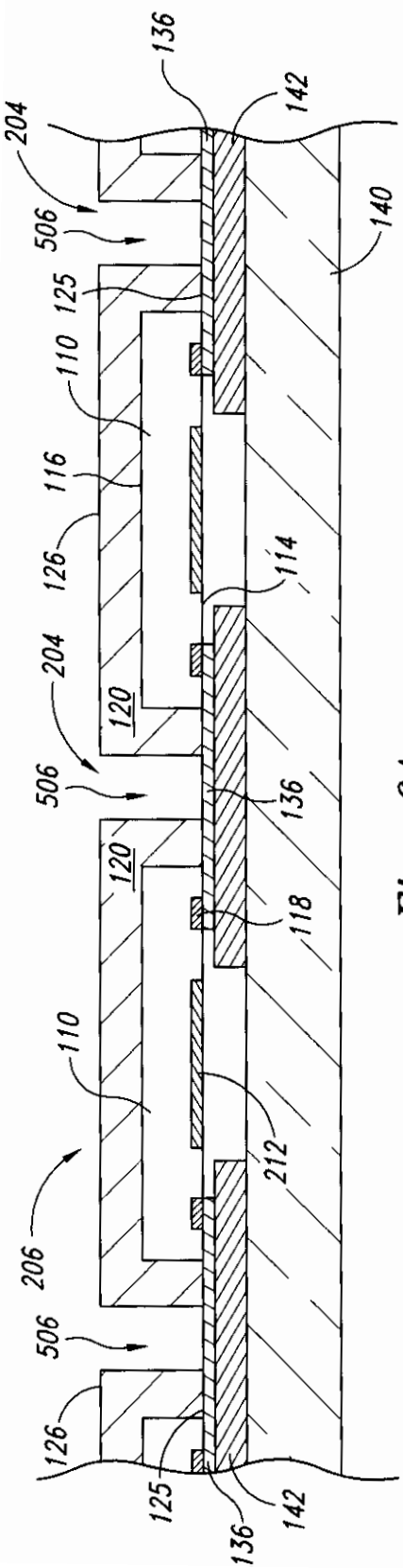

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136

Fig. 6A

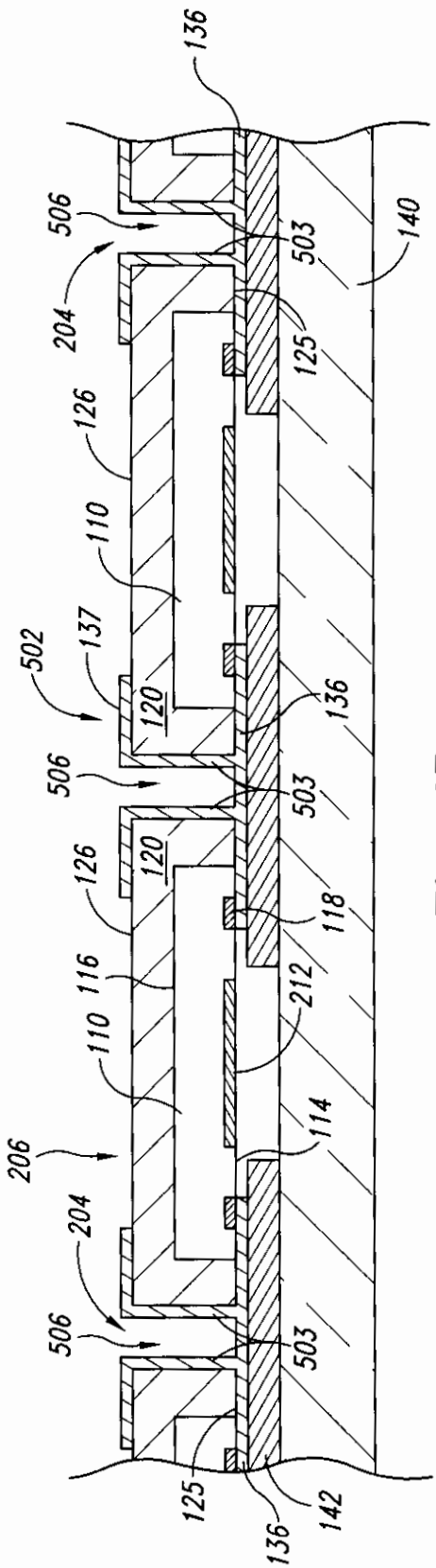

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142

Fig. 6B

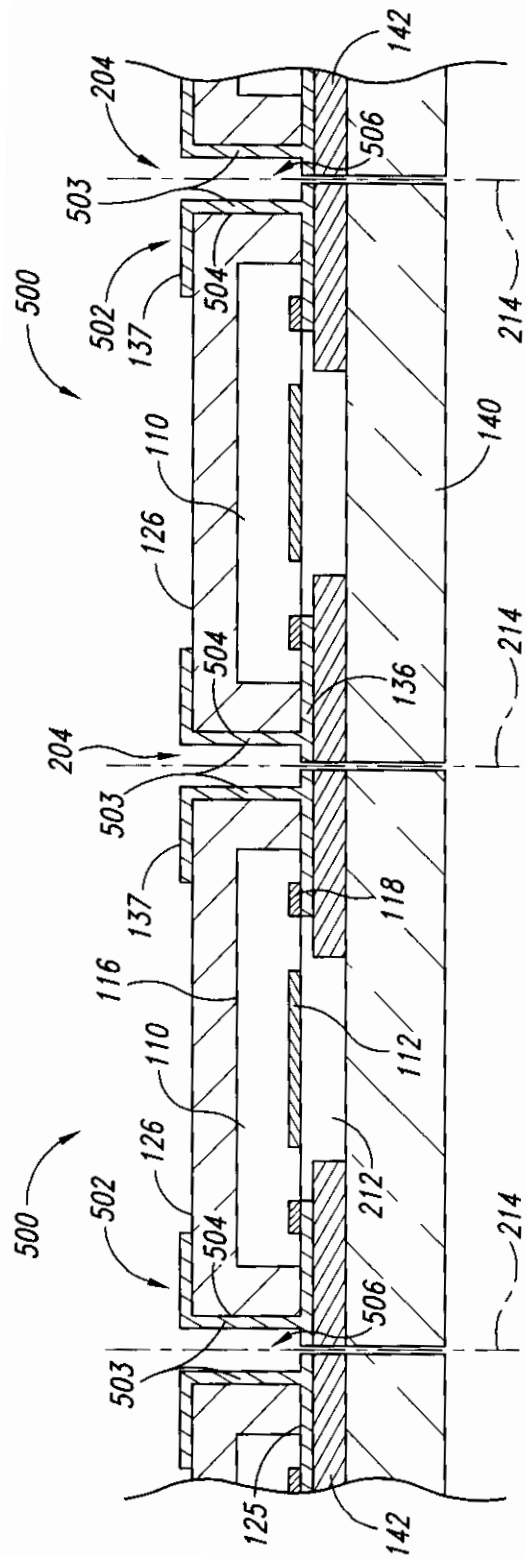

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Fig. 6C

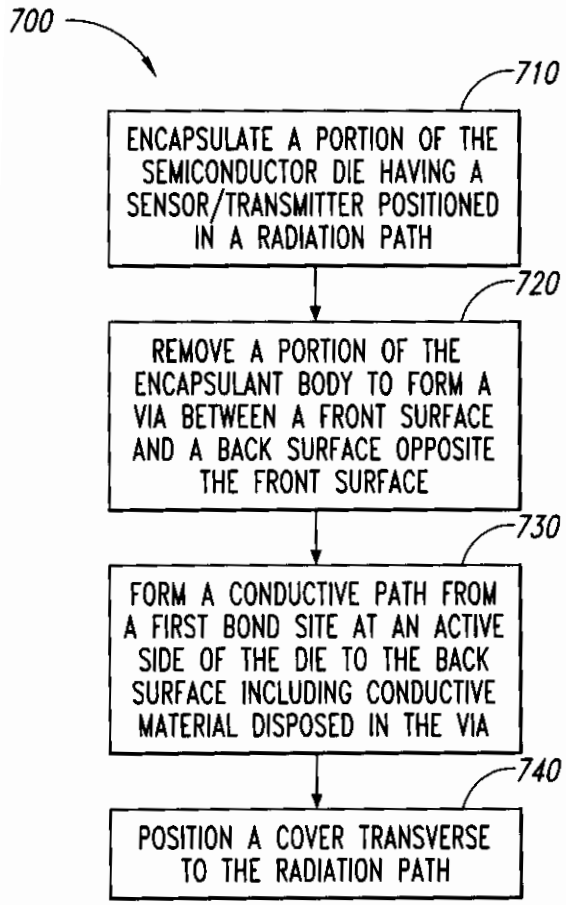

700
710
ENCAPSULATE A PORTION OF THE SEMICONDUCTOR DIE HAVING A SENSOR/TRANSMITTER POSITIONED IN A RADIATION PATH
720
REMOVE A PORTION OF THE ENCAPSULANT BODY TO FORM A VIA BETWEEN A FRONT SURFACE AND A BACK SURFACE OPPOSITE THE FRONT SURFACE
730
FORM A CONDUCTIVE PATH FROM A FIRST BOND SITE AT AN ACTIVE SIDE OF THE DIE TO THE BACK SURFACE INCLUDING CONDUCTIVE MATERIAL DISPOSED IN THE VIA
740
POSITION A COVER TRANSVERSE TO THE RADIATION PATH

Fig. 7

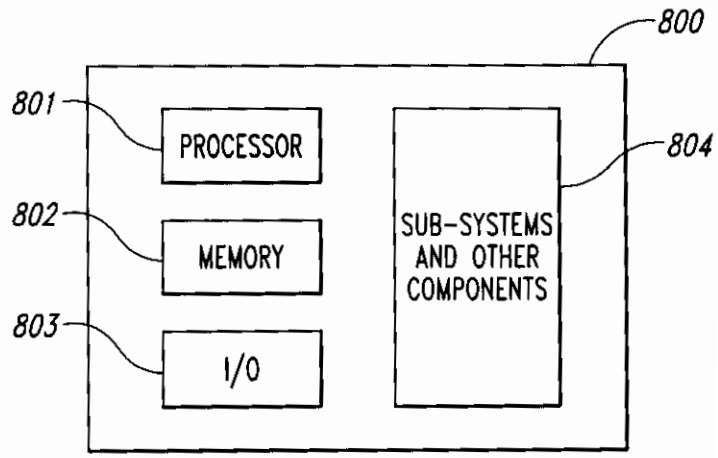

800
801
PROCESSOR
802
MEMORY
803
I/O
804
SUB-SYSTEMS AND OTHER COMPONENTS

Fig. 8