

Silicon would allow fabricating costs to be drastically decreased and substrates of large size to be accessed, but structures of III-N-alloy-on-silicon type are penalized by RF losses and by a poor dissipation of heat.

Composite structures, such as SopSiC or SiCopSiC structures, have also been investigated [1] but have not proved to be entirely satisfactory. These structures comprise a layer of single-crystal silicon or a layer of single-crystal SiC (intended to form a seed layer for the epitaxial growth of the gallium nitride) on a polycrystalline SiC substrate, respectively. Although polycrystalline SiC is a material that is inexpensive, that is available in the form of substrates of large size and that dissipates heat well, these composite structures are penalized by the presence of a layer of silicon oxide at the interface between the layer of single-crystal silicon or SiC and the polycrystalline SiC substrate, which forms a thermal barrier hindering the dissipation of heat from the layer of III-N alloy to the polycrystalline SiC substrate.

Brief description of the invention

One aim of the invention is therefore to remedy the aforementioned drawbacks and in particular limitations related to the size and cost of semi-insulating SiC substrates.

The aim of the invention is therefore to provide a process for fabricating a substrate for the epitaxial growth of a III-N alloy based on gallium, in particular with a view to forming HEMTs or other high-frequency, high-power electronic devices in which RF losses ~~are~~ may be minimized and the dissipation of heat ~~is~~ may be maximized.

~~To this end,~~ An aspect of the invention provides a process for fabricating a substrate for epitaxial growth of a layer of gallium nitride (GaN), of aluminium gallium nitride (AlGaN) or of indium gallium nitride (InGaN), comprising the following successive steps:

- providing a base substrate comprising at least one layer of single-crystal silicon carbide,
- performing epitaxial growth of a layer of semi-insulating SiC on the layer of single-crystal SiC to form a donor substrate,
- implanting ionic species into the layer of semi-insulating SiC so as to form a weakened region that defines a thin layer of single-crystal semi-insulating SiC to be transferred,
- bonding the layer of semi-insulating SiC to a receiver substrate having a high electrical resistivity,
- detaching the donor substrate along the weakened region so as to transfer the thin layer of single-crystal semi-insulating SiC to the receiver substrate.

By “high-frequency”, what is meant in the present text is a frequency higher than 3 kHz.

By “high-power” what is meant in the present text is a power density higher than 0.5 W/mm injected through the gate of the transistor.

- said recycling comprises polishing a residual segment of the layer of semi-insulating SiC and performing epitaxial regrowth in order to increase the thickness of said layer of semi-insulating SiC to form the new donor substrate;
- said recycling comprises removing a residual segment of the layer of semi-insulating SiC to uncover the carbon face of the layer of single-crystal SiC and performing epitaxial growth of a new layer of semi-insulating SiC on the carbon face of the layer of single-crystal SiC to form the new donor substrate;
- the layer of single-crystal silicon carbide of the base substrate has a free carbon face, the epitaxial growth of the layer of semi-insulating SiC is performed on said carbon face of the layer of single-crystal SiC, the ionic species are implanted through the carbon face of the layer of semi-insulating SiC, the carbon face of the layer of semi-insulating SiC is bonded to the receiver substrate, at the end of the detachment, the silicon face of the transferred layer of single-crystal semi-insulating SiC is uncovered;
- the process comprises fabricating the base substrate via the following successive steps: providing a start substrate of single-crystal SiC having a silicon face; implanting ionic species through the silicon face of the start substrate so as to form a weakened region that defines a thin layer of single-crystal SiC to be transferred; bonding the silicon face of the start substrate to an intermediate carrier; detaching the start substrate along the weakened region so as to transfer the thin layer of single-crystal SiC to the intermediate carrier and to uncover the carbon face of said transferred layer of single-crystal SiC, the intermediate carrier and the transferred layer of single-crystal SiC together forming the base substrate;
- the intermediate carrier is an SiC substrate having a crystal quality lower than that of the start substrate;
- the start substrate is bonded directly to the intermediate carrier after activation of each surface to be bonded by bombardment of neutral species;
- the start substrate is bonded to the intermediate carrier by way of a refractory bonding layer;
- the process comprises a step of recycling the segment of start substrate detached from the transferred layer, with a view to forming a new start substrate.

Another subject aspect of the invention ~~relates to~~provides a process for fabricating a layer of ~~a III-N alloy based on gallium on a substrate obtained using the process that has just been described~~ gallium nitride, of aluminium gallium nitride (AlGaN) or of indium gallium nitride (InGaN).

Said process comprises:

- providing a substrate fabricated using the process described above,
- performing epitaxial growth of the layer of gallium nitride, of aluminium gallium nitride (AlGaN) or of indium gallium nitride (InGaN) on the layer of semi-insulating SiC of said substrate.

The layer of gallium nitride, of aluminium gallium nitride (AlGaN) or of indium gallium nitride (InGaN) has a thickness typically comprised between 1 and 2 μm .

Another subject aspect of the invention ~~relates to~~provides a process for fabricating a high-electron-mobility transistor (HEMT) ~~in such a layer of III-N alloy based on gallium~~.

Said process comprises:

- fabricating by epitaxy a layer of gallium nitride, of aluminium gallium nitride (AlGaN) or of indium gallium nitride (InGaN) using the aforementioned process,
- forming a heterojunction by epitaxy of a layer of a III-N material different from gallium nitride on the layer of gallium nitride, of aluminium gallium nitride (AlGaN) or of indium gallium nitride (InGaN),
- forming a channel of the transistor level with said heterojunction,
- forming a source, a drain and a gate of the transistor on the channel.

Brief description of the drawings

Further features and advantages of the invention will become apparent from the following detailed description, with reference to the appended drawings, in which:

[Fig 1A] is a schematic cross-sectional view of a single-crystal SiC base substrate;

[Fig 1B] is a schematic cross-sectional view of a donor substrate formed by epitaxial growth of a layer of single-crystal semi-insulating SiC on the C-face of the base substrate of Figure 1A;

[Fig 1C] is a schematic cross-sectional view of the donor substrate after trimming intended to remove an SiC outgrowth formed on the edges of said substrate during the epitaxy;

[Fig 1D] is a schematic cross-sectional view of the donor substrate of Figure 1C during the formation of a weakened region via implantation of ionic species in the layer of semi-insulating SiC to define a thin layer to be transferred;

[Fig 1E] is a schematic cross-sectional view of assembly of a receiver substrate and of the donor substrate of Figure 1D;

[Fig 1F] is a schematic cross-sectional view of the donor substrate being detached along the weakened region in order to transfer the thin layer of single-crystal semi-insulating SiC to the receiver substrate;

[Fig 1G] is a schematic cross-sectional view of the thin layer of single-crystal semi-insulating SiC transferred to the receiver substrate after its free surface (silicon face) has been polished;

[Fig 1H] is a schematic cross-sectional view of a layer of GaN being formed by epitaxy on the silicon face of the layer of single-crystal semi-insulating SiC of Figure 1G;

[Fig 1I] is a schematic cross-sectional view of the formation by epitaxy of a heterojunction on the layer of GaN of Figure 1H;