12 SEP 2005

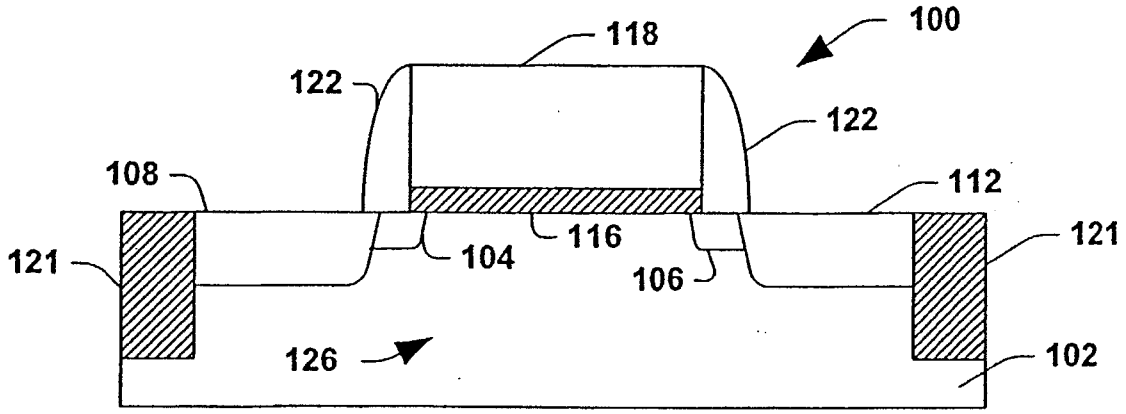


FIG. 1
(PRIOR ART)

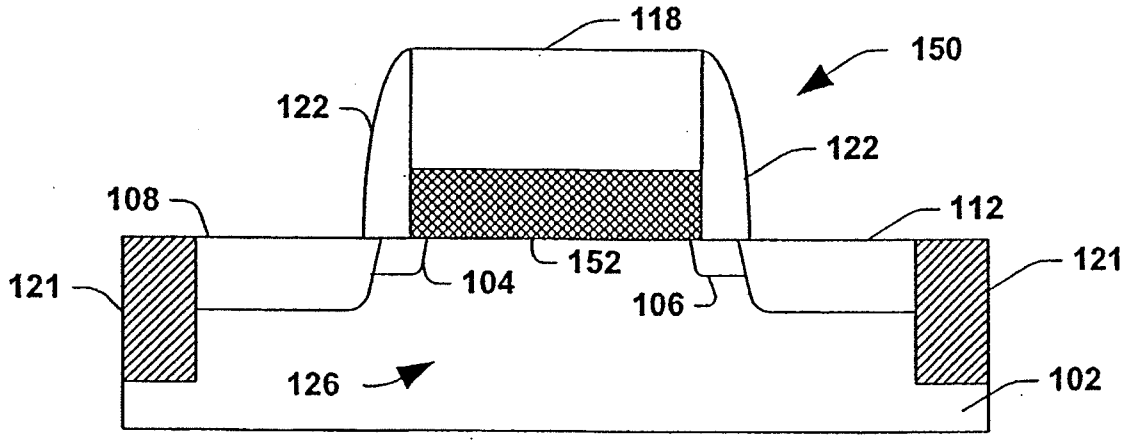


FIG. 2
(PRIOR ART)

12 SEP 2005

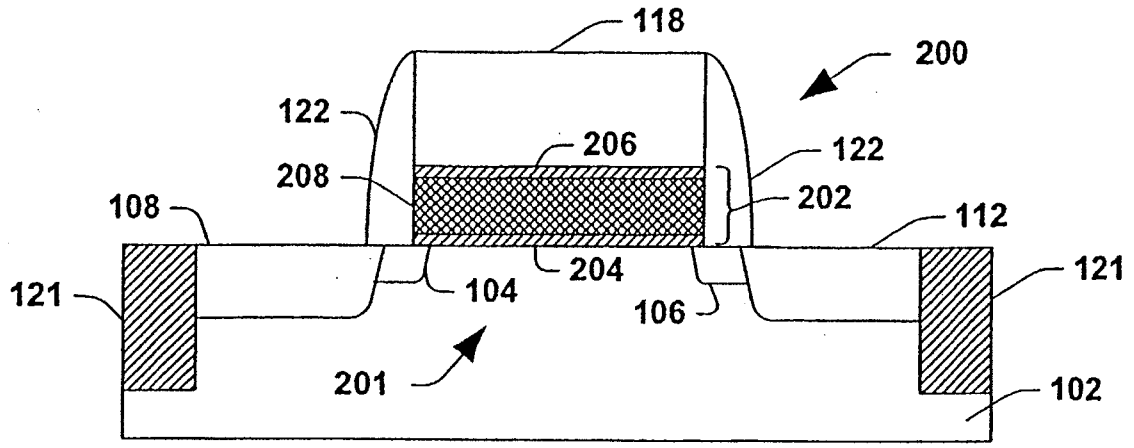


FIG. 3

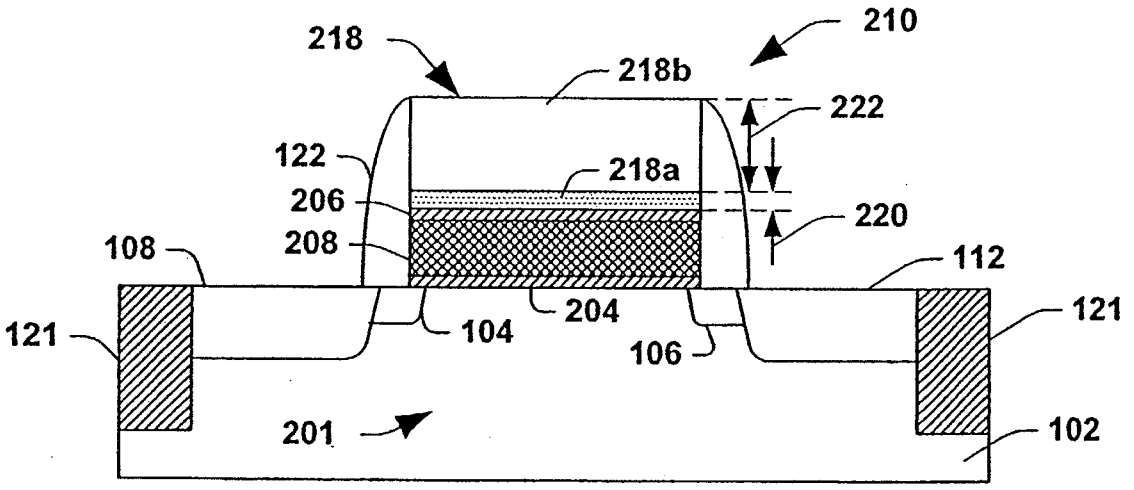


FIG. 4

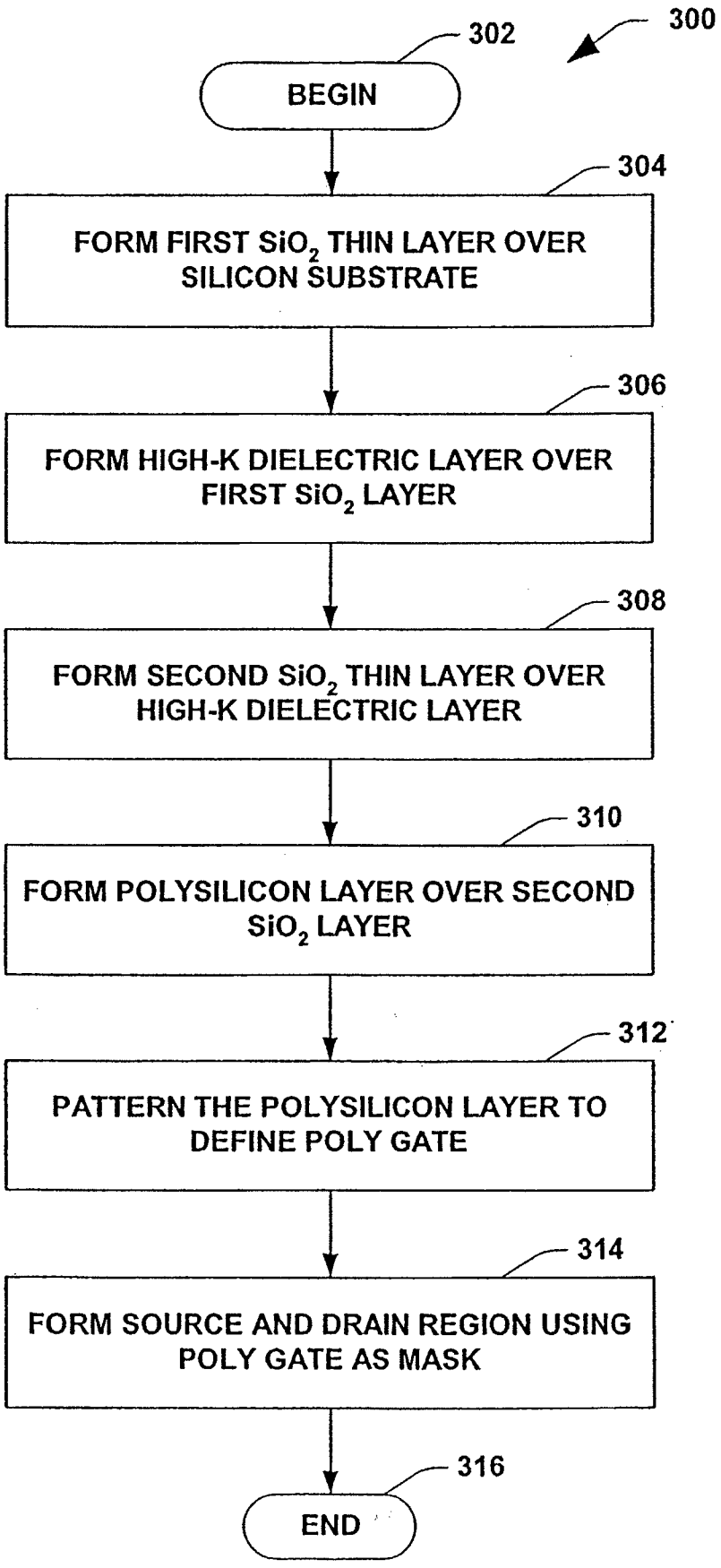

300
302
BEGIN
304
FORM FIRST SiO_2 THIN LAYER OVER SILICON SUBSTRATE
306
FORM HIGH-K DIELECTRIC LAYER OVER FIRST SiO_2 LAYER
308
FORM SECOND SiO_2 THIN LAYER OVER HIGH-K DIELECTRIC LAYER
310
FORM POLYSILICON LAYER OVER SECOND SiO_2 LAYER
312
PATTERN THE POLYSILICON LAYER TO DEFINE POLY GATE
314
FORM SOURCE AND DRAIN REGION USING POLY GATE AS MASK
316
END

FIG. 5

12 SEP 2005

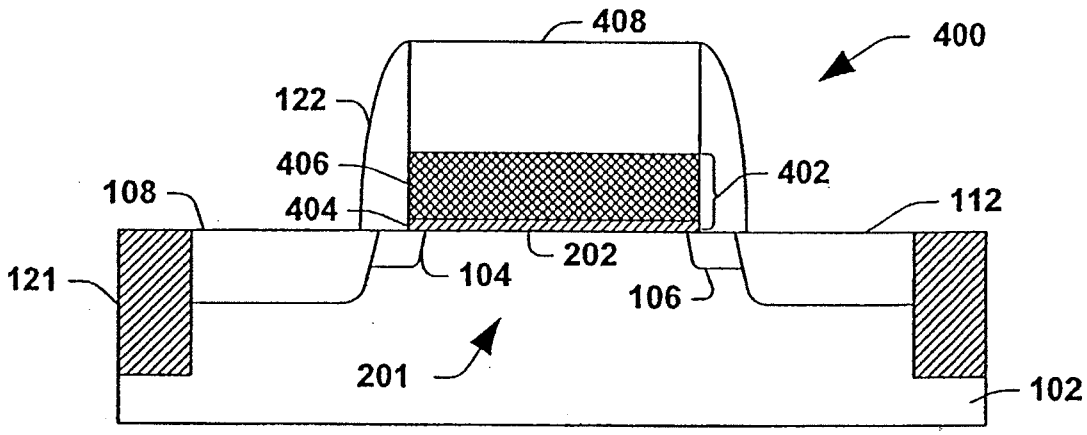


FIG. 6

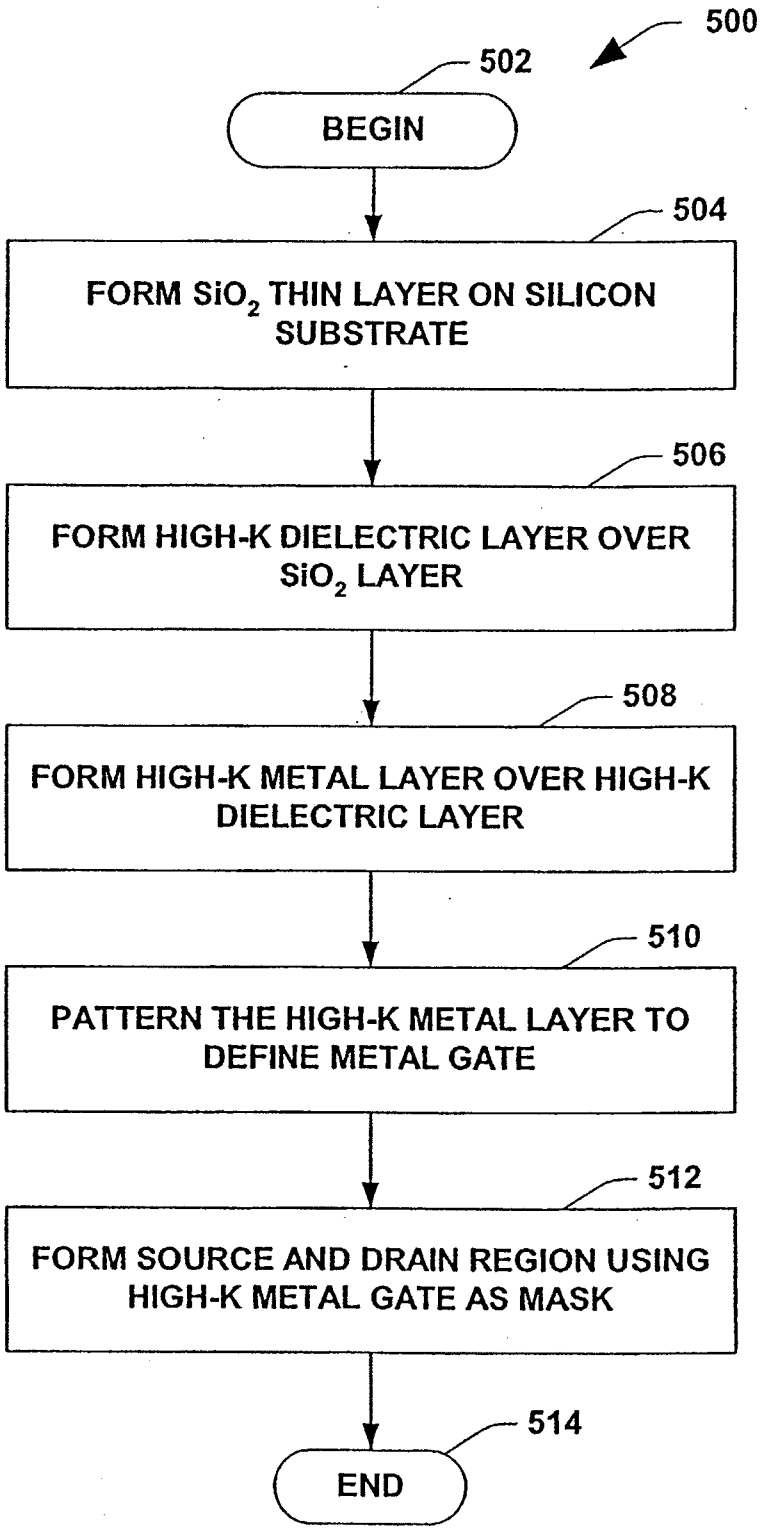

500
502
BEGIN
504
FORM SiO_2 THIN LAYER ON SILICON SUBSTRATE
506
FORM HIGH-K DIELECTRIC LAYER OVER SiO_2 LAYER
508
FORM HIGH-K METAL LAYER OVER HIGH-K DIELECTRIC LAYER
510
PATTERN THE HIGH-K METAL LAYER TO DEFINE METAL GATE
512
FORM SOURCE AND DRAIN REGION USING HIGH-K METAL GATE AS MASK
514
END

FIG. 7