

# SEMICONDUCTOR-ON-INSULATOR CHIP WITH <100>-ORIENTED TRANSISTORS

## CROSS REFERENCE

[0001] This application is related to, and claims priority of, U.S. Provisional Patent Application Ser. No. 60 516,473, filed on October 31, 2003.

## BACKGROUND

[0002] The present disclosure relates to semiconductor integrated circuits, and more specifically to a silicon-on-insulator chip comprising <100>-oriented transistors.

[0003] Application of longitudinal stress - stress applied in the direction of current flow - modifies the mobilities of electrons and holes in NMOS and PMOS transistors, respectively. By using a conventional bulk silicon substrate with a (001) surface orientation and forming transistors with source-to-drain orientation in <110> directions, application of longitudinal stress leads to different reactions for electrons and holes. When a stress is applied in the longitudinal direction, either the electron mobility is increased and the hole mobility is decreased, or the electron mobility is decreased and the hole mobility is increased.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

[0004] Fig. 1 is an exploded view illustrating a silicon layer formed on an insulator layer overlying a substrate.

[0005] Fig. 2 is a three-dimensional perspective of a silicon-on-insulator chip with directional orientations for the silicon layer and the silicon substrate shown.

[0006] Fig. 3 is a three-dimensional perspective of the silicon-on-insulator chip of Fig. 2 showing a transistor placement according to one embodiment of the present disclosure.

[0007] Fig. 4a is a cross section of Fig. 3 showing mesa isolation of the active regions.

[0008] Fig. 4b is a cross section of Fig. 3 showing shallow trench isolation of the active regions.

[0009] Figs. 5a-h illustrate a method for manufacturing the silicon-on-insulator chip of Fig. 3 according to one embodiment of the present disclosure.

## **DETAILED DESCRIPTION**

[0010] It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of various embodiments. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. Moreover, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed interposing the first and second features, such that the first and second features may not be in direct contact.

[0011] Complementary metal oxide semiconductor (CMOS) fabrication processes conventionally use a bulk silicon substrate with a (001) surface crystal orientation as the starting material to fabricate N-type (NMOS) and P-type (PMOS) devices. In such conventional substrates, the formed transistors have a source-to-drain orientation, i.e. channel orientation, in

the  $\langle 110 \rangle$  directions. The notation  $\langle 110 \rangle$  indicates all  $\langle 110 \rangle$  equivalent directions, including the  $[110]$  direction and the  $[\bar{1}10]$  direction for example. Notations for crystal directions and planes commonly used in crystallography are used here. The  $[110]$  and the  $[\bar{1}10]$  directions are perpendicular to the  $(110)$  and  $(\bar{1}10)$  crystal planes, respectively. Incidentally, the  $(110)$  and  $(\bar{1}10)$  planes are silicon crystal planes that cleave very easily.

[0012] Referring to Fig. 1, a silicon-on-insulator substrate 100 is used in one embodiment of the present disclosure. The silicon-on-insulator substrate 100 comprises a silicon layer 30 with a  $(001)$  oriented surface plane. The silicon layer 30 is used as an example in this embodiment, and it is understood that other materials such as a silicon-germanium layer, multi-layer, diamond, gallium, and/or arsenic may be used in place of, or in addition to, the silicon layer 30. For example, a multi-layer may be comprised of a silicon germanium layer and a silicon layer.

[0013] The silicon layer 30 overlies an insulator layer 40. In general, the insulator layer 40 may comprise any dielectric material, inter-metal dielectric material, or insulating material such as silicon oxide, silicon nitride, carbon, or aluminum oxide (also known as sapphire). The dielectric layer may have various dielectric constants and in one embodiment has a dielectric constant of less than about 4.5. The thickness of the insulator may range from 100 angstroms to 2000 angstroms. The insulator layer may also be a composite layer comprising of a stack combination of dielectric materials, such as a aluminum oxide on a silicon oxide stack, or a silicon nitride on a silicon oxide stack. The insulator layer may be in an amorphous state, polycrystalline state, or in crystalline state.

[0014] The insulator layer 40 overlies a substrate 10, which may be a silicon substrate. However, other types of semiconductor substrates may be used. As illustrated by the Miller Index legends 11, 31, in the present embodiment, the silicon substrate 10 is a conventional silicon substrate having a notch 14 oriented in one of the equivalent  $\langle 110 \rangle$  directions. However, the silicon layer 30 has a  $\langle 100 \rangle$  crystal direction pointing in the direction of the notch 14 (downward as shown in Fig. 1). The  $[110]$  direction of the substrate 10 is substantially parallel to the  $[100]$  direction of the silicon layer 30 (e.g. within plus or minus 10 degrees of parallel).

[0015] A first transistor 16, formed on the silicon layer 30, has a source-to-drain direction oriented in the  $[010]$  crystal direction, and a second transistor 18, formed on another portion of

the silicon layer 30, has a source-to-drain direction oriented in the [100] crystal direction. The first and second transistors therefore have source-to-drain directions oriented in one of the  $\langle 100 \rangle$  equivalent directions. The first and second transistors 16, 18 can both be NMOS transistors, both PMOS transistors, or be of different types. By orienting transistors 16, 18 to a  $\langle 100 \rangle$ -equivalent orientation, if stressing is to be used, the relative degradation of one carrier mobility commensurate with a given amount of increase in the mobility of the other type of carrier is reduced.

[0016] Referring now to Fig. 2, the silicon layer 30 (Fig. 1) is semi-processed to form active regions 30a-d where active devices or transistors may be fabricated. The silicon active regions 30a-d have a top (001) oriented crystal surface. The active regions 30a-d may be formed by trenching the silicon layer 30, for example, by plasma etching. A plane 34 depicts where dies 12a, 12b are to be separated or cut. Since the plane 34 that separates the dies 12a, 12b is parallel to a {110} plane or equivalent plane (e.g. a cleavage plane) of the substrate 10, dicing of the substrate is facilitated. Since the plane 34 does not cut through the active regions 30a-d, it is unimportant that it is not parallel to one of their {100}-equivalent planes.

[0017] Referring now to Fig. 3, the gate electrodes 16g, 18g, source regions 16s, 18s, and drain regions 16d, 18d of transistors 16, 18 are illustrated. Transistor 16, formed on one of the silicon active regions 30a, is shown with a source-to-drain direction parallel to the [010] direction of the silicon layer 30. Second transistor 18, formed on a silicon active region 30b, is shown with a source-to-drain direction parallel to the [100] direction of the silicon layer 30. The silicon active regions 30a, 30b, may have been strained, mechanically for example. The strain may be a tensile strain or other strain. In some embodiments, only a portion of the transistors 16, 18 may be strained. For example the channel regions may be strained. In Fig. 3, the gate electrodes 16g, 18g are drawn for illustration purposes only, and are shown to lie only on the active regions. However, in actual devices, the gate electrodes may extend beyond the active regions.

[0018] There are many different types and configurations of circuit elements that may benefit from the present disclosure. For example, in Fig 4a, the trench 36 between active regions 30a, 30b is not filled prior to the fabrication of the transistors 16, 18 (e.g. mesa isolation is used). In another example, in Fig. 4b the trench 36 between active regions 30a, 30b is filled with a trench-filling dielectric 60 prior to the fabrication of the transistors 16, 18 (e.g. shallow trench isolation is used). The trench-filling dielectric 60 may be silicon oxide formed by chemical vapor

deposition, for further example. The trench-filling dielectric 60 may also be silicon oxide deposited by high-density plasma (HDP) deposition.

[0019] Referring to both Figs. 4a and 4b, a thickness  $t_{Si}$  200 of the silicon active regions 30a, 30b may be in the range of 20 angstroms to 2000 angstroms, and in the present embodiment is less than 300 angstroms. In general, the silicon active regions 30a, 30b may not be of the same thickness. It is understood that the cross-sectional views of the silicon active regions (e.g. Fig. 4) are for purposes of illustration only. For example, the silicon active regions 30a, 30b need not have sharp corners. The corners of the silicon active regions 30a, 30b may be faceted or rounded, for example, with a radius of curvature in the range of 10 angstroms to 500 angstroms.

[0020] Referring to Fig. 5a for purposes of continued and further example, a line drawn from the center of the silicon-on-insulator substrate 100 to the notch 14 (Fig. 1) would be pointing out of the page, as illustrated. The [010] crystal direction for the silicon layer 30 and the [110] crystal direction for the silicon substrate 10 are substantially parallel (e.g. within plus or minus 10 degrees of parallel). The silicon-on-insulator substrate 100 may be formed, for example, by a wafer bonding and wafer separation technique.

[0021] Referring now to Fig. 5b, the trenches 36 are formed in the silicon layer 30 (Fig. 5a) to define active regions 30a, 30b. This may be accomplished by forming a patterned mask to cover portions of the silicon layer 30 where active regions 30a, 30b are to be formed, followed by etching of exposed portions of the silicon layer to form the trenches 36. The etching may be a dry plasma etching process, for example. If mesa isolation is used, the trenches 36 would not be filled prior to the formation of transistors. If shallow trench isolation (STI) is used, the trenches 36 would be filled with a trench-filling material (60 of Fig. 5c), such as silicon oxide using a process such as chemical vapor deposition. The resulting structure may be planarized, and the patterned mask removed, to give a structure as shown in Fig. 5c.

[0022] Referring now to Fig. 5d, a gate stack 17 is formed on the active region 30a. The gate stack 17 comprises the gate electrode 16e overlying the gate dielectric 16c. The gate dielectric 16c may be formed on the active region 30a using any gate dielectric formation process known and used in the art (e.g. thermal oxidation, nitridation, sputter deposition, or chemical vapor deposition). The physical thickness of the dielectric 16c may be in the range of 5 to 100 angstroms. The dielectric 16c may employ a conventional gate dielectric such as silicon oxide and silicon oxynitride or a high permittivity (high-k) gate dielectric, or combinations

thereof. The high-k dielectric may have a permittivity of larger than 8, selected from a group comprising of aluminum oxide  $\text{Al}_2\text{O}_3$ , hafnium oxide  $\text{HfO}_2$ , hafnium oxynitride  $\text{HfON}$ , hafnium silicon oxynitride  $\text{HfSiON}$ , hafnium silicate  $\text{HfSiO}_4$ , zirconium oxide  $\text{ZrO}_2$ , zirconium oxynitride  $\text{ZrON}$ , zirconium silicate  $\text{ZrSiO}_4$ , yttrium oxide  $\text{Y}_2\text{O}_3$ , lanthalam oxide  $\text{La}_2\text{O}_3$ , cerium oxide  $\text{CeO}_2$ , titanium oxide  $\text{TiO}_2$ , tantalum oxide  $\text{Ta}_2\text{O}_5$ , or combinations thereof. In one embodiment, the high-k dielectric is hafnium oxide. The silicon oxide equivalent thickness (EOT) of the dielectric 16c may be larger than 5 angstroms, and in the present embodiment is larger than 20 angstroms. The physical thickness of the dielectric 16c may be larger than 5 angstroms and in the present embodiment is larger than 40 angstroms.

[0023] A material for the gate electrode 16e may be deposited on the dielectric 16c. The gate electrode material 16e may comprise conventional poly-crystalline silicon, poly-crystalline silicon germanium, metals, metallic silicides, metallic nitrides, or conductive metallic oxide. In one embodiment, the electrode 16e comprises poly-crystalline silicon. Metals such as molybdenum, tungsten, titanium, tantalum, platinum, and hafnium may also be used as a portion of the electrode 16e. Metallic nitrides may include, but will not be restricted to, molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride. Metallic silicides may include, but will not be restricted to, nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide. Conductive metallic oxides may include, but will not be restricted to, ruthenium oxide and indium tin oxide.

[0024] The gate electrode material may be deposited by conventional techniques such as chemical vapor deposition. The gate electrode 16e may also be formed by the deposition of silicon and metal, followed by an anneal to form a metal silicide gate electrode material. A patterned gate may then be formed on the gate electrode material using deposition and photolithography techniques. The gate mask may employ commonly used masking materials such as, but not limited to, silicon oxide, silicon oxynitride, and silicon nitride. The gate electrode material is then etched using plasma etching processes to form the gate electrode 16e. The gate dielectric material on regions not covered by the gate electrode 16e is usually etched away.

[0025] Referring now to Fig. 5e, a source and drain extension implant may be performed. A spacer 72 is formed, for example, by deposition of a spacer dielectric (e.g. silicon nitride) followed by anisotropic etching. It is understood that the spacer dielectric 72 may in fact

comprise a multi-layer of different dielectrics, e.g. silicon nitride on silicon oxide. This may be followed by a second and deeper source and drain implant.

[0026] Referring now to Fig. 5f, a resistance of the source 16s, drain 16d, and gate electrode 16e in the transistor 16 may be reduced by strapping the source/drain regions with a silicide 76, e.g. using a self-aligned silicide (salicide) process, or other metal deposition process. A mask, e.g. an oxide, is may be used prior to the silicidation process to cover portions of the substrate where silicidation is not intended (e.g. an active region where the resistance is to be kept high). For example, the oxide mask may cover an active region while the silicidation process is performed to form silicides on the gate electrode 16e, and source region 16s, and drain region 16d of the transistor.

[0027] Referring now to Fig. 5g, a high stress film 80 may be deposited, followed by the deposition of a passivation layer 82. The high stress film 80 may be a silicon nitride or silicon oxynitride film deposited by plasma-enhanced chemical vapor deposition. In the present embodiment, the high stress film 80 is deposited over NMOS and PMOS transistors. The high stress film 80 may have a stress magnitude in the range of 200 MPa to 2 GPa. When the thickness of the active region (30a, 30b of Fig. 5b) is thinner, the resulting stress in the channel region of the transistor is larger. Stress in the channel region also increases when the gate (e.g. 16g of Fig. 3) length is reduced.

[0028] Referring now to Fig. 5h, contact holes may be etched through the passivation layer 82, stopping on the contact etch stop layer. A conductive material is then filled into the contact holes to form conductive contacts 84 to the transistor.

[0029] Although in this disclosure, particular embodiments have been described in detail, it is understood that the disclosure is not limited correspondingly in scope, but includes all changes, modifications, and equivalents coming within the spirit and terms of the claims appended hereto. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense.

**WHAT IS CLAIMED IS:**

1. An integrated circuit comprising:  
a semiconductor substrate having <100> orientation,  
at least one field effect transistor on said substrate, said transistor having at least one gate electrode,  
at least three interconnection electrical contacts with said transistor.
2. The integrated circuit of claim 1, wherein said semiconductor substrate comprises at least one from a group consisting of silicon, germanium, gallium, and arsenic.
3. The integrated circuit of claim 1, wherein the transistor comprises a gate dielectric underlying said gate electrode and wherein the gate dielectric has a dielectric constant greater than 8.
4. The integrated circuit of claim 1, wherein said gate electrode is a metal gate.
5. The integrated circuit of claim 1, wherein said gate electrode is polysilicon gate.
6. The integrated circuit of claim 1 further comprising at least one inter-metal dielectric interposing the at least one transistor and the substrate.
7. The inter-metal dielectric of claim 6, wherein said dielectric comprises silicon, nitrogen, carbon, or combinations thereof.
8. The inter-metal dielectric of claim 6, wherein said dielectric has a dielectric constant less than 4.5

9. A semiconductor device, comprising:  
a silicon active region overlying an insulator layer, the silicon active region having a (001) oriented top surface and a  $\langle 100 \rangle$  crystal direction; and  
a substrate underlying the insulator layer, the substrate having a  $\langle 110 \rangle$  crystal direction;  
wherein the  $\langle 100 \rangle$  direction of the silicon active region is substantially parallel to the  $\langle 110 \rangle$  direction of the substrate.
10. The semiconductor device of claim 9 wherein the substrate is a silicon substrate having a (001) oriented top surface.
11. The semiconductor device of claim 10 wherein the silicon active region has a tensile strain.
12. The semiconductor device of claim 11 wherein the tensile strain is substantially in the  $\langle 100 \rangle$  crystal direction.
13. The semiconductor device of claim 9 further comprising a first transistor of a first conduction type formed on the silicon active region and having a strained channel region.
14. The semiconductor device of claim 13 wherein the first conduction type is N-type.
15. The semiconductor device of claim 13 wherein the strained channel region has a tensile strain in a source-to-drain direction.
16. The semiconductor device of claim 13 further comprising a stress film formed on the first transistor wherein the stress film has a magnitude in the range of 200MPa to 2Gpa.
17. The semiconductor device of claim 16 wherein the high stress film comprises silicon and nitrogen.

18. The semiconductor device of claim 9 wherein the silicon active region has a thickness in the range of 20 angstroms to 500 angstroms.
19. The semiconductor device of claim 9 wherein the silicon active region has rounded corners.
20. A semiconductor device comprising:  
an insulator layer;  
a silicon active region positioned on a first side of the insulator layer, wherein the silicon active region has a first crystal direction;  
a substrate positioned on a second side of the insulator layer, wherein the substrate has a second crystal direction that is offset from the first direction.
21. The semiconductor device of claim 20 wherein the offset comprises the first direction being a  $\langle 100 \rangle$  direction and the second direction being a  $\langle 110 \rangle$  direction that is parallel with the first direction.
22. The semiconductor device of claim 20 wherein the silicon active region and the substrate have a (001) oriented top surface.
23. The semiconductor device of claim 20 wherein the silicon active region has a tensile strain.
24. The semiconductor device of claim 20 further comprising a first transistor of a first conduction type formed on the silicon active region and having a strained channel region.
25. The semiconductor device of claim 24 wherein the strained channel region has a tensile strain in a source-to-drain direction.

26. The semiconductor device of claim 23 further comprising a stress film formed on the first transistor wherein the stress film has a stress magnitude in the range from about 200 MPa to about 2GPa.

27. The semiconductor device of claim 25 wherein the silicon active region has a thickness in the range of 20 angstroms to 2000 angstroms.

28. The semiconductor device of claim 25 wherein the silicon active region has faceted corners.

29. A semiconductor chip comprising:  
first and second active regions overlying an insulator layer, the active regions having a (001) oriented top surface and a  $\langle 100 \rangle$  crystal direction; and  
a substrate underlying the insulator layer, the substrate having a  $\langle 110 \rangle$  crystal direction;  
wherein the  $\langle 100 \rangle$  direction of the silicon active regions are substantially parallel to the  $\langle 110 \rangle$  direction of the substrate.

30. The semiconductor chip of claim 29 further comprising a first N-channel transistor formed on the first active region and a first P-channel transistor formed on the second active region.

31. The chip of claim 30 wherein the first N-channel transistor and the first P-channel transistor each have a strained channel region.

32. The chip of claim 31 wherein the substrate is a silicon substrate having a (001) oriented top surface.

33. The chip of claim 29 wherein the silicon active region has a thickness in the range of 20 angstroms to 300 angstroms.

34. The chip of claim 29 wherein the first N-channel transistor and the first P-channel transistor are isolated using mesa isolation or shallow trench isolation.

35. A silicon-on-insulator semiconductor device comprising:  
a silicon active region overlying an insulator layer, the silicon active region having a (001) oriented top surface and a <100> crystal direction;  
a substrate underlying the insulator layer; and  
a first transistor formed on a portion of the silicon active region, the first transistor having a strained channel region.

36. The silicon-on-insulator semiconductor device of claim 35 further comprising a stress film formed on at least the first transistor, wherein the stress film has a magnitude ranging from about 200 MPa to about 2 GPa.

37. The silicon-on-insulator semiconductor device of claim 35 wherein the first transistor comprises a gate dielectric selected from a group consisting of silicon oxide, silicon oxynitride, silicon nitride, or combinations thereof.

38. The silicon-on-insulator semiconductor device of claim 37 wherein the first transistor comprises a gate dielectric selected from a group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium oxide, tantalum oxide, or combinations thereof.

39. The device of claim 35 wherein the first transistor comprises a gate electrode selected from a group consisting of poly-crystalline silicon, poly-crystalline silicon-germanium, a metal, a metallic nitride, a metallic silicide, a metallic oxide, or combinations thereof.

40. A method of forming a semiconductor device, comprising the steps of:  
providing a semiconductor structure comprising a plurality of silicon active regions overlying an insulator layer, the silicon active regions having a (001) oriented top surface and a  $\langle 100 \rangle$  crystal direction;  
providing a substrate underlying the insulator layer, the substrate having a  $\langle 110 \rangle$  crystal direction wherein the  $\langle 100 \rangle$  direction of the silicon active regions is substantially parallel to the  $\langle 110 \rangle$  direction of the substrate;  
forming a gate stack on at least one of the silicon active regions;  
forming source and drain regions oppositely adjacent to the gate stack to form a transistor, the transistor having a source to drain direction being substantially aligned with the  $\langle 100 \rangle$  crystal direction of the active regions; and  
forming a stress film over at least the transistor.

41. The method of claim 40 further comprising the steps of:  
forming a passivation layer over the stress film;  
forming contact holes in the passivation layer; and  
filling the contact holes with a conductive material to form electrical contacts to the transistor.

42. The method of claim 40 wherein the silicon active regions have a thickness in the range of 20 angstroms to 500 angstroms.

43. The method of claim 40 wherein the silicon active regions are isolated from one another by mesa isolation or shallow trench isolation.

44. The method of claim 40 wherein the step of forming a gate stack comprises:  
forming a gate dielectric; and  
forming a gate electrode;  
wherein the gate dielectric is selected from a group consisting of aluminum oxide,  
hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride,  
zirconium silicate, yttrium oxide, lanthalam oxide, cerium oxide, titanium oxide, tantalum oxide,  
or combinations thereof.