WHAT IS CLAIMED IS:

1. A method of erasing a non-volatile memory device, the non-volatile memory device including a plurality of cell strings having a plurality of memory cells and selection transistors connected together, wherein the selection transistors are located at ends of each of the plurality of cell strings, the method comprising:

performing a first erase operation based on an erase voltage and an erase control voltage, the erase voltage being applied to a drain electrode of at least one of the selection transistors and the erase control voltage being applied to a gate electrode of the at least one of the selection transistors;

determining whether there are slow erase cells among the plurality of memory cells by performing a multiple erase verify operation based on a first verify voltage and a second verify voltage, the second verify voltage being higher than the first verify voltage;

adjusting, in response to determining that the slow erase cells are present, the erase control voltage to generate an adjusted erase control voltage such that a voltage difference between the erase voltage and the adjusted erase control voltage is greater than a voltage difference between the erase voltage and the erase control voltage;

increasing the erase voltage and the erase control voltage by an identical voltage level, in response to determining that the slow erase cells are not present; and

performing a second erase operation based on the adjusted erase control voltage,

wherein determining whether there are slow erase cells comprises:

performing a first erase verify operation based on the first verify voltage;

determining whether the erasing is associated with an erase pass or an erase fail based on the first erase verify operation;

performing, in response to the erase fail, a second erase verify operation based on the second verify voltage; and

determining whether the slow erase cells are present based on the second erase verify operation.

2. The method of claim 1, wherein the adjusting of the erase control voltage comprises:

reducing the erase control voltage while maintaining the erase voltage.

3. The method of claim 1, wherein the adjusting of the erase control voltage comprises:

reducing the erase control voltage while increasing the erase voltage.

4. The method of claim 1, wherein the determining whether the slow erase cells are present comprises:

determining that the slow erase cells are present, in response to a number of second fail bits associated with the second erase verify operation being greater than or equal to a reference number.

5. The method of claim 1, wherein the determining whether there are slow erase cells comprises:

determining that the slow erase cells are present, in response to a ratio of a number of second fail bits associated with the second erase verify operation to a number of first fail bits associated with the first erase verify operation being equal to or greater than a reference ratio.

6. The method of claim 1, wherein the determining whether the erasing is associated with the erase pass or the erase fail comprises:

determining a first erase fail when a number of first fail bits associated with the first erase verify operation is greater than or equal to a first reference number,

determining a second erase fail when the number of the first fail bits is greater than or equal to a second reference number, the second reference number being less than the first reference number, and the method further comprises:

increasing the erase voltage and the erase control voltage by an identical voltage level, in response to the first erase fail; and

performing the second erase verify operation based on the second verify voltage, in response to the second erase fail.

7. The method of any one of claims 1, 4, 5 or 6, wherein the adjusting of the erase control voltage comprises:

reducing the erase control voltage while maintaining the erase voltage, in response to a number of second erase fail bits associated with the second erase verify operation being less than a third reference number, and

increasing the erase voltage and reducing the erase control voltage, in response to the number of second erase fail bits being greater than or equal to the third reference number.

8. The method of any one of claims 1 to 7, further comprising:

storing, in a storage region, an indication of whether the slow erase cells are present;

performing a write operation on the plurality of memory cells; and

determining whether to perform the multiple erase verify operation based on the indication stored in the storage region.

9. The method of any one of claims 1 to 8, wherein the selection transistors include a ground selection transistor and a string selection transistor, and

performing the first erase operation and the second erase operation include applying the erase voltage to drain electrodes of each of the ground selection transistor and the string selection transistor, and applying a respective one of the erase control voltage and the adjusted erase control voltage to gate electrodes of each of the ground selection transistor and the string selection transistor.

10. The method of any one of claims 1 to 8, wherein the selection transistors include a ground selection transistor and a string selection transistor, and

the performing the first erase operation and the second erase operation include applying the erase voltage to a drain electrode of the string selection transistor, and applying a respective one of the erase control voltage and the adjusted erase control voltage to a gate electrode of the string selection transistor.

11. The method of any one of claims 1 to 10, wherein the first erase operation and the second erase operation are performed based on a leakage current generated from the drain electrode due to a voltage difference between the drain electrode and the gate electrode of the at least one of the selection transistors.

12. The method of any one of claims 1 to 11, wherein the non-volatile memory device includes a memory block in which the plurality of memory cells and the selection transistors are stacked in a direction perpendicular to a substrate.

13. A method of erasing a non-volatile memory device, the non-volatile memory device including a plurality of cell strings having memory cells and selection transistors connected together, wherein the selection transistors are located at ends of each of the plurality of cell strings, the method comprising:

performing a first erase operation based on an erase voltage and an erase control voltage, the erase voltage being applied to a drain electrode of at least one of the selection transistors and the erase control voltage being applied to a gate electrode of the at least one of the selection transistors;

detecting whether each of the plurality of cell strings are erase-passed or erase-failed by performing an erase verify operation based on a verify voltage;

determining whether there is an erase-passed cell string, when an erase fail is determined;

increasing the erase voltage and the erase control voltage by an identical voltage level, when it is determined that there is no erase-passed cell string among the plurality of cell strings;

adjusting the erase control voltage to generate an adjusted erase control voltage such that, when at least some of the plurality of cell strings are erase-passed, a voltage difference between the erase voltage and the adjusted erase control voltage is greater than a voltage difference between the erase voltage and the erase control voltage; and

performing a second erase operation based on the adjusted erase control voltage.

14. The method of claim 13, wherein the performing the second erase operation comprises:

inhibiting erasing of the at least some of the cell strings that are erase-passed.

15. The method of claim 13 or claim 14, wherein the selection transistors include a ground selection transistor and a string selection transistor, and

the performing the first erase operation and the second erase operation include applying the erase voltage to a drain electrode of each of the ground selection transistor and the string selection transistor, and applying a respective one of the erase control voltage and

the adjusted erase control voltage to a gate electrode of each of the ground selection transistor and the string selection transistor.

16. The erasing method of claim 15, wherein, the performing the second erase operation comprises:

applying the erase voltage to a drain electrode of the string selection transistor;

applying the adjusted erase control voltage to a gate electrode of the string selection transistor; and

setting a drain electrode and a gate electrode of the ground selection transistor to a floated state.

17. A non-volatile memory device comprising:

a memory block including a plurality of cell strings, each cell string including memory cells and a selection transistor stacked in a direction perpendicular to a substrate, the selection transistor being located at an end of each of the plurality of cell strings and including a drain electrode and a gate electrode; and

a control logic configured to,

determine whether slow erase cells are present among the memory cells based on a result of verification according to multiple sensing based on a first verify voltage and a second verify voltage when performing an erase-verify iteration on the memory block, and

adjust, in response to determining that the slow erase cells are present, an erase control voltage to generate an adjusted erase control voltage such that a voltage difference between an erase voltage provided to the drain electrode of the selection transistor of each of the plurality of cell strings, and the adjusted erase control voltage provided to the gate electrode of the selection transistor of each of the plurality of cell strings, is greater than a voltage difference between the erase voltage and the erase control voltage.

18. The non-volatile memory device of claim 17, wherein the control logic is configured to increase the erase voltage and the erase control voltage by an identical voltage level in response to determining that the slow erase cells are not present.