A NOVEL TEST STRUCTURE FOR AUTOMATIC DYNAMIC NEGATIVE-BIAS TEMPERATURE INSTABILITY TESTING

ABSTRACT

The invention describes a novel test structure and process to create the structure for performing automatic dynamic stress testing of PMOS devices for Negative Bias Temperature Instability (NBTI). The invention consists of an integrated inverter, two integrated electronic switches for switching from stress mode to device DC characterization measurement mode, and a PMOS FET device under test (DUT). The inverter assures the proper 180 degree phase relationship between the test device source and gate voltage while the imbedded electronic switches provide isolation of the test device during DC characterization testing. Another embodiment of the invention enables the testing of multiple devices under test (DUT's).

FIG. 7