



## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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| <b>(51) International Patent Classification <sup>7</sup>:</b><br><b>H03M 13/00, H04L 1/00</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                               | <b>A1</b> | <b>(11) International Publication Number:</b> <b>WO 00/08769</b><br><b>(43) International Publication Date:</b> 17 February 2000 (17.02.00)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>(21) International Application Number:</b> PCT/US99/17659<br><b>(22) International Filing Date:</b> 4 August 1999 (04.08.99)<br><b>(30) Priority Data:</b><br>09/129,022      4 August 1998 (04.08.98)      US<br><b>(71) Applicant:</b> QUALCOMM INCORPORATED [US/US]; 6455 Lusk Boulevard, San Diego, CA 92121 (US).<br><b>(72) Inventor:</b> HANSQUINE, David; Apartment 717, 7510 Charmant Drive, San Diego, CA 92122 (US).<br><b>(74) Agents:</b> MILLER, Russell, B. et al.; Qualcomm Incorporated, 6455 Lusk Boulevard, San Diego, CA 92121 (US). |           | <b>(81) Designated States:</b> AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).<br><br><b>Published</b><br><i>With international search report.<br/>         Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i> |

**(54) Title:** CACHED CHAINBACK RAM FOR SERIAL VITERBI DECODER**(57) Abstract**

A serial Viterbi decoder having a chainback cache is provided for use in a mobile telephone. In one embodiment described herein, the decoder includes a branch error metric block, an add-compare-select unit, and a chainback block including a chainback RAM, a full chainback cache and chainback controller circuitry. The chainback cache caches decision bits from previous process cycles such that full chainback operations need not always be performed. The chainback cache is configured to cache on all reads. With the chainback cache, significant savings in power consumption and processing time may be achieved with only a relatively modest increase in the amount of circuitry required. In another embodiment, a full chainback cache is not provided. Rather, the chainback block instead includes an L+1 bit RAM, an updown counter and a shift register configured to emulate a chainback cache. In still another embodiment, an L bit shift register is employed instead of the combination of the L+1 bit RAM and updown counter. In the various embodiments, the chainback block may be configured to perform only one chainback read in each process cycle or may be configured to perform *m* chainback reads in each process cycle. In still other embodiments, the chainback block is configured to perform chainback operations based on *a* through *b* reads where the cache is accessed for each read after *a* reads have been done until *b* reads have been performed or a match is obtained. In still further embodiments, the chainback block is configured to perform chainback operations over multiple process cycles rather than only a single process cycle.

