Description

The present invention relates to an arbitration circuit according to the preamble of claim 1.

Such a circuit is known from US-A-4 240 138. This known circuit under use of latches and gates operates as an asynchronous logic control circuit which distributes a request for access to a memory on a pure priority order, i.e. in the order of the arrival of the request. Therefore, a repeating higher priority requestor will always have its request entered and granted in preference to an earlier requesting lower priority requestor preventing the lower priority requestor from ever gaining access to the common resource.

Furthermore, EP-A-0 122 773 shows an arbitrator circuit within a memory interface which includes circuitry for granting poll requests of controllers in a prescribed manner of protocol.

Finally, US-A-3 603 935 discloses a priority access system for handling overlapping requests at the communication between a plurality of processors and a memory where the requests after acceptance are serviced on a predetermined priority basis.

Departing from the above mentioned prior art, it is the object of the present invention to devise an arbitration circuit which prevents transmission of a new request as long as an earlier granted access is processed. This object is achieved according to the characterizing features of claim 1. Further advantageous embodiments of the inventive arbitration circuit may be taken from the dependent claims.

The present invention will become more apparent when taken in conjunction with the following description and the attached drawings where like characters indicate like parts and where

Figure 1 shows a block diagram of a system which utilizes an arbitration circuit of the present invention;

Figure 2 shows a timing diagram of a bus cycle interacting with a memory bus;

Figure 3 shows a timing diagram of the arbitration circuit of the preferred embodiment of the present invention;

Figure 4 shows a logic diagram of the arbitration circuit of the preferred embodiment of the present invention;

Figures 5A, 5B, and 5C, which taken together comprise Figure 5, shows the various waveforms of the logic diagram of the arbitration circuit of Figure 4, for three different timing conditions of the request signals; and

Figure 6A and 6B, taken together comprise Figure 6, shows a logic diagram of an arbitration circuit having three requestors.

Referring to Figure 1, a block diagram is shown of a system which utilizes an arbitration circuit of the present invention. The system of Figure 1 shows a two bus system, designated IO BUS 11 and CPU BUS 12. A plurality of the devices (not shown) coupled to the IO BUS 11 desires to inteface with a memory via a memory bus (not shown). Likewise, a plurality of devices (not shown) coupled to the CPU BUS 12 desires to interface with a memory via the memory bus (not shown) having an associated memory bus controller (not shown). Both the IO BUS 11 and CPU BUS 12 can include a bus controller for resolving which of the devices attached thereto will have access to the respective buses. The details of the operation of the bus and the bus controller are not necessary for an understanding of the present invention and will not be discussed further herein.

The IO BUS 11 is operatively connected to a multiplexer (MUX) 15 via an IOADDRESS line 18, an IODATA line 19, and an I/O read/write line 20. The CPU BUS 12 is operatively connected to the MUX 15 via a CPUADDRESS line 21, a CPUDATA line 22, and CPU read/write line 23. When (a device coupled to) the IO BUS 11 desires to communicate with the memory (not shown) a request is made to an arbitration circuit 30 via the RQIO line 31. When (a device coupled to) the CPU BUS 12 desires to communicate with a memory (not shown) a request is made to the arbitration circuit 30 via the RQCPU line 32.

The arbitration circuit 30 will grant a request to access memory by generating a phase 1, phase 2, and phase 3 signals corresponding to either the IO BUS 11 or the CPU BUS 12. The phase 1 signal is coupled to the memory bus controller (not shown) to indicate a memory cycle request has been initiated and allows the memory to set up its logic for the memory cycle. The phase 2 signals (PHASE2IO, PHASE2CPU) are coupled to the MUX 15 to perform the selection function (S), thereby selecting the address and/or data from either the IO BUS 11 or CPU BUS 12, the selected address and data being transmitted to the memory bus controller (not shown) via the ADDRESS and DATA lines 35, 36 (or data returned for a memory read operation), and the selected read/write operation is transmitted to the memory bus controller (not shown) via read/write line 37. The phase 3 signal is transmitted back to the respective bus, PHASE3IO signal being transmitted to the IO BUS 11 via PHASE3IO line 38, and the PHASE3CPU signal being transmitted to the CPU BUS 12 via the PHASE3CPU line 39. When the requests are made to the arbitration circuit 30 in a simultaneous or near simultaneous time frame, the arbitration circuit 30 will resolve the timing of the request and permit only one bus to have access to the memory. When the memory cycle initiated by the IO BUS 11 is completed, the memory bus controller (not shown) transmits a cycle complete A (CCA) signal back to the arbitration circuit 30. Likewise, when the memory cycle initiated by the CPU BUS 12 is completed, the memory bus controller (not shown) transmits a cycle complete B (CCB) signal back to the arbitration circuit 30.

Referring to Figure 2, a timing diagram of a bus cycle interacting with the memory bus/memory is shown. A bus cycle is divided into three parts comprising request/arbitration, memory cycle, and retraction. The first part is the request/arbitration. When a bus requests communication with the memory unit, the arbitration circuit 30 responds to the re-

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quest and allows the communication to proceed. If two (or more) requests are made, the arbitration circuit will resolve the conflict. If the requests are made simultaneously or nearly simultaneously, then the resolution is made on a priority basis. Otherwise, the arbitration circuit 30 determines which bus made the request first and permits the bus making the first request to communicate with the memory unit. (Although the following description centers on the request being made from two buses, it will be understood that the arbitration can be made between three or more buses.)

The second part of the bus cycle is the memory cycle. This is the time in which the memory is performing the actual reading or writing. The third part of the bus cycle is the retraction. This includes any post memory cycle activity formed by the bus interface unit which includes error correction and detection functions, parity checking, etc. Typical values for the memory cycle of the present invention is 250 nano seconds and a typical value for the bus cycle of the present invention is 500 nano seconds.

Referring to Figure 3, a timing diagram of the arbitrator circuit 30 is shown. When a request is made by the IO BUS 11, request signal RQIO is raised. For purposes of example only, shortly thereafter, assume a request is made from the CPU BUS 12, and request signal RQCPU is raised. The arbitration takes place (ARB) and the request is granted to the IO BUS 11. The phase 1 signal is raised, and the phase 2 and the phase 3 signals are raised for the IO BUS 11, PHASE1, PHASE2IO, and PHASE3IO, respectively. During phase 1, write data is latched from the appropriate requestor. In the preferred embodiment error detection and correction (EDAC) check-bit generation occurs for write request operations, and some internal checking of address, read/write, etc. is performed. During phase 2, (PHASE2IO), address and read/write setup and hold time occurs on the bus. The phase 3 signal indicates a cycle is in process. Since phase 3 is transmitted back to the bus (PHASE3IO TO BUS 11), the bus knows the request has been acknowledged and lowers the request signal RQIO. The memory cycle begins with the end of phase 1. The end of the memory cycle corresponds with the beginning of EDAC time, which can also be considered as phase 4. EDAC time (or phase 4) routes the read data to the appropriate requestor and an EDAC check-bit comparison is performed for a read operation. At the completion of phase 2, the arbitration function (ARB) occurs again and the request pending from the CPU BUS 12 is acknowledged. The phase 1, phase 2, and phase 3 signals for the CPU BUS 12 are raised, PHASE1, PHASE2CPU, and PHASE3CPU, respectively. At the completion of the PHASE3IO signal, the lowering of the phase 3 signal indicates to the IO BUS 11 that the operation to the memory unit is complete (denoted in Figure 3 as memory cycle complete).

Cycle B cannot begin until the end of cycle A phase 2. Cycle A phase 4 cannot begin until the end of cycle B phase 1. Cycle A cannot begin until the end of cycle B phase 2. Cycle B phase 4 cannot begin until the end of cycle A phase 1. From this one can see that phase 1 and phase 4 are always mutually exclusive (non-overlapping). Phase 2 of cycle A and phase 2 of cycle B are always mutually exclusive (non-overlapping). Phase 3 of cycle A and phase 3 of the cycle B can and do overlap. The arbitration period for cycle B (phase 1, phase 2 and phase 3) can only begin when cycle A phase 2 has ended. The arbitration period for cycle A (phase 1, phase 2 and phase 3) can only begin when cycle B phase 2 has ended.

Referring to Figure 4, the logic diagram of the arbitration cicruit 30 is shown. A first and second comparator (COMP1, COMP2) 301, 302 are utilized to determine if a request signal is to be accepted. Request signal RQIO enables COMP1 301 and request signal RQCPU enables COMP2 302. The comparators 301, 302 determine the condition upon which a request will be accepted. If a phase 2 signal is high for the other requestor bus, then a no compare condition exists and the comparator will not pass the request signal. For example, referring to Figure 3, at time T_a, PHASE2IO is high so COMP2 302 will not pass the request signal RQCPU. At time T_b, PHASE2IO is low and PHASE3CPU is low, generating a compare condition and hence a request signal RQCPU is outputted from COMP2 302. If a request signal RQIO existed at time T_a, COMP1 301 would not pass the request signal RQIO, since PHASE3IO is high at this time because all the bus functions are not completed.

Referring back to Figure 4, the output COMP1 301 is coupled to OR-gate 303 and to a corresponding D-type flip-flop 305. The output of COMP2 302 is coupled to the OR-gate 303 and to a D-type flip-flop 306. The output of OR-gate 303 is coupled to a first delay, delay A, 308 and the output of delay A 308 is coupled to a second delay, delay B, 309 and is also coupled to the clock input of the D-type flip-flops 305, 306. Five J-K type flip-flops comprise the PHASE1 flip-flop 321, PHASE2IO flip-flop 322, PHASE3IO flip-flop 323, PHASE2CPU flip-flop 324, and PHASE3CPU flip-flop 325. The output of delay B 309 is coupled to a transmission gate (sometimes referred to herein as a driver) 310 which is coupled to the set input of PHASE1 flip-flop 321. The output of delay B 309 is also coupled to an input of NAND GATE 311 and NAND GATE 312. The Q output of D type flip-flop 305 is coupled to NAND GATE 311. A Q bar output of D type flip-flop 305 is coupled to NAND GATE 312, and the Q output of D-type flip-flop 306 is coupled to NAND GATE 312. The output of NAND GATE 311 is coupled to the set input of PHASE2IO flip-flop 322 and to the set input of PHASE3IO flip-flop 323. The output of NAND GATE 312 is coupled to the set input of PHASE2CPU flip-flop 324 and to the set input of PHASE3CPU flip-flop 325. The J-K input of the five J-K type flip-flops are connected to ground, or a logic 0, and the clear input of the five J-K type flip-flops are connected to a system reset (RESET). The T input of PHASE1 flip-flop 321 is connected to a timer T_r which resets the flip-flop. The T input of PHASE2IO flip-flop 322 is coupled to a second timer [illegible] and the T input of the PHASE2CPU flip-flop

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324 is also connected to the T_s timer. This timer, T_s (not shown), is initiated at the time the PHASE1 flip-flop 321 is reset and the time out occurs at a predetermined time yielding the wave form as shown in Figure 3, the time being selected to give a required amount of time to perform the desired function. When the timer times out the respective flip-flop is reset. The T input of PHASE3IO flip-flop 323 receives the cycle complete A (CCA) and the T input of the PHASE3CPU flip-flop 325 receives the cycle complete B signal (CCB) from the memory bus controller.

The operation of the arbitration circuit 30 will now be described in conjunction with Figure 5A, 5B, and 5C, which taken together comprise Figure 5. Figure 5A shows a request RQIO being made at time T_0, and request RQCPU being made a short time thereafter. The output of COMP1 301 (waveform A) is shown delayed by the operation of COMP1 301. (For purposes of example only the delays shown herein are representative and are shown to be essentially equal for each element of arbitration circuit 30.) The output of OR-gate 303 (waveform B) is shown delayed to include the proprogation time through OR-gate 303, and the output of delay A 308 (waveform C) is shown again delayed by the delay time of the delay A 308 (in the preferred embodiment the delay is to exceed the setup time requirements of the D-type flip-flops 305, 306). Since the D input to flip-flop 305 is high as a result of waveform A, when the clock input goes high, the D-type flip-flop 305 is set and Q output (waveform D) goes high, and conversely the Q bar output goes low (waveform E). NAND GATE 311 is partially qualified by the output signal of D-type flip-flop 305. The output of delay B 309, which in the preferred embodiment is to exceed the metastable time of the D-type flip-flops 305, 306, is a combined request signal which indicates a request is in progress. When the combined request signal of delay B 309 is outputted (waveform G), NAND GATE 311 is qualified setting the PHASE2IO and PHASE3IO flip-flops thereby outputting the PHASE2IO and the PHASE3IO signal enabling the communication path from the IO BUS to the MEMORY BUS, effectively acknowledging the RQIO request. When the combined request signal of delay B 309 is outputted (waveform G), transmission gate 310 sets PHASE1. The Q bar output of D-type flip-flop 305 disables NAND GATE 312 so that when the output of D-type flip-flop 306 is set (waveform F), the effect of this signal is nullified by the Q bar output of D-type flip-flop 305 to NAND GATE 312. Note that the output of COMP2 302 will go high (waveform A') since PHASE3CPU and PHASE2IO are both low at this time.

Figure 5B shows the wave forms of the various signals through arbitration circuit 30 when a request signal is made from the CPU BUS. In this case the output of COMP2 302 goes high after the request is made and likewise the output of OR-gate 303 (waveform B) goes high and when the output of delay A 308 (waveform C) goes high, D-type flip-flop 306 is set resulting in the Q output of D-type flip-flop 306 going high (waveform F) which partially enables NAND GATE 312. Since D type flip-flop 305 is not set, the Q bar output (waveform E) is high further partially enabling NAND GATE 312. When the combined request signal is outputted from delay B 309 (waveform G) NAND GATE 312 is completely enabled thereby setting PHASE2CPU flip-flop 324 and PHASE3CPU flip-flop 325 generating the respective phase 2 and phase 3 signals thereby granting the MEMORY BUS access to the CPU BUS. When the combined request signal delay B 309 is outputted (waveform G), transmission gate 310 sets PHASE1.

Figure 5C shows a near simultaneous request between the request signals from the CPU BUS 12 and IO BUS 11. At time T_0, RQCPU goes high resulting in the output of COMP2 302 (waveform A') going high, the output of OR-gate 303 (waveform B) going high, and the output of delay A 308 (waveform C) going high. When waveform C goes high, since the D input to D-type flip-flop 306 is high (waveform A'), the Q output of D-type flip-flop 306 goes high also (waveform F), partially enabling NAND GATE 312. The output of delay B 309 (waveform G) is essentially that of the waveform C delayed by the delay time of delay B 309. The request from the IO BUS RQIO occurs a short time after the request from the CPU BUS. Since neither PHASE3IO nor PHASE3CPU are high, or logic one, shortly after time T_0, COMP1 301 is qualified resulting in a request signal RQI0 being transmitted (waveform A). Since the D input of D-type flip-flop 305 is high at the time when the waveform C signal goes high (the clock input to D-type flip-flop 305) D-type flip-flop 305 is set resulting in the Q output of D-type flip-flop 305 (waveform D) going high and conversely the Q bar output of D-type flip-flop 305 being reset, or going low, (waveform E). The Q bar output of D-type flip-flop 305 (waveform E disables NAND GATE 312. The Q output of D-type flip-flop 305 (waveform D) partially enables NAND GATE 311, so that when the signal of waveform G goes high NAND GATE 311 is enabled resulting in the request being granted to the IO BUS, shown in Figure 5C as the PHASE2IO and PHASE3IO signals going high. Thus, in this case, even though the request signal RQIO was made shortly after the request signal from the CPU BUS, the request from the IO BUS was granted first as a matter of priority. Anytime between T_0 and T_x is the simultaneous or near simultaneous occurrence of the request. If the RQIO signal occurs at or after time T_x, then the signal of waveform A will not be present at D-type flip-flop 305 so that the waveform C will not cause a change in state of the D-type flip-flop 305 and NAND GATE 311 will not be enabled nor will NAND GATE 312 be disabled.

Figure 6 (comprised of Figure 6A and 6B) shows an alternative embodiment of the present invention having three requestors, the CPU bus, the IO bus, and a third bus, XBUS. The conditions of the comparators 301, 302, and 304 include the condition for when the third bus can be granted access to the memory unit. It will be understood by those skilled in the art that additional conditions may be added to the comparators when it is desired to prevent trans-

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mission of the request.

Claims

1. An arbitration circuit (30), for determining which one of a plurality of request signals from a plurality of requestors (11, 12) is to be acknowledged and granted access to a common bus (35, 36, 37) having an associated bus controller, said arbitration circuit comprising

a) an enabling means (301, 302, 304) for each requestor (11, 12) for receiving:

i) the request signal (RQIO, RQCPU) of said requestor (11, 12),

characterised in that said enabling means further receives

ii) first signals (PHASE 2) denoting the granting to any one of the other requestors of access to the common bus (35, 36, 37), and

iii) second signals (PHASE 3) denoting that said requestor has been granted access to the common bus (35, 36, 37) and is engaged in completing the operation of communicating with the common bus,

with said enabling means (301, 302, 304) transmitting said request signal (RQIO, RQCPU) of said requestor (11, 12) only if none of said denoting signals (PHASE 2, PHASE 3) are present;

b) said arbitration circuit further comprising first gate means (303, 308, 309), operatively connected to each of said enabling means (301, 302, 304), for combining transmitted request signals to generate a combined request signal (G);

c) a plurality of first latch means (305, 306), each of said first latch means having a sequential priority order and operatively connected to a corresponding enabling means (301, 302), and further connected to the output of said first gate means (303, 308), each of said first latch means for generating an enable signal and a disable signal;

d) a plurality of second gate means (311, 312), each of said second gate means operatively connected to said first gate means (303, 308, 309) to receive said combined request signal (G), and each of said second gate means operatively connected to the corresponding first latch means (305, 306) to receive said enabling signal, and further each of said second gate means operatively connected to each first latch means having a higher sequential priority to receive said disabling signal from each of said higher sequential priority first latch means, each of said second gate means for generating a select control signal corresponding to the request signal selected by the arbitration circuit thereby permitting that requestor access to the bus;

e) a plurality of second latch means (322, 324) operatively connected to a corresponding said second gate means (311, 312) for maintaining said first denoting signals (PHASE 2) to provide for interfacing control information with the common bus including address and read/write, set-up and hold; and

f) a plurality of third latch means (323, 325) operatively connected to a corresponding said second gate means (311, 312) for maintaining said second denoting signals (PHASE 3) to provide a cycle in process indication.

2. An arbitration circuit according to claim 1, characterized in that each of said second latch means (322, 324) having an output terminal adapted to transmit said select control signal whereby permitting the requestor to communicate with said bus, and further each of said second latch means operatively connected to said bus controller to receive a time-out signal (Ts), whereupon said select control signal is removed.

3. An arbitration circuit according to claim 2, characterized in that each of said third latch means (323, 325) is operatively connected to a corresponding requestor, and further, each of said third latch means having a terminal adapted to receive a cycle-complete signal (CCA, CCB) thereby removing said cycle control signal upon completion of post bus cycle activity.

4. An arbitration circuit according to claim 3, characterized by:

driver means (310), operatively connected to said first gate means (303, 308, 309), for transmitting said combined request signal (G) to the bus controller to indicate the start of the access.

5. An arbitration circuit according to claim 4, further characterized by:

fourth latch means (321), operatively connected to said driver means (310), for maintaining said combined request signal.

6. An arbitration circuit according to claim 5, further characterized in that said first gate means comprises:

a) OR-gate means (303), operatively connected to each of said plurality of enabling means (301, 302), for combining transmitted request signals to generate a combined request signal;

b) first delay means (308), operatively connected to said OR-gate means (303), for delaying the transmission of said combined request signal a predetermined time; and

c) second delay means (309), operatively connected to said first delay means (308), for delaying the transmission of said combined request signal a predetermined time.

Patentansprüche

1. Arbiterschaltkreis (30) zur Festlegung, welches der Anforderungssignale mehrerer Anforderer (11, 12) zu bestätigen ist und Zugriff zu einem gemeinsamen Bus (35, 36, 37) mit einer zugeordneten Bussteuerung zu gewähren ist, wobei der Arbiterschaltkreis umfaßt:

a) eine Freigabeeinrichtung (301, 302, 304) für jeden Anforderer (11, 12) zum Empfang:

i) des Anforderungssignales (RQIO, RQCPU) des Anforderers (11, 12), dadurch gekennzeichnet, daß die Freigabeeinrichtung ferner empfängt:

ii) erste Signale (PHASE2), die die Zugriffsgewährung irgendeines der anderen Anforderer zu dem gemeinsamen Bus (35, 36, 37) anzeigen, und

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mission of the request.

Claims

1. An arbitration circuit (30), for determining which one of a plurality of request signals from a plurality of requestors (11, 12) is to be acknowledged and granted access to a common bus (35, 36, 37) having an associated bus controller, said arbitration circuit comprising

a) an enabling means (301, 302, 304) for each requestor (11, 12) for receiving:

i) the request signal (RQIO, RQCPU) of said requestor (11, 12),

characterised in that said enabling means further receives

ii) first signals (PHASE 2) denoting the granting to any one of the other requestors of access to the common bus (35, 36, 37), and

iii) second signals (PHASE 3) denoting that said requestor has been granted access to the common bus (35, 36, 37) and is engaged in completing the operation of communicating with the common bus,

with said enabling means (301, 302, 304) transmitting said request signal (RQIO, RQCPU) of said requestor (11, 12) only if none of said denoting signals (PHASE 2, PHASE 3) are present;

b) said arbitration circuit further comprising first gate means (303, 308, 309), operatively connected to each of said enabling means (301, 302, 304), for combining transmitted request signals to generate a combined request signal (G);

c) a plurality of first latch means (305, 306), each of said first latch means having a sequential priority order and operatively connected to a corresponding enabling means (301, 302), and further connected to the output of said first gate means (303, 308), each of said first latch means for generating an enable signal and a disable signal;

d) a plurality of second gate means (311, 312), each of said second gate means operatively connected to said first gate means (303, 308, 309) to receive said combined request signal (G), and each of said second gate means operatively connected to the corresponding first latch means (305, 306) to receive said enabling signal, and further each of said second gate means operatively connected to each first latch means having a higher sequential priority to receive said disabling signal from each of said higher sequential priority first latch means, each of said second gate means for generating a select control signal corresponding to the request signal selected by the arbitration circuit thereby permitting that requestor access to the bus;

e) a plurality of second latch means (322, 324) operatively connected to a corresponding said second gate means (311, 312) for maintaining said first denoting signals (PHASE 2) to provide for interfacing control information with the common bus including address and read/write, set-up and hold; and

f) a plurality of third latch means (323, 325) operatively connected to a corresponding said second gate means (311, 312) for maintaining said second denoting signals (PHASE 3) to provide a cycle in process indication.

2. An arbitration circuit according to claim 1, characterized in that each of said second latch means (322, 324) having an output terminal adapted to transmit said select control signal whereby permitting the requestor to communicate with said bus, and further each of said second latch means operatively connected to said bus controller to receive a time-out signal (Ts), whereupon said select control signal is removed.

3. An arbitration circuit according to claim 2, characterized in that each of said third latch means (323, 325) is operatively connected to a corresponding requestor, and further, each of said third latch means having a terminal adapted to receive a cycle-complete signal (CCA, CCB) thereby removing said cycle control signal upon completion of post bus cycle activity.

4. An arbitration circuit according to claim 3, characterized by:
driver means (310), operatively connected to said first gate means (303, 308, 309), for transmitting said combined request signal (G) to the bus controller to indicate the start of the access.

5. An arbitration circuit according to claim 4, further characterized by:
fourth latch means (321), operatively connected to said driver means (310), for maintaining said combined request signal.

6. An arbitration circuit according to claim 5, further characterized in that said first gate means comprises:

a) OR-gate means (303), operatively connected to each of said plurality of enabling means (301, 302), for combining transmitted request signals to generate a combined request signal;

b) first delay means (308), operatively connected to said OR-gate means (303), for delaying the transmission of said combined request signal a predetermined time; and

c) second delay means (309), operatively connected to said first delay means (308), for delaying the transmission of said combined request signal a predetermined time.

Patentansprüche

1. Arbiterschaltkreis (30) zur Festlegung, welches der Anforderungssignale mehrerer Anforderer (11, 12) zu bestätigen ist und Zugriff zu einem gemeinsamen Bus (35, 36, 37) mit einer zugeordneten Bussteuerung zu gewähren ist, wobei der Arbiterschaltkreis umfaßt:

a) eine Freigabeeinrichtung (301, 302, 304) für jeden Anforderer (11, 12) zum Empfang:

i) des Anforderungssignales (RQIO, RQCPU) des Anforderers (11, 12), dadurch gekennzeichnet, daß die Freigabeeinrichtung ferner empfängt:

ii) erste Signale (PHASE2), die die Zugriffsgewährung irgendeines der anderen Anforderer zu dem gemeinsamen Bus (35, 36, 37) anzeigen, und

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iii) zweite Signale (PHASE3), die anzeigen, daß dem Anforderer Zugriff zu dem gemeinsamen Bus (35, 36, 37) gewährt worden ist und daß dieser mit der Vervollständigung des Dialogs mit dem gemeinsamen Bus beschäftigt ist,

wobei die Freigabeeinrichtung (301, 302, 304) das Anforderungssignal (RQIO, RQCPU) des Anforderers (11, 12) nur überträgt, wenn keines der Anzeigesignale (PHASE2, PHASE3) vorliegt; wobei der Arbiterschaltkreis ferner umfaßt;

b) eine erste Gattereinrichtung (303, 308, 309), die an die Freigabeeinrichtung (301, 302, 304) angeschlossen ist, um die übertragenen Anforderungssignale zu kombinieren und ein kombiniertes Anforderungssignal (G) zu erzeugen;

c) mehrere erste Verriegelungen (305, 306), wobei jede erste Verriegelung eine sequentiell gestaffelte Priorität aufweist, operativ an eine entsprechende Freigabeeinrichtung (301, 302) angeschlossen ist und ferner mit dem Ausgang der ersten Gattereinrichtung (303, 308) verbunden ist, um ein Freigabe- und ein Sperrsignal zu erzeugen;

d) mehrere zweite Gatter (311, 312), wobei jedes zweite Gatter operativ mit der ersten Gattereinrichtung (303, 308, 309) verbunden ist, um das kombinierte Anforderungssignal (G) zu empfangen und operativ mit den ersten Verriegelungen (305, 306) verbunden ist, um das Freigabesignal zu empfangen und ferner mit jeder ersten Verriegelung verbunden ist, die eine höhere sequentiell gestaffelte Priorität aufweist, um das Sperrsignal zu empfangen, wobei jedes zweite Gatter ein Auswahl-Steuersignal entsprechend dem Anforderungssignal erzeugt, das durch den Arbiterschaltkreis ausgewählt worden ist, wodurch dem Anforderer Zugriff zu dem Bus gewährt wird;

e) mehrere zweite Verriegelungen (322, 324), die operativ mit einem entsprechenden zweiten Gatter (311, 312) verbunden sind, um die ersten Anzeigesignale (PHASE2) zu speichern und eine Schnittstellen-Steuerinformation mit dem gemeinsamen Bus vorzugeben, die die Adresse, einen Lese/Schreibbefehl, den Verbindungsaufbau und das Speichern umfaßt; und

f) mehrere dritte Verriegelungen (323, 325), die operativ mit den zweiten Gattern (311, 312) verbunden sind, um die zweiten Anzeigesignale (PHASE3) zu speichern und einen Bearbeitungszyklus anzuzeigen.

2. Arbiterschaltkreis nach Anspruch 1, dadurch gekennzeichnet, daß jede zweite Verriegelung (322, 324) einen Ausgangsanschluß zur Abgabe des Auswahl-Steuersignales aufweist, wodurch dem Anforderer ein Dialog mit dem Bus gewährt wird, und daß jede zweite Verriegelung operativ mit der Bussteuerung verbunden ist, um ein Zeitablaufsignal (Ts) zu empfangen, worauf das Auswahl-Steuersignal entfernt wird.

3. Arbiterschaltkreis nach Anspruch 2, dadurch gekennzeichnet, daß jede dritte Verriegelung (323, 325) operativ mit einem entsprechenden Anforderer verbunden ist und ferner jede dritte Verriegelung einen Anschluß aufweist, durch ein Zyklus-Vervollständigungssignal (CCA, CCP) zugeführt wird, wodurch das Zyklus-Steuersignal nach Beendigung der Buszyklus-Aktivität entfernt wird.

4. Arbiterschaltkreis nach Anspruch 3, gekennzeichnet durch einen operativ mit der ersten Gattereinrichtung (303, 308, 309) verbundenen Treiber (310) für die Übertragung des kombinierten Anforderungssignales (G) zu der Bussteuerung, um den Beginn des Zugriffs anzuzeigen.

5. Arbiterschaltkreis nach Anspruch 4, ferner gekennzeichnet durch eine vierte Verriegelung (321), die operativ an den Treiber (310) angeschlossen ist, um das kombinierte Anforderungssignal aufrechtzuerhalten.

6. Arbiterschaltkreis nach Anspruch 5, ferner dadurch gekennzeichnet, daß die erste Gattereinrichtung umfaßt:

a) ein ODER-Gatter (303), das operativ an jede der Freigabeeinrichtungen (301, 302) angeschlossen ist, um die übertragenen Anforderungssignale zu kombinieren und ein kombiniertes Anforderungssignal zu erzeugen;

b) eine erste Verzögerungseinrichtung (308), die operativ an das ODER-Gatter (303) angeschlossen ist, um die Übertragung des kombinierten Anforderungssignales um eine vorbestimmte Zeit zu verzögern; und

c) eine zweite Verzögerungseinrichtung (309), die operativ an die erste Verzögerungseinrichtung (308) angeschlossen ist, um die Übertragung des kombinierten Anforderungssignales um eine vorbestimmte Zeit zu verzögern.

Revendications

1. Circuit d'arbitrage (30), pour déterminer pour lequel parmi une pluralité de signaux d'interrogation émanant d'une pluralité de circuits interrogateurs (11, 12) doit se voir accuser réception et autoriser l'accès à un bus commun (35, 36, 37) ayant un contrôleur de bus associé, ce circuit d'arbitrage comprenant :

a) des moyens d'habilitation (301, 302, 304) pour chaque circuit interrogateur (11, 12) en vue de recevoir :

i) le signal d'interrogation (RQIO, RQCPU) de ce circuit interrogateur (11, 12), caractérisé en ce que lesdits moyens d'habilitation reçoivent en outre :

ii) des premiers signaux (PHASE 2) indicatifs de l'autorisation d'accès, pour tout autre circuit interrogateur, au bus commun (35, 36, 37) ; et

iii) des seconds signaux (PHASE 3) indiquant que ledit circuit interrogateur a été autorisé à accéder au bus commun (35, 36, 37) et est en voie d'achèvement de l'opération de communication avec le bus commun ;

lesdits moyens d'habilitation (301, 302, 304) transmettant le signal d'interrogation (RQIO, RQCPU) du circuit interrogateur (11, 12) seulement si aucun desdits signaux d'indication (PHASE 2, PHASE 3) n'est présent ;

b) ledit circuit d'arbitrage comprenant en outre des premiers moyens formant porte (303, 308, 309) raccordés de manière active à chacun des-

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dits moyens d'habilitation (301, 302, 304) pour combiner lesdits signaux d'interrogation transmis en vue de générer un signal d'interrogation combinée (G) ;

c) une pluralité de premiers moyens formant circuit de verrouillage (305, 306), chacun desdits premiers moyens formant circuit de verrouillage ayant un ordre de priorité séquentiel et étant raccordé de manière active à des moyens d'habilitation correspondants (301, 302), et en outre raccordé à la sortie desdits premiers moyens formant porte (303, 308), chacun desdits premiers moyens formant circuit de verrouillage étant conçu pour générer un circuit d'habilitation et un circuit de mise hors service ;

d) une pluralité de seconds moyens formant porte (311, 312), chacun desdits seconds moyens formant porte étant raccordé de manière active auxdits premiers moyens formant porte (303, 308, 309) en vue de recevoir ledit signal d'interrogation combinée (G), et chacun desdits seconds moyens formant porte étant raccordé de manière active à des premiers moyens correspondants formant circuit de verrouillage (305, 306) en vue de recevoir ledit signal d'habilitation, et en outre, chacun desdits seconds moyens formant porte étant raccordé de manière active à chacun desdits premiers moyens formant circuit de verrouillage ayant une priorité séquentielle supérieure en vue de recevoir ledit signal de mise hors service émanant de chacun desdits premiers moyens formant circuit de verrouillage à priorité séquentielle supérieure, chacun desdits seconds moyens formant porte étant conçu pour générer un signal de commande de sélection correspondant au signal d'interrogation choisi par le circuit d'arbitrage de manière à permettre l'accès du circuit interrogateur au bus ;

e) une pluralité de seconds moyens formant circuit de verrouillage (322, 324) raccordés de manière active auxdits seconds moyens correspondants formant porte (311, 312) en vue de maintenir lesdits premiers signaux d'indication (PHASE 2) pour délivrer une information de commande d'interfaçage avec le bus commun comprenant des adresse, lecture-écriture, réglage et maintien ; et

f) une pluralité de troisièmes moyens formant circuit de verrouillage (323, 325) raccordés de manière active auxdits seconds moyens correspondants formant porte (311, 312) en vue de maintenir lesdits seconds signaux d'indication (PHASE 3) pour fournir un cycle d'indication de procédé.

2. Circuit d'arbitrage selon la revendication 1, caractérisé en ce que chacun desdits seconds moyens formant circuit de verrouillage (322, 324) présente une borne de sortie adaptée à transmettre ledit signal de commande choisi de manière à autoriser le circuit interrogateur à communiquer avec ledit bus, et en outre, en ce que chacun desdits seconds moyens formant porte de verrouillage est raccordé de manière active audit contrôleur de bus en vue de recevoir un signal de temporisation (T_S), de sorte que ce signal de commande de sélection est retiré.

3. Circuit d'arbitrage selon la revendication 2, caractérisé en ce que chacun des troisièmes moyen formant circuit de verrouillage (323, 325) est raccordé de manière active à un circuit interrogateu correspondant, et chacun des troisièmes moyen formant circuit de verrouillage comportant en outr une borne adaptée à recevoir un signal d'exécutio de cycle (CCA, CCB) de manière à retirer ledit si gnal de commande de cycle au moment de l'exécutio de l'activité de cycle après-bus.

4. Circuit d'arbitrage selon la revendication 3, caractérisé par :

- des moyens de mise en conduction (310) raccordés de manière active auxdits premiers moyens formant porte (303, 308, 309), pour transmettre ledit signal d'interrogation combinée (G) au contrôleur de bus en vue d'indiquer le début de l'accès.

5. Circuit d'arbitrage selon la revendication 4, caractérisé en outre par :

- les quatrièmes moyens formant circuit de verrouillage (321) raccordés de manière active auxdits moyens de mise en conduction (310) pour maintenir le signal d'interrogation combinée.

6. Circuit d'arbitrage selon la revendication 5, caractérisé en outre en ce que les premiers moyens formant porte comprennent :

a) des moyens formant porte OU (303), raccordés de manière active à chacun desdits moyens d'habilitation (301, 302) pour combiner lesdits signaux d'interrogation transmis en vue de générer un signal d'interrogation combinée ;

b) des premiers moyens de retard (308), raccordés de manière active auxdits moyens formant porte OU (303), pour retarder la transmission du signal d'interrogation combinée d'une durée prédéterminée ; et

c) des seconds moyens de retard (309), raccordés de manière active auxdits premiers moyens de retard (308) pour retarder la transmission du signal d'interrogation combinée d'une durée prédéterminée.

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