The invention relates to a serial data interface in accordance with the first part of claim 1.

A serial data interface serves to connect peripheral circuits, which transmit or receive data over a data bus, in a properly transmissive manner to the data bus. A data transmission using a bidirectional data bus is described in the DE-OS 34 04 721. For the realisation of the shortest possible transmission times of the data over the data bus, the data words are selected to be only so long as is necessary for the length of the data which is to be transmitted. The serial data interface has to evaluate the data stream flowing through the data bus for features which permit the association with the connected peripheral circuit to be recognised.

The object of the invention is to construct a serial data interface such that, the length of the data words pertinent to the connected peripheral circuit, as well as an address possibly contained in the data word, can be quickly and precisely recognised and the data words intended for the peripheral circuit can be immediately conveyed to the latter.

In a serial data interface in accordance with the first part of claim 1, this object is achieved by the features given in the characterising part.

The serial data interface in accordance with the invention is particularly suitable for the connection of a peripheral circuit to a data bus which corresponds to the Thomson specification. Herein, just the length of the data words is utilised for the association. If this criteria is not sufficient because a plurality of peripheral circuits receive data words of equal length, an address inserted into the data word can be additionally evaluated.

The evaluation of the data words occurs during a reading cycle. This reading cycle is defined by a certain logical state of the enable lead. The number of the clock pulses transmitted over a clock pulse lead during the reading cycle corresponds to the length of the data word. A bit of the data occurring on the data lead is written into a data store at each clock pulse. The length of the data word is checked by means of a comparison circuit arranged at the output of the data store. A down stream control circuit suppresses the transfer of the stored data to the peripheral circuit upon the occurrence of deviations of the length of the data word from the length assigned to the peripheral circuit. For a correct length of the data word, either a transfer command is generated or, in the event that

data words of the determined length are ambiguously allocatable, a further check of the address bits contained in the data word is carried out. In the event of an appropriate address, a transfer command is generated which causes a transmission of the data intermediately stored in the data store to the peripheral circuit. The transfer is otherwise suppressed.

By means of a combined evaluation of the state of the enable lead and of the clock pulses on the clock pulse lead, the comparison circuit and the control circuit are set into a defined standby state at the beginning of a data transmission of the data store, from which (state) a complete new checking of the transmitted data words is always possible. By switching over the enable lead into a writing state, the serial interface can be switched over for the outputting of data onto the data bus whereby here, a simultaneous pre-setting to a certain length, of the data to be emitted onto the data bus, is possible.

Further developments and advantageous embodiments of the invention are apparent from the claims, the further description and the drawing which shows an embodiment of the invention.

The drawing shows in detail, in

Fig. 1 the block circuit diagram of a serial data interface in accordance with the invention,

Fig. 2 the complete circuit of a serial data interface for a data word length of 24 bits,

Fig. 3 a set/reset circuit including a clock pulse generator as a section from Fig. 2,

Fig. 4 a signal diagram of the circuit illustrated in Fig. 3,

Fig. 5 a data store as a section from Fig. 2,

Fig. 6 a comparison circuit as a section from Fig. 2,

Fig. 7 a timing diagram of the circuit illustrated in Fig. 6,

Fig. 8 a control circuit as a section from Fig. 2,

Fig. 9 a timing diagram of the control circuit illustrated in Fig. 8 and

Fig. 10 a flow diagram of the circuit illustrated in Fig. 8.

Fig. 1 shows a block circuit diagram of the serial data interface 1. This establishes a connection between a peripheral circuit 2 and a data bus 3. The serial data interface 1 comprises a data store 4, a comparison circuit 5, a control circuit 6, a set/reset circuit 7 and an internal clock pulse generator 8. The data bus 3 comprises three leads, a data lead 9, an enable lead 10 and a clock pulse lead 11. In addition, a reset lead 12 is provided.

A parallel data output 13, a serial data input and output 14, an address output 15, a counter output 16 and control outputs 17 - 19 serve for the connection to the peripheral circuit.

The complete circuit of the serial data interface 1 follows from Fig. 2. Therein, the circuit components which are associable with the blocks illustrated in Fig. 1, are provided with a dashed framing and carry the same reference numbers. The conductors and outputs already illustrated in Fig. 1 are also provided with the same reference numbers.

In the circuit illustrated in Fig. 2, an input of the data store 4 is connected to the data lead 9. The comparison circuit 5 is arranged at the output of the data store 4 and, in turn, the control circuit 6 is connected downstream of the former. Inputs of the internal set/reset circuit 7 are connected to the enable lead 10 and the clock pulse lead 11. Outputs of the set/reset circuit 7 lead to set and reset inputs of the data store 4, the comparison circuit 5 and the control circuit 6. Inputs of the clock pulse generator 8 are connected to the enable lead 10 and the clock pulse lead 11 and outputs of the clock pulse generator 8 lead to clock inputs of the data store 4, the comparison circuit 5 and the control circuit 6. For the explanation of the individual component groups and the complete operation of the serial data interface, reference is made to the following Figures.

Fig. 3 shows the set/reset circuit 7 and the internal clock pulse generator 8. As follows from the timing diagram of Fig. 4, a switching of a flip-flop 20 of the set/reset circuit 7 into a defined state initially occurs due to an external reset signal EXTRES. Set and reset commands PRESET, RESET to the further circuit components of the serial data interface resulting therefrom are generated by combination of the enable signals ENABLE and clock pulse signals CLOCK. As can be gathered from the timing diagram, a change of state during a first clock pulse is produced from the set and reset signals PRESET, RESET. The states do not change any more during the succeeding clock pulses. Even during the writing cycle, which is entered into by

switching over the state of the enable signal, there is no renewed alteration of the set and reset signals. In combination with the signal ENABLE occurring on the enable lead and the clock pulse signal CLOCK occurring on the clock pulse lead, the clock pulse generator 8 generates an internal clock pulse CNTCLK. This occurs by combining the two signals ENABLE, CLOCK through a logical EX-OR combination by means of the gate 21. The internal clock pulse CNTCLK in the writing cycle is thereby inverted relative to the reading cycle.

The data store 4 is illustrated in Fig. 5. This is constructed as a shift register having storage cells 25 wherein the number n of the storage cells 25 corresponds to the number of the bits in the data word which are associated with the peripheral circuit 2. The whole data word can either consist exclusively of these data bits or of the data bits and the address bits in the event that address bits are also required. The data lead 9, which carries signals referenced DATA, is connected to a serial input 22 of the data store and the data DATAOUT are derivable at a parallel data output 13. Clock pulse signals CNTCLK are supplied via a clock pulse input 23 whereby a bit occurring at the data input 22 is switched on one storage cell 25 further by each clock pulse. Set/reset signals RESET, with which the individual storage cells 25 can be placed in a defined starting state, can be supplied over a set/reset input 24. The output of the first storage cell 25 is thereby set to the state logical 1 and the remaining storage cells 25 to the state logical 0.

As soon as a data stream is written into the data store 4, the bit formed by the setting of the first storage cell 25 moves through the data store 4 as the leading bit in front of the other bits of the data word. For the case of a correct or too great a length of the data word, this leading bit later appears as the first bit in the comparison circuit 5 and, as BIT 24, enables an evaluation as to whether the data word possesses the correct length for the association with the peripheral circuit 2. During the outputting of the data, the shift register of the data store 4 also serves for the conversion of the serially written-in data word into a data word that is read-out in parallel. In the writing cycle, i.e. during the outputting of the data from the peripheral circuit 2 to the data bus 3, the data is read-out serially.

The comparison circuit 5 is illustrated in Fig. 6. The comparison circuit comprises a shift register consisting of storage cells 26 into which the data written into the data store 4 are transmitted as data (N). If the data word does not contain any bits for an address associated with a circuit of the

peripheral circuit 2, then a single storage cell 26 of the shift register would be sufficient for checking the bit set in the first storage cell 25 of the data store 4. If, on the other hand, further address bits are present, then m further storage cells 26 are needed in correspondence with the number m of the address bits m. If, as is provided for in the embodiment, four address bits are placed in front of the data bits of the data word, then three further storage cells 26 are thus required in the shift register of the comparison circuit 5.

A timing diagram of the comparison circuit 5 is illustrated in Fig. 7. With the aid of this diagram, one can see that at the beginning of a reading cycle, in which data from the data bus 3 is written into the data store 4 and passed from there into the comparison circuit as DATA (N), the state of the enable signal ENABLE is at logical 1. It is assumed that with a data word length of 24 bits for which the circuit is laid out, a data word of equal length is transmitted over the data bus 3. In the diagram, the last of the 24 clock pulses are illustrated by means of which this data word is written into the storage cells 26 of the comparison circuit 5. With the twenty-fourth clock pulse CNTCLK, the leading bit placed in front as BIT 24 appears at the output of the last storage cell 26 whilst the three storage cells 26 arranged in front of it contain the address bits. The correspondence between the data word address and the address of the peripheral circuit 2 is now checked by means of a comparison logic 27. To this end, the data word address is applied to inputs of the comparison logic 27 via the outputs of the storage cells 26 and, via outputs of the module giving the address of the peripheral circuit 2, its address as IC-ADRESSE. If there is correspondence, the output of the comparison logic 27 emits a recognition signal CAV at the same time, at which the leading bit appears as BIT 24 at the output of the last storage cell 26.

The circuit illustrated has yet a further function for the writing cycle, into which it is switched over by a change of the logical state of the enable signal ENABLE. The circuit is reset by a transfer signal LATCH coming from the control circuit 6 and simultaneously, a signal WRITE coming from the control circuit 6 blocks the data stream from the data store 4 and connects up the shift register formed from the storage cells 26 as a counter. Upon reaching a specific counting state, a signal AVN is then transmitted to the control circuit 6. This state, after the switch over into the writing cycle and the occurrence of clock pulses from a total number of 16 clock pulses, is illustrated in the timing diagram in accordance with Fig. 7.

The control circuit 6 is illustrated in Fig. 8. The control circuit 6 also comprises a plurality of storage cells 28 which form a shift register wherein the storage cells 28 are connected via combinatorial logic element 29, 30, 31. The first storage cell 28 is set to the state logical 1 by an internal setting signal PRESET. In the case that the number of the bits in the data word does not correspond to the prescribed length, i.e. the enable signal ENABLE changes its state to logical 1 before or after the leading bit, there is no onward transfer of the output state Q1 of the first storage cell 28 to the second storage cell 28. If, on the other hand, the number of bits corresponds, then it still depends on the state of the CAV signal as to whether the combinatorial logic element 30 will enable the transfer of the state of the first storage cell 28 into the second storage cell 28. This is the case in the state logical 1 of the CAV signal so that the output Q2 goes to logical 1 as follows from Fig. 9, and, after a change of the enable signal ENABLE from logical 0 to logical 1, the transfer signal LATCH is emitted. Amongst other things, this serves for the transfer of the data stored in the data store 4 into the peripheral circuit 2. Furthermore, during the occurrence of this state, the third storage cell 28 is set by a further clock pulse and a signal WRITE appears at the output of this storage cell 28. As already explained in connection with Figs. 6 and 7, this sets the comparison circuit 5 into a counter mode. After the ending of the writing cycle, which is notified as AVN signal by the comparison circuit 5 acting as a counter, the control circuit 6 returns into a standby mode. The writing cycle may also be interrupted earlier if the state of the enable signal ENABLE is altered and the circuit is switched over into a reading cycle. In this case too, the storage cells 28 of the control circuit 6 are returned to the defined starting state as mentioned hereinabove.

The described processes for the control circuit 6 are additionally illustrated as a flow diagram in Fig. 10.

Claims

1. Serial data interface (1) for the connection of a known data bus (3) to a peripheral circuit (2), wherein a plurality of peripheral circuits are connected to a corresponding plurality of data interfaces and the data bus includes a data lead (9), an enable lead (10) and a clock pulse lead (11), characterised by:

- a data store (4) connected to the data lead for the successive storage of data words of equal or different word lengths transmitted over the data lead;

- a comparison circuit (5), which detects addresses for peripheral circuits that are possibly present in the data words and compares them with the address of the currently connected peripheral circuit, connected to the data store;

- a control circuit, which compares the word lengths of the data words with a predefined word length and then, taking into account the signals transmitted on the enable lead, only allows a further transfer of the data words to the connected peripheral circuit if the two word lengths are equal, connected to the comparison circuit;

- an internal clock pulse generator (8), which supplies the data store (4), the comparison circuit (5) and the control circuit (6) with clock pulse signals, connected to the enable lead and to the clock pulse lead;

- an internal set/reset circuit (7) connected to the enable lead and to the clock pulse lead, whose outputs are connected to set and/or reset inputs of the data store (4), the comparison circuit (5) and the control circuit (6) and emits to these outputs corresponding set and/or reset commands which are generated either by an external reset signal or by means of a combination of signals transmitted on the enable lead and on the clock pulse lead.

2. Data interface in accordance with Claim 1, characterised in that, the data store (4) comprises a shift register having n storage cells (25) wherein the number n corresponds to the number of the bits of the data word associated with the peripheral circuit (2).

* C L M S *

3. Data interface in accordance with Claim 2, characterised in that, the data store (4) can be placed by the set/reset circuit (7) into a state in which the first storage cell (25) as seen from the input is a logical 1 and the remaining storage cells (25) are logical 0 or vice versa.

4. Data interface in accordance with Claim 2 or 3, characterised in that, the last storage cells of the data store (4) as seen from the input are components of the comparison circuit (5), wherein the comparison circuit (5) also comprises a comparison logic (27) to which the outputs of the last storage cells on the one hand and outputs of a module containing the address of the peripheral circuit (2) on the other hand are connected.

5. Data interface in accordance with any of the Claims 2 to 4, characterised in that, the control circuit (7) is formed as a shift register having a plurality of storage cells (28), wherein the storage cells (28) are connected to each other via logical combinatorial elements (29, 30, 31), that outputs of the comparison circuit (5) and of the set/reset circuit (7) are connected to the inputs of the combinatorial logic elements (29, 30, 31) and that a store transfer signal LATCH and a write/read signal WRITE are derivable at outputs of the control circuit (6).

6. Data interface in accordance with Claim 5, characterised in that, the control circuit (6) is settable by the set/reset circuit (7) into a state in which the first storage cell (28) as seen from the input is a logical 1 and the remaining storage cells (28) are logical 0 or vice versa.

7. Data interface in accordance with Claim 5 or 6, characterised in that, the output carrying the write/read signal WRITE of the control circuit (6) is connected to a control logic (29) of the comparison circuit (5) by means of which the storage cells (26) of the comparison circuit (5) in the writing mode can be connected up as a counter and that a counter output is connected to one of the combinatorial logic elements (29) between the storage cells (28) of the control circuit (6).

* C L M S *