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(54) Title: SLOPED EPITAXY BURIED CONTACT

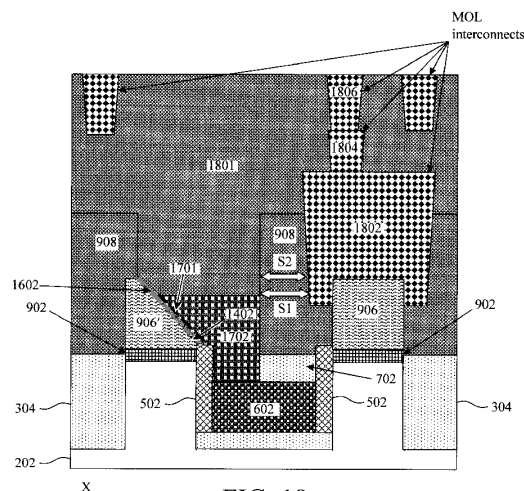


FIG. 18

(57) Abstract: Semiconductor device designs having a buried power rail (602) with a sloped epitaxy buried contact (1702) are provided. In one aspect, a semiconductor FET device includes: at least one gate disposed on a substrate (202); source and drains (906) on opposite sides of the at least one gate, wherein at least one of the source and drains (906) has a sloped surface (1402); a buried power rail (602) embedded in the substrate (202); and a buried contact (1702) that connects the buried power rail (602) to the sloped surface (1402) of the at least one source and drain (906). Sidewall spacers (502) separate the buried power rail (602) from the substrate (202). A top of the sloped surface (1402) of the at least one source and drain (906) is above a top surface of the buried contact (1702). Methods of forming a semiconductor FET device are also provided.

[Continued on next page]

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