

Chip Module and Method of Forming Same

Field of the Invention

This invention relates to a chip module, such as an integrated-circuit (IC) chip module, a
5 chip module card inlay with such a chip module, a method of forming such a chip module, and a
method of forming such a chip module card inlay.

Background of the Invention

Chip module card inlays are frequently used for the production of smart cards, e.g.
10 credit cards, identity cards, etc. Such cards are used frequently, and may be subjected to
warping and bending when carried around by the users or in use. Such warping and bending
of the cards may adversely affect the structural integrity and proper functioning of the cards.
Furthermore, conventional chip modules in the smart card industry do not provide a flat and
uniform top surface, which adversely affect the manufacturing process of chip module card
15 inlays and smart cards. In particular, chip modules are conventionally of a two-level stepped
structure or formed with an uneven top housing, as in the chip on board method.

It is thus an object of the present invention to provide a chip module, a chip module
card inlay, a method of forming a chip module, and a method of forming a chip module card
20 inlay in which the aforesaid shortcoming is mitigated, or at least to provide a useful
alternative to the trade and public.

Summary of the Invention

According to a first aspect of the present invention, there is provided a chip module
25 including an integrated-circuit (IC) chip, a first substrate layer made at least partly of a flexible
material and with a first hole, a second substrate layer made at least partly of an adhesive
material and with a second hole, and a third substrate layer made at least partly of an electrically
conductive material, wherein said second substrate layer is sandwiched between and fixedly
engaged with said first substrate layer and said third substrate layer, wherein said first hole of
30 said first substrate layer and said second hole of said second substrate layer are aligned with
each other to form a first cavity, and wherein at least a first part of said IC chip is received
within said first cavity.

According to a second aspect of the present invention, there is provided a chip module card inlay including at least one chip module, said chip module including an integrated-circuit (IC) chip, a first substrate layer made at least partly of a flexible material and with a first hole, a second substrate layer made at least partly of an adhesive material and with a second hole, and a third substrate layer made at least partly of an electrically conductive material, wherein said second substrate layer is sandwiched between and fixedly engaged with said first substrate layer and said third substrate layer, wherein said first hole of said first substrate layer and said second hole of said second substrate layer are aligned with each other to form a first cavity, and wherein at least a first part of said IC chip is received within said first cavity.

According to a third aspect of the present invention, there is provided a method of forming a chip module including providing a first substrate layer made at least partly of a flexible material and with a plurality of first holes, providing a second substrate layer made at least partly of an adhesive material and with a plurality of second holes, providing a third substrate layer made at least partly of an electrically conductive material, aligning said first holes of said first substrate layer with said second holes of said second substrate layer to form a plurality of first cavities, sandwiching said second substrate layer between said first substrate layer and said third substrate layer, fixedly engaging said first substrate layer, said second substrate layer and said third substrate layer to form a first layered structure, fixedly engaging at least a first part of an integrated-circuit (IC) chip within one of said first cavities of said first layered structure, and cutting out at least one chip module from said first layered structure fixedly engaged with said IC chip.

According to a fourth aspect of the present invention, there is provided a method of forming a chip module card inlay including forming at least one chip module including providing a first substrate layer made at least partly of a flexible material and with a plurality of first holes, providing a second substrate layer made at least partly of an adhesive material and with a plurality of second holes, providing a third substrate layer made at least partly of an electrically conductive material, aligning said first holes of said first substrate layer with said second holes of said second substrate layer to form a plurality of first cavities, sandwiching said

second substrate layer between said first substrate layer and said third substrate layer, fixedly engaging said first substrate layer, said second substrate layer and said third substrate layer to form a first layered structure, fixedly engaging at least a first part of an integrated-circuit (IC) chip within one of said first cavities of said first layered structure, and cutting out at least one
5 chip module from said first layered structure fixedly engaged with said IC chip.

Brief Description of the Drawings

Embodiments of the present invention will now be described, by way of examples only, with reference to the accompanying drawings, in which:

10 Fig. 1 is a perspective view of a length of chip housing carrier formed of five substrate layers suitable for forming a chip module and a chip module card inlay according to an embodiment of the present invention;

Fig. 2 is a disassembled perspective view of the length of chip housing carrier of Fig. 1;

15 Fig. 3 is a top view of the five substrate layers forming the length of chip housing carrier of Fig. 1;

Fig. 4 is a front view of a flipped integrated-circuit (IC) chip;

Fig. 5 shows steps of forming chip modules from the length of chip housing carrier of Fig. 1 and the flipped IC chip of Fig. 4;

20 Figs. 6 to 9 shows steps of forming a chip module card inlay from the chip module formed in Fig. 5; and

Fig. 10 is a sectional view of a chip module card inlay according to an embodiment of the present invention.

Description of the Embodiments

25 Fig. 1 shows a length of chip housing carrier 10 formed of five substrate layers for forming a chip module and a chip module card inlay according to an embodiment of the present invention. The chip housing carrier 10 is elongate in shape and may be wound around itself in a reel form, and then unwound for subsequent steps for forming the chip module and chip module card inlay. Along the chip housing carrier 10 are formed a number of cavities 12.
30 The cavities 12 may be of a square, rectangular, or circular transverse cross sectional shape. As shown as an example in Fig. 1, the cavities 12 are arranged in three rows, although it

should be understood that the chip housing carrier 10 may be formed with other numbers of rows of cavities 12.

Fig. 2 is a disassembled perspective view of the length of chip housing carrier 10 shown in Fig. 1. This chip housing carrier 10 according to this embodiment is made of five substrate layers 14, 16, 18, 20, 22 stacked one on top of the other. It should be understood that, according to the present invention, the chip housing carrier 10 may be formed of a different number of substrate layers, e.g. only of the substrate layers 14, 16, 18.

The five substrate layers 14, 16, 18, 20 and 22 are shown separately in Fig. 3. The substrate layer 14 is made of copper (or other electrically conductive material(s)). Three rows of slits 24 are formed along the length of the substrate layer 14. On top of the substrate layer 14 is the substrate layer 16 with three rows of holes 26 along its length. The substrate layer 16 is made of an adhesive material. On top of the substrate layer 16 is the substrate layer 18 with three rows of holes 28 along its length. The substrate layer 18 is flexible, e.g. being made of a flexible material, such as one or more of polyimide (PI), polyethylene terephthalate (PET), and a glass-reinforced epoxy laminate material (such as "FR-4", which is a composite material composed of woven fiberglass cloth with an epoxy resin binder that is flame resistant).

On top of the substrate layer 18 is the substrate layer 20 with three rows of holes 30 along its length. The substrate layer 20 is made of an adhesive material. On top of the substrate layer 20 is the substrate layer 22 with three rows of holes 32. The substrate layer 22 is made of or electro-plated with one or more electrically conductive materials, e.g. copper and nickel.

The holes 26, 28, 30, 32 of the respective substrate layers 16, 18, 20, 22 are of the same size and shape, and are arranged such that when the substrate layers 16, 18, 20, 22 are duly assembled and stacked one on top of another, their respective holes 26, 28, 30, 32 are aligned with one another such that they collectively form a number of cavities 12 extending through the substrate layer 16 to the substrate layer 22. The substrate layer 16 are positioned under and in contact with the substrate layer 14 such that a respective slit 24 is positioned

below each cavity 12 formed by a row of the holes 26, 28, 30, 32 aligned with one another.

Fig. 4 shows an integrated-circuit (IC) chip 34. The IC chip 34 may be a contactless chip or other types of chip. In electronics manufacturing, integrated circuit (IC) packaging is the final stage of semiconductor device fabrication, in which the block of semiconductor material is encapsulated in a supporting case (also known as a “package”) that prevents physical damage and corrosion. A common plastic used for making the package is epoxy-cresol-novolac (also called “epoxy-cresol-novolac”). In the IC chip 34, two electrically conductive legs 36 are shown as extending and leading from a package 38 of the IC chip 34.

Turning to Fig. 5, such shows a length of chip housing carrier 10 with a number of cavities 12 formed by the alignment of the holes 26, 28, 30, 32 of the respective substrate layers 16, 18, 20, 22 with the substrate layer 14 forming a bottom. The substrate layers 14, 16, 18, 20, 22 are then laminated to fixedly engaged with one another to form the chip housing carrier 10, which is of a layered-structure. The IC chip 34 is positioned within one of the cavities 12 such that the IC chip 34 is fully received within the cavity 12 with the legs 36 contacting the substrate layer 14 as to establish electrical and physical connection between the legs 36 (and thus the IC chip 34) with the substrate layer 14. The depth of the cavity 12 formed by the alignment of the holes 26, 28, 30, 32 of the substrate layers 16, 18, 20, 22 is shorter than the total height h of the IC chip 34, with a part of the IC chip 34 received within the cavity formed by the holes 26, 28 and another part of the IC chip 34 received within the cavity formed by the holes 30, 32.

When the IC chip 34 is received within the cavity 12 (and with its legs 36 physically and electrically connected with the substrate layer 14), an adhesive (glue) is filled into any space within the cavity 12 not occupied by the IC chip 34, so as to enhance the fixed engagement of the IC chip 34 within the cavity 12 and with the chip housing carrier 10.

When the IC chips 34 are fixedly engaged with and received within the cavities 12 of the chip housing carrier 10, a plurality of chip modules 40a, 40b are cut out from the chip housing carrier 10, e.g. by die-cutting. Each of the chip modules 40a, 40b comprises an IC

chip 34 fixedly received within and engaged with the substrate layers 14, 16, 18, 20, 22, with the substrate layer 14 fixedly engaged with the legs 36 of the IC chip 34. The chip modules 40a, 40b differ with each other in their respective shape, in that the chip module 40a is in the shape of a generally rectangular prism, and the chip module 40b is in the shape of a generally elliptical cylinder. Generally speaking, the chip modules 40a, 40b according to the present invention may be in the shape of a prism, a cylinder, or an elliptical cylinder, more particularly, a right prism, a right cylinder, or a right elliptical cylinder, all of a relatively short thickness/height. The two opposite major surfaces of the chip module 40a (of which only one of which, 41a, is shown in Fig. 5) are planar, of the same shape and parallel with each other. Similarly, the two opposite major surfaces of the chip module 40b (of which only one of which, 41b, is shown in Fig. 5) are planar, of the same shape and parallel with each other. Thus, the chip modules 40a, 40b are not in of a two-level stepped structure or formed with an uneven top housing, as in the case of conventional chip modules.

Figs. 6 to 9 shows steps of forming a chip module card inlay, using the chip module 40a as an example.

As shown in Fig. 6, the chip module 40a is positioned within a hole 42 of a substrate layer 44, which may be made of a plastic material, such as polycarbonate (PC), polyvinyl chloride (PVC), or polyethylene terephthalate glycol (PETG). In the case of the conventional two-level stepped structured chip modules, at least two such substrate layers (also called “compensation layers”) are required, to cater for the different shapes of the two levels. On the other hand, as the chip modules according to the present invention may be in the shape of a prism, a cylinder, or an elliptical cylinder, more particularly, a right prism, a right cylinder, or a right elliptical cylinder, only one compensation layer is required. This facilitates the production of the chip module card inlays (to be discussed below) and subsequently the smart cards.

As further shown in Fig. 7, an electrically conductive wire 46 (e.g. made of copper) is embedded on a major surface 48 of the substrate layer 44. The wire 46 may be embedded on the major surface 48 of the substrate layer 44 for several rounds, e.g. to form an antenna.

Two free ends of the wire 46 are bonded with the chip module 40a, e.g. by thermo-bonding.

The substrate layer 44 is sandwiched between two protective substrate layers 50, 52. The two substrate layers 50, 52 may also be made of PC, PVC or PETG. The substrate layers 44, 50, 52 thus stacked together with one another are then laminated so as to fixedly engage the substrate layers 44, 50, 52 to form a chip module card inlay 54, which is in a layered-structure.

Fig. 10 shows a sectional view of a chip module card inlay 60 with a chip module 62. The chip module 62 has an IC chip 64 received within a cavity 66 formed of alignment of the holes 26, 28 of the respective substrate layers 16, 18. The legs 36 of the IC chip 64 are connected physically and electrically with the substrate layer 14 on top of the substrate layer 16. The substrate layer 16 is thus sandwiched between and fixedly engaged with the substrate layers 14, 18.

The chip module 62 is received within a hole 68 of an inner substrate layer 70, and is electrically connected (e.g. by bonding) to an antenna formed of an electrically conductive wire 72 (which may be made of copper). The inner substrate layer 70 is sandwiched between two outer substrate layers 74, 76. The substrate layers 70, 74, 76 are laminated and thus fixedly engaged with one another to form the chip module card inlay 60 in a layered structure. The depth of the cavity 66 formed by the alignment of the holes 26, 28 of the substrate layers 16, 18 is no shorter than the total height of the IC chip 64.

It should be understood that the above only illustrates and describes examples whereby the present invention may be carried out, and that modifications and/or alterations may be made thereto without departing from the spirit of the invention.

It should also be understood that certain features of the invention, which are, for clarity, described in the context of separate embodiments, may also be provided in combination in a single embodiment. Conversely, various features of the invention which are, for brevity, described in the context of a single embodiment, may also be provided separately or in any
5 suitable sub-combination.

CLAIMS

1. A chip module including:
 - an integrated-circuit (IC) chip,
 - a first substrate layer made at least partly of a flexible material and with a first
 - 5 hole,
 - a second substrate layer made at least partly of an adhesive material and with a
 - second hole, and
 - a third substrate layer made at least partly of an electrically conductive material,
 - wherein said second substrate layer is sandwiched between and fixedly engaged
 - 10 with said first substrate layer and said third substrate layer,
 - wherein said first hole of said first substrate layer and said second hole of said
 - second substrate layer are aligned with each other to form a first cavity, and
 - wherein at least a first part of said IC chip is received within said first cavity.
- 15 2. The chip module of Claim 1, wherein said third substrate layer is made at least partly of copper.
3. The chip module of Claim 1 or 2, wherein said third substrate layer includes at least one
- 20 slit engaged with a leg of said IC chip to electrically connect said IC chip with said third
- substrate layer.
4. The chip module of any of the preceding claims, wherein said first hole and said second
- hole are of the substantially the same size and shape.
- 25 5. The chip module of any of the preceding claims, wherein said first substrate layer is
- made of polyimide (PI), polyethylene terephthalate (PET), and/or a glass-reinforced
- epoxy laminate material.
6. The chip module of any of the preceding claims, further including a fourth substrate
- 30 layer made at least partly of an adhesive material and with a third hole and a fifth
- substrate layer with a fourth hole.
7. The chip module of Claim 6, wherein said third hole and said fourth hole are aligned

with each other to form a second cavity, and wherein at least a second part of said IC chip is received within said second cavity.

- 5 8. The chip module of Claim 7, wherein said third hole and said fourth hole are of the substantially the same size and shape.
9. The chip module of any one of Claims 6 to 8, wherein said fifth substrate layer is made of or electro-plated with an electrically conductive material.
- 10 10. The chip module of any of the preceding claims, wherein said chip module is in the shape of a prism, a cylinder, or an elliptical cylinder.
11. A chip module card inlay including at least one chip module according to any one of Claims 1 to 10.
- 15 12. The chip module card inlay of Claim 11, wherein said chip module is received within a fifth hole of a sixth substrate layer.
13. The chip module card inlay of Claim 12, wherein said sixth substrate layer is sandwiched between and fixedly engaged with a seventh substrate layer and an eighth substrate layer.
- 20 14. The chip module card inlay of any one of Claims 11 to 13, wherein said chip module is electrically connected with at least one conductive wire.
- 25 15. A method of forming a chip module including:
- providing a first substrate layer made at least partly of a flexible material and with a plurality of first holes,
- providing a second substrate layer made at least partly of an adhesive material and with a plurality of second holes,
- 30
- providing a third substrate layer made at least partly of an electrically conductive material,
- aligning said first holes of said first substrate layer with said second holes of said second substrate layer to form a plurality of first cavities,

sandwiching said second substrate layer between said first substrate layer and said third substrate layer,

fixedly engaging said first substrate layer, said second substrate layer and said third substrate layer to form a first layered structure,

5 fixedly engaging at least a first part of an integrated-circuit (IC) chip within one of said first cavities of said first layered structure, and

cutting out at least one chip module from said first layered structure fixedly engaged with said IC chip.

10 16. The method of Claim 15, wherein said third substrate layer is made at least partly of copper.

17. The method of Claim 15 or 16, including engaging a leg of said IC chip with at least one slit of said third substrate layer to electrically connect said IC chip with said third
15 substrate layer.

18. The method of any one of Claims 15 to 17, wherein said first holes and said second holes are of the substantially the same size and shape.

20 19. The method of any one of Claims 15 to 18, further including filling at least a part of a space between said first part of said IC chip and said first cavity with an adhesive.

20. The method of any one of Claims 15 to 19, wherein said first substrate layer is made of polyimide (PI), polyethylene terephthalate (PET), and/or a glass-reinforced epoxy
25 laminate material.

21. The method of any one of Claims 15 to 20, further including providing a fourth substrate layer made at least partly of an adhesive material and with a plurality of third holes and a fifth substrate layer with a plurality of fourth holes.

30 22. The method of Claim 20, further including aligning said third holes of said fourth adhesive substrate layer with said fourth holes of said fifth substrate layer to form a plurality of second cavities, and positioning at least a second part of said IC chip within

one of said second cavities.

23. The method of Claim 22, wherein said third holes and said fourth holes are of the substantially the same size and shape.
- 5
24. The method of any one of Claims 21 to 23, wherein said fifth substrate layer is made of or electro-plated with an electrically conductive material.
25. The method of any one of Claims 21 to 24, further including fixedly engaging said
10 fourth adhesive substrate layer and said fifth substrate layer with said first layered structure to form a second layered structure.
26. A method of forming a chip module card inlay including forming at least one chip module according to a method to any one of Claims 15 to 24.
- 15
27. The method of Claim 26, including positioning said chip module within a fifth hole of a sixth substrate layer.
28. The method of Claim 27, including sandwiching said sixth substrate layer between a
20 seventh substrate layer and an eighth substrate layer, and fixedly engaging said sixth substrate layer, said seventh substrate layer and said eighth substrate layer with one another.
29. The method of any one of Claims 26 to 28, including electrically connecting said chip
25 module with at least one conductive wire.