PMOS TRANSISTOR STRAIN OPTIMIZATION WITH RAISED JUNCTION REGIONS

FIELD

[0001] Circuit devices and the manufacture and structure of circuit devices.

BACKGROUND

[0002] Increased performance of circuit devices on a substrate (*e.g.*, integrated circuit (IC) transistors, resistors, capacitors, etc. on a semiconductor (*e.g.*, silicon) substrate) is usually a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to increase movement of electrons in N-type MOS device (NMOS) channels and to increase movement of positive charged holes in P-type MOS device (PMOS) channels.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Various features, aspects, and advantages will become more thoroughly apparent from the following detailed description, appended claims, and accompanying drawings in which:

[0004] **Figure 1** is a schematic cross-section view of a portion of a semiconductor substrate after forming a well, gate dielectric, and gate electrode of NMOS and PMOS devices.

[0005] **Figure 2** shows the semiconductor substrate of **Figure 1** after forming sidewall spacers and junction regions of the NMOS and PMOS devices.

[0006] **Figure 3** shows the semiconductor substrate of **Figure 1** after forming of PMOS junction region voids.

[0007] **Figure 4** shows the semiconductor substrate of **Figure 1** after depositing of silicon alloy material into the PMOS junction region voids.

[0008] **Figure 5** shows the substrate of **Figure 1** after forming of silicide layers on the diffusion regions and gate electrodes of the NMOS and PMOS devices.

[0009] **Figure 6** shows the substrate of **Figure 1** after the forming of a conformal etch stop layer over the NMOS and PMOS devices.

[0010] **Figure 7** shows the substrate of **Figure 1** after removing an etch stop layer from the PMOS device.

[0011] **Figure 8** is a flow diagram of a process for forming a CMOS structure having a PMOS device with silicon alloy material deposited in the junction regions such that the silicon alloy material is in a non-planar relationship with the surface of the substrate.

DETAILED DESCRIPTION

[0012] **Figure 1** is a schematic cross-section view of a portion of a semiconductor substrate after forming a well, gate dielectric, and gate electrode of an NMOS device and a PMOS device. Apparatus 100 (*e.g.*, such as one or more CMOS structures) includes semiconductor substrate 102, such as a silicon substrate, or epitaxial layer of a semiconductor substrate, having active areas or cell regions defined by isolation areas such as shallow trench isolation structures 110 formed in substrate or epitaxial layer 102. For example, substrate 102 may be formed or grown from single crystal silicon, and shallow trench isolation (STI) structures 110 may be formed by defining regions (through trench etching) and growing or depositing silicon dioxide (SiO_2) dielectric in the trench openings (*e.g.*, such as formed to height H as shown in **Figure 1**). In embodiments, STI structures 110 define active areas or cell regions for individual transistor devices (*e.g.*, such as NMOS and PMOS devices of a CMOS structure).

[0013] **Figure 1** also shows P-type well 105 and N-type well 115 formed in the individual active area or cell region defined by STI structures 110. For example, P-type well 105 is formed in one region of substrate 102 while N-type well 115 is formed in a second region of substrate 102. P-type well 105 is formed, such as, by introducing a dopant, such as boron (B) and/or aluminum (Al), into an area of substrate 102 designated for an N-type device. N-type well 115 is formed, such as, by introducing a dopant, such as arsenic (As), phosphorous (P), and/or antimony (Sb) in an area of substrate 102 designated for a P-type device. P-type well 105 and N-type well 115 may have work functions corresponding to the work function of an NMOS device and PMOS device, respectively, of a CMOS circuit. Practices for forming, sizes, and thicknesses (*e.g.*, depths) of STI structures 110 and wells 105 and 115 are known in the art and are, therefore, not presented further herein.

[0014] **Figure 1** shows substrate 102 after the forming a gate dielectric layer and gate electrode layer over the surface 136 of substrate 102, and subsequent patterning or removal of unwanted portions of the gate dielectric layer and/or gate electrode layer. For instance, as shown, gate dielectric 120

may be grown or deposited. An example of gate dielectric material that is typically grown by thermal techniques over substrate 102 is SiO_2. It is to be appreciated that, in addition to SiO_2, other gate dielectrics, such as carbon doped oxide (CDO), cubic boron nitride (CBN), phosphosilicate glass (PSG), silicon nitride (Si_3N_4), fluorinated silicate glass (FSG), silicon carbide (SiC) may be used to further optimize the CMOS transistor devices. For example, gate dielectric materials having a high dielectric constant may be used, if desired, for example, to increase the capacitance of the gate. Practices of forming, sizes, and thicknesses (*e.g.*, heights) of gate dielectric 120 are known in the art, and are, therefore, not described further herein.

[0015] **Figure 1** shows a structure which includes gate electrodes 130 and 132 over the surface of substrate 102, such as by deposition onto gate dielectric 120. NMOS gate electrode 130 and PMOS gate electrode 132 may each be deposited to a thickness of, for example, 150-2000 angstroms (*e.g.*, 15-200 nanometers (nm)). Accordingly, the thickness of NMOS gate electrode 130 and PMOS gate electrode 132 are each scalable and may be selected or chosen based on integration issues related to device performance. NMOS gate electrode 130 has a work function corresponding to the work function of an N-type device. PMOS gate electrode 132 has a work function corresponding to the work function of a P-type device. In embodiments, NMOS gate electrode 130 and PMOS gate electrode 132 are each silicon deposited by chemical vapor deposition (CVD) and then doped to form N-type and P-type materials, respectively, such as the doping is described above with respect to forming the N-type and P-type material of N-type well 115 and P-type well 105, respectively. For instance, NMOS gate electrode 130 may be doped at the same time that the corresponding NMOS junction regions are doped (*e.g.*, such as NMOS junction regions 203, shown in **Figure 2**), and PMOS gate electrode 132 may be doped at the same time the PMOS junction regions are doped (*e.g.*, such as PMOS junction regions 204, shown in **Figure 2**). Practices for forming, sizes (*e.g.*, area of gate dielectric 120 the gate electrodes cover) and additional thicknesses (*e.g.*, heights) of NMOS gate electrode 130 and PMOS gate electrode 132 are known in the art, and are, therefore, not presented further herein.

[0016] **Figure 1** further shows the substrate after removal of undesired portions of gate dielectric 120 and NMOS gate electrode 130 and PMOS gate electrode 132, such as by patterning a mask layer over a defined area for NMOS gate electrode 130 and PMOS gate electrode 132 and etching away the undesired exposed portions not covered by the mask. For example, undesired portions of gate dielectric 120 and one or more types of gate electrode material may be patterned to form gate dielectric 120 and NMOS gate electrode 130 over NMOS device 103, and to form gate dielectric 120 and PMOS electrode 132 over PMOS device 104, such as by patterning using conventional techniques, such as plasma etchant, sputter etchant, and/or a chlorine-based etch chemistry. Masking and/or removal of gate dielectric and gate electrodes in the NMOS and PMOS devices may be performed simultaneously or in separate patterning, masking, and/or etching operations as are well known in the art, and are, therefore, not further described herein. For instance, according to embodiments, NMOS gate electrode 130 and PMOS gate electrode 132 are polysilicon deposited by CVD and then masked and etched.

[0017] **Figure 2** shows the semiconductor substrate of **Figure 1** after forming sidewall spacers and junction regions of the NMOS and PMOS devices. **Figure 2** shows NMOS gate isolation spacers 213 and PMOS gate isolation spacers 214 that may be formed, of a suitable dielectric incorporated around NMOS gate electrode 130 and PMOS gate electrode 132, respectively, to insolate the individual electrodes of the transistor devices. For example, NMOS gate isolation spacers 213 may be formed by depositing dielectric material, similar to dielectric materials described above for gate dielectric 120, along sidewalls of gate dielectric 120 and NMOS gate electrode 130 structure shown in **Figure 1** and then patterning and etching the formed or deposited dielectric material to create NMOS gate isolation spacers 213, such as patterning and etching techniques described above for NMOS and PMOS gate electrodes 120 and 130. Similarly, PMOS gate isolation spacers 214 may be formed of a suitable dielectric material incorporated around PMOS gate electrode 132 to insulate the individual electrodes of the transistor devices. For example, PMOS gate isolation spacers 214 may be formed of a similar material and using a similar method to that described above for forming NMOS gate isolation spacers 213. It is contemplated that NMOS gate isolation spacers 213

may be the same or a different material than PMOS gate isolation spacers 214. In an embodiment NMOS gate isolation spacers 213 and PMOS gate isolation spacers 214 are SiO_2. Moreover, processes for forming shapes, sizes, and thicknesses of gate isolation spacers such as NMOS gate isolation spacers 213 and PMOS gate isolation spacers 214 are known in the art (*e.g.*, and are sometimes referred to as "sidewall spacers" or "shoulder spacers"), and, therefore, are not further presented herein.

[0018] **Figure 2** shows NMOS junction regions 203 and PMOS junction regions 204 (*e.g.*, also referred to as "source-drain regions" or "diffusion regions") that may be formed by a junction implant (*e.g.*, such as implanting with arsenic, phosphorous, and/or antimony for N-type junction regions 203 and boron and/or aluminum for P-type junction regions 204) and possibly include additionally corresponding type tip implants. Thus, NMOS junction regions 203 may be formed, such as by doping portions of P-type well 105 to form those junction regions. For example, NMOS junction regions 203 may be formed, in accordance with the characteristics of an NMOS device, such as by doping the material of P-type well 105, to form the N-type material in NMOS junction regions 203, as described above with respect to doping to form the N-type material of N-type well 115. Moreover, PMOS junction regions 204 may be formed, such as by doping portions of N-type well 115 to form those junction regions. For example, portions of N-type well 115 may be doped to form the P-type material in PMOS junction regions 204, in accordance with the characteristics of a PMOS device, such as by doping as described with respect to doping to form the P-type material of P-type well 105.

[0019] In addition, as noted above, according to embodiments, corresponding tip implants may be included in or incorporated with the junction regions. For example, NMOS junction regions 203 may also include additional N-type doping, such as implanting arsenic, phosphorous, and/or antimony into NMOS junction regions 203 adjacent to NMOS gate electrode 130 at an angle directed at the channel. Also, for example, PMOS junction regions 204 may also include additional P-type angled doping, such as implanting boron and/aluminum into PMOS junction regions 204 adjacent to PMOS gate electrode 132.

[0020] More specifically, embodiments include forming NMOS junction regions 203 by doping P-type well 105 with phosphorous, and further subsequently doping the region of P-type well 105 adjacent NMOS electrode 130 further with phosphorous to form tip implants. Also, embodiments include forming PMOS junction regions 205 by doping N-type well 115 with boron, and further subsequently doping portions of N-type well 115 adjacent to PMOS gate electrode 132 with boron to form P-type tip implants.

[0021] Portions of P-type well 105 may be doped with tip implants to form N-type material before or after formation of NMOS spacers 213, such as by doping as described above with respect to doping to form the N-type material of N-type well 115. Similarly, **Figure 2** shows PMOS tip implants 204 that may be formed, such as by doping portions of N-type well 115 to form those tip implants. For example, portions of N-type well 115 may be lightly doped to form P-type material before or after formation of PMOS spacers 214, such as by doping as described above with respect to doping to form the P-type material of P-type well 105. According to embodiments, formation of NMOS gate isolation spacers 213, PMOS gate isolation spacers 214, NMOS junction regions 203, and/or PMOS junction regions 204 may occur in any order as appropriate, such as in accordance with the characteristics of the desired device. Practices for forming, sizes, and thicknesses (*e.g.*, depths) of NMOS junction regions 203 and PMOS junction regions 204, and possibly additionally including corresponding tip implants, are known in the art and are, therefore, not presented further herein.

[0022] **Figure 3** shows the semiconductor substrate of **Figure 1** after the forming of PMOS junction region voids. **Figure 3** shows first PMOS junction region void 340 and second PMOS junction region void 360 that may be formed, by removing a portion of or all of PMOS junction regions 204, and/or portions of N-type well 115 (*e.g.*, such as portions of N-type well 115 adjacent to PMOS gate electrode 132). According to embodiments, first void 340 and second void 360 may be formed at various surface areas of surface 136 and to various dimensions (*e.g.*, such as to depth D, and width W, as shown in **Figure 3**, and extending an extent E, not shown, but perpendicular to the cross-sectional view of **Figure 3**) in N-type well 115 within the space between STI 110

and an effective width of a channel under PMOS gate electrode 132 for the device. For example, in embodiments, first void 340 and second void 360 may be formed to a depth D in the range between 50 nanometers and 200 nanometers below surface 136, and to a width W in the range of between 90 nanometers and 270 nanometers. It is to be appreciated that, in embodiments, width W may be scaled according to the gate length, such as to be between one and three times the gate length. In addition, according to embodiments, first void 340 and second void 360 may be formed to a depth in the range of between 20 nanometers and 250 nanometers below surface 136, so that deposition of a silicon alloy in first void 340 and second void 360 to a height that is non-planar with surface 136 (*e.g.*, such as a height extending above surface 136) provides a PMOS device that operates sufficiently and in accordance with characteristics of the desired PMOS and/or CMOS structure (*e.g.*, such as a desired PMOS as shown by the device on the right side of **Figure 6** or **7**, or desired CMOS, such as shown by structures 600 or 700).

[0023] For example, first PMOS junction region void 340 and second PMOS junction region void 360 may be formed simultaneously or independently by patterning, etching, and/or recess etching (*e.g.*, such as is described above for removing undesired portions of electrodes 130 and 132) to various desired sizes and depths characteristic for NMOS and PMOS devices by operations as are known in the art, and are therefore not described further herein. In addition, embodiments include wherein a surface of the substrate proximate to the first junction region (*e.g.*, such as first PMOS junction region void 340) defines a first substrate sidewall surface 342, and a surface of the substrate proximate to the second junction region (*e.g.*, such as second PMOS junction region void 360) defines a second substrate sidewall surface 362.

[0024] **Figure 4** shows the semiconductor substrate of **Figure 1** after depositing of silicon alloy material into the PMOS junction region voids (*e.g.*, such as first PMOS junction region void 340 and second PMOS junction region void 360). **Figure 4** shows silicon alloy material 470 disposed in first PMOS junction region void 340 and silicon alloy material 480 disposed in second PMOS junction region void 360 such that surface 472 of the resulting first junction region is in a non-planar relationship with surface 136 of the substrate,

and such that surface 482 of the resulting second junction region is also in a non-planar relationship with surface 136 of the substrate. Silicon alloy materials 470 and 480 may be formed of a suitable silicon alloy material disposed in first and second PMOS junction region voids 340 and 360, respectively, to cause strain 494 during performance of the device in a region of N-type well material 115 between silicon alloy material 470 and silicon alloy material 480 (*e.g.*, such as a strain in a region that may be referred to as the PMOS channel). Suitable silicon alloy materials that may be used to cause strain 494 include one or more of the following: silicon germanium (SiGe), silicon carbide (SiC), nickel silicide (NiSi), titanium silicide ($TiSi_2$), cobalt silicide ($CoSi_2$), and possibly may be doped with one or more of boron and/or aluminum. For example, silicon alloy material 470 and 480 may include a material having a silicon alloy lattice spacing that is different than the lattice spacing of the substrate material of N-type well 115. More specifically, in operation of the PMOS device, silicon alloy materials 470 and 480 may cause a compression in the well material or a compressive strain at strain 494 in a region of N-type well 115 caused by silicon alloy 470 and 480 having a lattice spacing that is a larger lattice spacing than the lattice spacing of N-type well 115 in that region.

[0025] Moreover, according to embodiments, silicon alloy materials 470 and 480 have a surface of the first junction region 472 and a surface of the second junction region 482 that are superior to the top surface (*e.g.*, surface 136) of the substrate as viewed. The non-planar relationship between the junction regions and the substrate surface tends to cause first silicon alloy strain from point 474 below substrate surface, as well as first silicon alloy strain above substrate surface 476, and second silicon alloy strain below the substrate surface 484 and second silicon alloy strain above the substrate surface 486 which any and/or all of contribute to operation strain 494. For example, the thickness of silicon alloy material 470 and/or 480 deposited (*e.g.*, the length L plus the depth D forming the height to surfaces 472 and/or 482) can be controlled by the time duration of the deposition and/or the deposition concentration, or deposition rate of the deposition operation. In addition, in embodiments, the silicon alloy material disposed or deposited in the first junction region (*e.g.*, such as silicon alloy material 470) may be attached super

adjacent to first substrate sidewall surface 342 and the silicon alloy material disposed or deposited in the second junction region (*e.g.*, such as silicon alloy material 480) may be attached super adjacent to second substrate sidewall surface 362.

[0026] Thus, according to embodiments, first void 340 and second void 360 may be formed at suitable surface areas of surface 136 and to various dimensions and depths within N-type well 115 sufficient to provide desired operational strains 474, 476, 484, 486, and/or 494; including strains desired in accordance with characteristics of a desired PMOS device and/or CMOS structure (*e.g.*, such as desired PMOS device, as shown by the device on the right side of **Figure 6** or 7, or desired CMOS structure, such as shown by structures 600 or 700). Hence, the dimensions and depth of first void 340 and second void 360, silicon alloy materials 470 and 480, and non-planar relationship of surfaces 472 and 482 with respect to surface 136 may be selected to cause a compressive strain at strain 494 in a range between 0.1 percent and 10 percent. Particularly, a proper design may be chosen to provide a compressive strain at strain 494 in the range between 0 percent and 2 percent or 0.5 percent and 2.5 percent (*e.g.*, for example, a compressive strain of approximately 1 percent). It is to be appreciated that, in embodiments, a sufficient compressive strain at strain 494 may be accomplished according to embodiments having a non planar relationship where length L is in a range between a fraction of an Angstrom and 200 nanometers.

[0027] According to embodiments, silicon alloy material 470 and/or 480 may be formed or deposited into first PMOS junction region void 340 and/or second PMOS junction region void 360, respectively, such by selective deposition, CVD deposition, or epitaxial deposition. For example, an epitaxial layer of single crystal semiconductor film may be formed upon a single crystal substrate, where the epitaxial layer has the same crystallographic characteristics as the substrate material, but differs in type or concentration of dopant. More particularly, silicon alloy materials 470 and/or 480 may be formed by selective CVD deposition, and possibly include epitaxial deposition of single crystal silicon alloy with the same crystal structure as that of the material of N-type well 115 (*e.g.*, having the same crystal structure meaning

that if the material of N-type well 115 has a crystal grade of, for example, 100, 110, etc., then the silicon alloy deposited will have a similar or the same grade crystal grade, such as, 100, 110, etc.).

[0028] Furthermore, according to embodiments, silicon alloy materials 470 and/or 480 may be formed by epitaxial deposition of boron doped silicon germanium (SiGe), then annealing to remove the boron from the silicon germanium. Therefore, a layer of $Si_{1-x}Ge_x$ may be grown on top of a substrate of Si such that the silicon germanium has a bulk relaxed lattice constant that is larger (*e.g.*, such as by 4.2 percent) than the silicon it is grown on. The resulting misfit dislocation or dislocations at the block or blocks where the silicon germanium bonds to the silicon may create strains 474, 476, 484, 486, and/or 494. In other words, strain 494, such as a compressive strain, may result from the germanium atoms squeezed into the silicon of silicon alloy materials 470 and 480 such that those silicon alloys have a lattice spacing different and distorted as compared to the silicon material of N-type well 115.

[0029] Suitable processes for forming or growing of silicon alloy materials 470 and/or 480 include by vapor phase (VPE), liquid phase (LPE), or solid phase (SPE) blocks of silicon processing. For example, one such CVD process that is applicable to VPE of silicon includes: (1) transporting reactants to the substrate surface; (2) reactants absorbed on the substrate surface; (3) chemical reaction on the surface leading to formation of a film and reaction products; (4) reaction products deabsorbed from the surface; and (5) transportation away of the reaction product from the surface.

[0030] In addition, suitable forming of silicon alloy comprises selective epitaxial deposition, formation, or growth known in the art as Type 1 selective epitaxial deposition. Using Type 1 deposition, silicon alloy deposition would be occurring only on bare silicon substrates within the openings of the oxide film, and minimal, if any, growth on the oxide. Thus, in the embodiment shown in **Figure 4**, for example, silicon alloy material 470 and/or 480 are formed on surfaces of voids 340 and/or 360 respectively (*e.g.*, including PMOS junction regions 204), but are not formed on surfaces of STI 110, gate dielectric 120, PMOS gate isolation spacers 214, or PMOS gate electrode 132. Moreover,

it is to be appreciated, that in embodiments, silicon alloy material (e.g,. such as material 470 and/or 480) may be formed on surfaces of voids 340 and/or 360, respectively, as well as on gate surfaces of STI 110, gate dielectric 120, PMOS gate isolation spacers 214 and/or PMOS gate electrode 132. Specifically, embodiments include silicon alloy material 470 and/or 480 formed by Type 1 selective epitaxial deposition using a silicon source including one or more of the following: silicon germanium (SiGe), silicon carbide (SiC), nickel silicide (NiSi), titanium silicide ($TiSi_2$), cobalt silicide ($CoSi_2$), halides, $SiCl_4$, $SiHCl_3$, $SiHBr_3$, and $SiBr_4$ at suitable temperatures. Also, SiH_2Cl_2, SiH_4 may be used as a silicon source if hydrogen chloride (HCl), chlorine (Cl_2) is present.

[0031] Suitable selective epitaxial formation also includes Type 2 selective epitaxial deposition where selectivity of deposition is non-critical. Using Type 2 deposition, formation or growth of the silicon alloy occurs on bare silicon substrate, as well as on the oxide film, and thus when this type of deposition is made, an interface between the epitaxial layer of silicon alloy formed on the bare silicon substrate and a polysilicon layer of silicon alloy formed on the oxide film is created. The angle of this interface relative to the film growth direction depends on the crystallographic orientation of the substrate. Thus, in the embodiment shown in **Figure 4**, for example, silicon alloy material 470 and/or 480 are formed on surfaces of voids 340 and/or 360, respectively (*e.g.*, including PMOS junction regions 204), and may also be formed on surfaces of STI 110, gate dielectric 120, PMOS gate isolation spacers 214, and/or PMOS gate electrode 132. Particularly, embodiments include Type 2 selective epitaxial deposition using SiH_4, SiGe, SiC, NiSi, $TiSi_2$, and/or $CoSi_2$ as the silicon source.

[0032] Consequently, according to embodiments, subsequent to formation, undesired portions of silicon alloy material 470 and/or 480 may be patterned and/or etched away using various techniques known in the art (*e.g.*, such as is described above for removing undesired portions of electrodes 130 and 132) and, therefore, not presented herein.

[0033] Thus, according to embodiments, silicon alloy material 470 and/or 480 may be formed having surface of the first junction region 472

and/or surface of the second junction region 482 superior to a top surface of the substrate (*e.g.*, such as surface 136) by a length in the range between 5 nanometers and 150 nanometers in length. For example, as shown in **Figure 4**, surface of the first junction region 472 and/or surface of the second junction region 482 may extend superior to surface 136 of the substrate by length L between 400 and 500 angstroms (*e.g.*, 40-50 nanometers), and silicon alloy materials 470 and/or 480 may extend into N-type well 115 to a depth D, as shown in **Figure 4**, in a range of between 20 and 250 nanometers in depth. Moreover, contemplated are embodiments where depth D is approximately 120 nanometers and length L is in the range between 40 and 50 nanometers in length.

[0034] Furthermore, in embodiments, silicon alloy materials 470 and/or 480 may be deposited, as described above, and then doped to form junction regions in accordance with the characteristics of a desired PMOS device. For example, after deposition of silicon alloy materials 470 and/or 480, one or both of those materials may be doped such as by doping those materials, as described above with respect to doping to form the P-type material of P-type well 105. Thus, for example, silicon alloy materials 470 and/or 480 may be formed as, or may be doped to be, or to increase their polarity as electrically positively charged (P-type) junction region material. Consequently, it is contemplated that silicon alloy material 470 may be the same or different material, and may be doped the same or differently than silicon alloy material 480. Hence, according to embodiments, silicon alloy materials 470 and 480 may include silicon germanium formed by selective CVD deposition of an epitaxial layer having depth D of 120 nanometers and length L of 50 nanometers above surface 136 and subsequently doped with boron after deposition.

[0035] As a result, silicon alloy materials 470 and/or 480 may be selected to be materials of a type, doped suitably, in a junction region void of suitable dimensions, and/or extending to a length L above surface 136 sufficient to operate and/or provide desired strains 474, 476, 484, 486, and/or 494 in accordance with characteristics of a desired PMOS and/or CMOS structure (*e.g.*, such as desired PMOS, as shown by the device on the right side of **Figure 6** or **7**, or desired CMOS, such as shown by structure 600 or 700).

[0036] In addition, according to embodiments, length L to surface of the first junction region 472 and/or a length to surface of the second junction region 482 may include a silicide layer and/or may be complemented by an additional length superior to surface 136 (as viewed) and including a layer of silicide material. For instance, **Figure 5** shows the substrate of **Figure 1** after forming silicide layers on the diffusion regions and gate electrodes of the NMOS and PMOS devices. NMOS junction silicide layers 523, NMOS gate silicide layer 513, PMOS junction region silicide layers 524, and PMOS gate silicide layer 514 formed in, on or in and on, NMOS junction regions 203, NMOS gate electrode 130, PMOS junction regions (*e.g.*, such as portions or all of silicon alloy material 470 and 480, and non or some of PMOS junction regions 204) and PMOS gate electrode 132 respectively. Silicide layers 523, 513, 524, and/or 514 may be formed of the same or various suitable silicide materials and/or by the same or various suitable operations to provide an appropriate surface for coupling to an electrical contact formed to them in accordance with characteristics for the desired PMOS device and/or CMOS structure. For example, one or more of silicide layers 523, 513, 524, and 514 may be formed by sputtering down a blanket of suitable silicide material (*e.g.*, such as nickel (Ni), titanium (Ti), cobalt (Co), and annealing the silicide material so that it reacts with any exposed silicon to form the appropriate silicide layer (*e.g.*, such as nickel silicide (NiSi), titanium silicide ($TiSi_2$), and/or cobalt silicide ($CoSi_2$)). After sputtering down the blanket of suitable silicide material, undesired portions can be etched away (*e.g.*, such as is described above for removing undesired portions of electrodes 130), such as by removal of any unreacted silicide material (*e.g.*, such as any unreacted nickel, titanium, and/or cobalt).

[0037] According to embodiments, a layer of silicide material may be deposited along the entire exposed surface of structure 500 (*e.g.*, such as NMOS device 503 and PMOS device 504 of a CMOS structure) and heated so that the silicide material partially diffuses into selected portions of that entire surface. Thus, it is contemplated that layer of silicide material 523, 513, 524, and/or 514 may consume a portion of NMOS junction regions 203, NMOS gate electrode 513, silicon alloy materials 570 and 580, and/or PMOS gate electrode 514, respectively. More particularly, layers of silicide material 523, 513, 524, and 514

may comprise nickel silicide consuming approximately 20 nanometers of silicon alloy materials 470 and 480 beginning at surfaces 472 and 482 and extending downward, as shown in **Figure 5**. However, the formation of silicide layers 524 and 514 should be such that the formation of those silicide layers or subsequent operations do not cause silicide 524 and 514 to short together (*e.g.*, such as by effecting the length L or surface height 570, 580, and/or height of silicide 514 to be effected such that silicides 524 short to silicide 514). Practices for forming, sizes, and thicknesses (*e.g.*, depth and height) of suitable silicide layers are well known in the art and are, therefore, not further described herein.

[0038] **Figure 6** shows the substrate of **Figure 1** after forming a conformal etch stop layer over the NMOS and PMOS devices. **Figure 6** shows NMOS conformal etch stop layer 663 covering exposed surfaces of NMOS device 603 and PMOS conformal etch stop layer 664 covering exposed surfaces of PMOS device 604. NMOS etch stop layer 663 and/or PMOS etch stop layer 664 may be formed by the same or various suitable operations known in the art and/or of the same or various suitable materials, such as by deposition, sputter deposition, and/or growth of silicon nitride (Si_3N_4) SiO_2, PSG, SiC, as well as various other appropriate materials, sizes, and thicknesses suitable for and in operations suitable for depositing those materials such that surfaces below NMOS etch stop layer 663 and/or PMOS etch stop layer 664 are protected (*e.g.*, such as silicide layers therebelow).

[0039] Further, according to embodiments, NMOS etch stop layer 663 and/or PMOS etch stop layer 664 may include a material that causes NMOS tension 693 in a region of P-type well material 105, as a result of tensile attributes of NMOS etch stop layer such as shown by NMOS etch stop layer tensile vectors 613, 614, and 615. Alternatively, an etch stop material may be selected, that causes PMOS tension 694 in a region of N-type well 115 such as a tension resulting from PMOS etch stop tensile vectors 623, 624, and 625. However, while the region of P-type well material may result in a channel that is overall in tension, as a result of the effect of tensile vectors 613, 614, and 615 of NMOS etch stop layer 663, the region of N-type well material 115 may experience a channel that overall is in compression of the tensile strain 694 that

may be the result of vectors 623, 624, and 625 of PMOS etch stop layer 664 are counteracted by compressive strain 494 resulting from compressive vectors 474, 476, 484, and 486. Moreover, as first surface height 570 and second surface height 580 extend above surface 136, PMOS etch stop layer tensile vectors 623 and 624 have less of an effect and create a less powerful PMOS tension 694 than that of NMOS tension 693, because vectors 623 and 624 are pushed farther away from the region of N-type well material 115 (*e.g.*, the PMOS channel) by the formed or disposed silicon alloy materials 470 and 480 whose surfaces 570 and 580 extend above surface 136. Practices for forming, sizes, and thicknesses of etch stop layer 663 and/or 664 are known in the art and, are therefore not presented further herein.

[0040] **Figure 7** shows the substrate of **Figure 1** after removing an etch stop layer from the PMOS device. **Figure 7** shows an embodiment where PMOS etch stop layer 664 has been removed from one or more portions of the surfaces of PMOS device 703 (*e.g.*, such as is described above for removing undesired portions of electrodes 130 and 132). Thus, PMOS etch stop layer 664 may be removed, such as by patterned etching, selective etching, or other suitable removal techniques from PMOS surfaces 747 which may include the surfaces of one or more of STI 110, surface 170, surface 180, surfaces of gate isolation spacers for PMOS gate electrode 132, and/or the surface of PMOS gate electrode silicide 514. Moreover, removal of PMOS etch stop layer 664 may adjacent to a proximate end of STI 110, along the surface of STI 110 (*e.g.*, such as shown by edge 749), or adjacent to a distal end of STI 110 (*e.g.*, such as shown by edge 743). Practices of removing, area sizes removed, and thicknesses removed of etch stop layer 664 are known in the art and, are therefore not presented further herein.

[0041] According to embodiments, a sufficient or selected portion of area of, a thickness of the layer, and/or all of PMOS etch stop layer 664 is removed to decrease or eliminate any tension or tensile stress resulting from PMOS etch stop layer 664 where it has been removed. Thus, the residual strain 794 in N-type well 115 will include more of a compression in the channel as the strain associated with vectors 474, 476, 484, and 486 are kept largely in tact, while those of vectors 623, 624, and 625 have been substantially removed.

[0042] Furthermore, embodiments include formation of a dielectric layer (*e.g.*, such as a planarized interlayer dielectric (ILD) formed of SiO_2, PSG, Si_3N_4, and/or SiC, as well as various other appropriate materials for the CMOS structure desired) formed over any of the structures shown in **Figures 4-7**. Practices for forming, sizes, and thicknesses of a dielectric layer formed over any of the structures shown in **Figures 4-7** is known in the art and is, therefore, not presented further herein.

[0043] **Figure 8** is a flow diagram of a process for forming a CMOS structure having a PMOS device with silicon alloy material deposited in the junction regions such that the silicon alloy material is in a non-planar relationship with the surface of the substrate. At 810, NMOS and PMOS devices of a CMOS structure are formed on a substrate having the appropriate wells, junction regions, gate dielectrics, gate electrodes, and gate isolation spacers, and STIs (*e.g.*, such as is shown in **Figure 2**). At 820, a portion of PMOS junction regions 204 and possibly N-type well 115 are removed to a width and depth as desired adjacent PMOS gate electrode 132 (*e.g.*, such as is shown in **Figure 3**). For example, first and second PMOS junction region voids 340 and 360 may be formed such as by etching, as described herein.

[0044] At 830, silicon alloy material is deposited or formed in the PMOS junction regions such that a surface of the first junction region and a surface of the second junction region are in a non-planar relationship with the surface of the substrate (*e.g.*, for example, as shown in **Figure 4**). For example, silicon germanium, doped silicon germanium, silicon carbide, silicon carbon, carbon doped silicon with lattice spacings different from than the silicon substrate (*e.g.*, N-type well 115) can be deposited including by an operation using one or more of CVD, epitaxial deposition, and/or selective deposition. Thus, for a PMOS device, such as shown by 404, a silicon alloy having a lattice spacing larger than that of the substrate can be deposited to provide a compressive strain in the substrate (*e.g.*, such as in the PMOS channel).

[0045] On the other hand, for an NMOS device, embodiments include formation of structure 404 where the electrical type of the materials is reversed (*e.g.*, such that well 115 is P-type material, gate electrode 132 is N-type material,

etc. as necessary in accordance with the characteristics of the desired NMOS device). A silicon alloy material having a lattice spacing that is smaller than the silicon substrate (*e.g.*, such as silicon carbide, silicon carbine, and/or carbon doped silicon) can be deposited into a first and second NMOS junction region void (*e.g.*, the NMOS equivalence of voids 340 and 360) to cause a tensile or tension in the channel of the NMOS device (*e.g.*, such as by creating the opposite vectors of those shown by 474, 476, 484, 486, and 494).

[0046] For example, a surface of the substrate may define a top surface of the substrate and the surface of the first junction region, and the surface of the second junction region (*e.g.*, of either a PMOS or NMOS device embodiment, as described above) are superior to the top surface of the substrate. Deposition of the silicon alloy material may include depositing a thickness or amount of the material sufficient to cause a desired strain (*e.g.*, a tension, or compression) in the substrate (*e.g.*, such as in a region of the well or channel of the device), as desired. Moreover, the deposition of silicon alloy material may include a concentration or type of silicon alloy material having a silicon alloy lattice spacing that comprises a different lattice spacing (*e.g.*, smaller or larger) than the lattice spacing of the substrate material, as desired, to cause the target strain in the substrate. Furthermore, the deposition of the silicon alloy material may comprise deposition of one or more of silicon germanium, silicon carbide, doped with one or more of boron, and/or aluminum to form an electrically positive charge junction region material.

[0047] At 840, silicide layers are formed on the silicon alloy material and gate electrode (*e.g.*, such as is shown in **Figure 5**). For example, nickel, titanium, and/or cobalt may be deposited onto the exposed surfaces, as shown in **Figure 4**, in a manner as known in the art such that the nickel, titanium, and/or cobalt reacts with any exposed silicon to form a silicide, and then any unreacted portions may be etched away. Thus, the silicide layers may consume of the silicon alloy material and/or gate electrode.

[0048] At 860, an etch stop layer may be formed over the current surfaces of the device (*e.g.*, such as is shown in **Figure 6**). For example, a conformal layer of tensile silicon nitride can be deposited on the NMOS and

PMOS device sufficient to cause a compression in the NMOS channel. Moreover, the type, thickness, and/or method of deposition of the etch stop layer may be selected such that the resulting tension in the PMOS channel does not overcome the compression from the silicon alloy deposition selected.

[0049] Correspondingly, according to embodiments, a tensile etch stop layer may be selectively formed only over the NMOS portion of a CMOS structure. Alternately, according to embodiments, a tensile etch stop layer formed over a CMOS structure may be subsequently removed from the PMOS portion of the CMOS structure.

[0050] Although **Figures 1-8** describe formation of a CMOS structure having an NMOS device and PMOS device therein, embodiments include formation of a PMOS device portion, as described above (*e.g.*, such as device 404, 504, 604, and/or 703) without the NMOS device. Thus, contemplated formation of independent single PMOS devices, single PMOS devices coupled to form a device other than a CMOS structure multiple coupled PMOS devices, or other appropriate circuit devices on a substrate where the description above with respect to silicon alloy material formed or disposed in junction regions such that the surface of the silicon alloy material is in a non-planar relationship with the surface of a substrate applies.

[0051] The invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

Claims:

1. An apparatus comprising:

a substrate;

a first device including a gate electrode on a surface of the substrate and a first junction region and a second junction region in the substrate adjacent the gate electrode the first junction region and the second junction region defining a channel region in a first well of the substrate; and

an epitaxial layer comprising a silicon alloy material disposed in each of the first junction region and the second junction region such that a surface of the first junction region and a surface of the second junction region are in a non-planar relationship with the surface of the substrate, and the silicon alloy material extends below the surface of the substrate, wherein a lattice spacing of the silicon alloy material is different than a lattice spacing of a material of the well of the substrate;

a second device complementary to the first device and comprising a gate electrode on the surface of the substrate and junction regions formed in a second well of the substrate, the second well of a conductivity type different than a conductivity type of the first well; and

a dielectric material selectively disposed on the surface of the substrate in an area defined by the second well.

2. The apparatus of claim 1, wherein a surface of the substrate defines a top surface of the substrate and the surface of the first junction region and the surface of the second junction region are superior to the top surface of the substrate.

3. The apparatus of claim 1, wherein the surface of the first junction region and the surface of the second junction region are superior to the top surface of the substrate by a length in the range of between 5 nanometers and 150 nanometers.

4. The apparatus of claim 3, wherein the first junction region and the second junction region define a depth in the range of between 30 nanometers and 250 nanometers in depth.

5. The apparatus of claim 4, wherein the lattice spacing of the silicon alloy material is larger than the lattice spacing of the material of the well of the substrate.

6. The apparatus of claim 1, wherein a surface of the substrate proximate to the first junction region defines a first substrate sidewall surface and a surface of the substrate proximate to the second junction region defines a second substrate sidewall surface and the silicon alloy material disposed in the first junction region is attached to the first substrate sidewall surface and the silicon alloy material disposed in the second junction region is attached to the second substrate sidewall surface.

7. The apparatus of claim 1, wherein the silicon alloy material comprises an epitaxial layer of silicon alloy material.

8. The apparatus of claim 1, wherein the silicon alloy material comprises one of silicon germanium (Si_{y-x} Ge_x), silicon carbide (Si_{y-x} C_x), nickel silicide (NiSi), titanium silicide ($TiSi_2$), and cobalt silicide ($CoSi_2$).

9. The apparatus of claim 1, further comprising a layer of silicide material on the surface of the first junction region, the surface of the second junction region, and the gate electrode, wherein the layer of silicide material comprises one of nickel silicide (NiSi), titanium silicide ($TiSi_2$), and cobalt silicide ($CoSi_2$).

10. The apparatus of claim 9, further comprising a layer of conformal etch stop material on the layer of silicide material, wherein the layer of etch stop material comprises one of silicon dioxide (SiO_2), phosphosilicate glass (PSG, a Phosphorous doped SiO_2), silicon nitride (Si_3N_4), and silicon carbide (SiC).

11. The apparatus of claim 10, further comprising a layer of dielectric material comprising on the layer of conformal etch stop material, wherein the layer of dielectric material comprises one of carbon doped oxide (CDO), cubic boron nitride (CBN), silicon dioxide (SiO_2), phosphosilicate glass (PSG), silicon nitride (Si_3N_4), fluorinated silicate glass (FSG), and silicon carbide (SiC).

12. An apparatus comprising:

a substrate;

a first device including a gate electrode on a surface of the substrate and a first junction region and a second junction region in the substrate adjacent the gate electrode the first junction region and the second junction region defining a channel in a first well of the substrate; and

a silicon alloy material, having a silicon alloy lattice spacing that is different than a lattice spacing of the single crystal silicon of the well of the substrate, disposed in each of the first junction region and the second junction region such that a surface of the first junction region and a surface of the second junction region are superior to the top surface of the substrate by a length sufficient to cause a strain in the channel of the substrate, and the silicon alloy material extends below the surface of the substrate, wherein a lattice spacing of the silicon alloy material is different than a lattice spacing of a material of the well of the substrate;

a second device complementary to the first device and comprising a gate electrode on the surface of the substrate and junction regions formed in a second well of the substrate, the second well of a conductivity type different than a conductivity type of the first well; and

a dielectric material selectively disposed on the surface of the substrate in an area defined by the second well.

13. The apparatus of claim 12, wherein the substrate comprises an N-type channel/well material having an electrically negative charge, and wherein the silicon alloy material comprises a P-type junction region material having an electrically positive charge.

14. The apparatus of claim 13, wherein the silicon alloy is silicon germanium having a lattice spacing that is larger than a lattice spacing of the N-type channel/well material, and wherein the strain is a compressive strain.

15. A method comprising:

forming a first device in an area of a substrate defined by a first well, the device including:

a gate electrode on a surface of the substrate;

a first junction region and a second junction region in the first well adjacent the gate electrode;

depositing a silicon alloy material in each of the first junction region and the second junction region such that a surface of the first junction region and a surface of the second junction region are in a non-planar relationship with the surface of the substrate;

forming a second device in an area of the substrate defined by a second well having a conductivity type different from the first well the second device comprising a gate electrode on the surface of the substrate and junction regions formed in the second well; and

selectively forming a dielectric layer over the area of the substrate defined by the second well.

16. The method of claim 15, wherein depositing the silicon alloy material comprises depositing a sufficient thickness of silicon alloy material having a larger lattice spacing than a lattice spacing of the substrate to cause a compressive strain in the range between 0.5 percent compression and 2.5 percent compression in the substrate.

17. The method of claim 15, wherein depositing the silicon alloy material comprises a chemical vapor deposition sufficient to form an epitaxial layer of silicon alloy material.

18. The method of claim 15, wherein depositing the silicon alloy material comprises depositing silicon alloy material in the first junction region superjacent to a first substrate sidewall surface of the substrate proximate to the first junction region, and depositing silicon alloy material in the second junction region superjacent to a second substrate sidewall surface of the substrate proximate to the second junction region.

19. The method of claim 15, further comprising doping the substrate material with one of phosphorous, arsenic, and antimony to form an N-type channel/well material having an electrically negative charge.

20. The method of claim 15, further comprising doping the silicon alloy material with one of boron and aluminum to form a P-type junction region material having an electrically positive charge.

21. The method of claim 15, further comprising forming a layer of silicide material on the surface of the first junction region, the surface of the second junction region, and the gate electrode.

22. The method of claim 21, further comprising forming a sufficient layer of conformal etch stop material on the layer of silicide material to cause a tensile strain in the channel.

23. The apparatus of claim 1, wherein the dielectric material imposes tensile attributes on the second well.

24. The apparatus of claim 12, wherein the dielectric material imposes tensile attributes on the second well.

ABSTRACT OF THE DISCLOSURE

PMOS TRANSISTOR STRAIN OPTIMIZATION WITH RAISED JUNCTION REGIONS

Optimal strain in the channel region of a PMOS transistor is provided by silicon alloy material in the junction regions of the device in a non-planar relationship with the surface of the substrate. The silicon alloy material, the dimensions of the silicon alloy material, as well as the non-planar relationship of the silicon alloy material with the surface of the substrate are selected so that the difference between the lattice spacing of the silicon alloy material and of the substrate causes strains in the silicon alloy material below the substrate surface, as well as above the substrate surface, to affect an optimal silicon alloy induced strain in the substrate channel. In addition, the non-planar relationship may be selected so that any strains caused by different lattice spaced layers formed over the silicon alloy material have a reduced effect on the strain in the channel region.

Fig. 7