

ERROR CORRECTION SYSTEM

ABSTRACT

Embodiments of the disclosure provide an error correction system including: M decoding units, each configured to perform decoding on the X first operation codes and the Y second operation codes; here the decoding unit includes: a decoder, configured to receive the X first operation codes and output N first decoded signals, each of the N first decoded signals corresponding to a respective one bit of the N data; a first AND gate unit, configured to receive and perform a logical AND operation on Z selected operation codes; an NOR gate unit, configured to receive and perform a logical NOR operation on (Y-Z) unselected operation codes; and N second AND gate units, each having an input terminal connected to an output terminal of the first AND gate unit, an output terminal of the NOR gate unit and one of the first decoded signals, here at least one of error detection or error correction is performed on the memory system based on the output of the N second AND gate units.

[Fig. 11]