SYSTEM AND METHOD FOR ESTABLISHING A KNOWN TIMING RELATIONSHIP BETWEEN TWO CLOCK SIGNALS

BACKGROUND

[0001] Digital electronic systems, e.g., computer systems, often comprise a number of circuit domains that need to communicate with one another using different interfaces, each running at an optimized speed for increased performance. Typically, multiple clock signals having related frequencies are utilized for providing appropriate timing to the interfaces. For instance, a clock signal with a particular frequency may be provided separately to two circuits that are physically spaced apart, wherein one circuit is operable to transmit data to the other. Accordingly, where data is to be transferred at high rates between a transmitting circuit and a receiving circuit, a clock signal is also provided by the transmitting circuit via a separate trace such that data may be registered accurately at the receiving end using a local clock signal that is derived from the transmitted clock signal (which may also be referred to as the transported clock signal). In such applications, it would be necessary that the clock signal used for clocking out data towards the receiving circuit be disposed in a known relationship with the transported clock signal so that proper timing reference may be obtained for capturing the data. There are no known mechanisms that address this requirement, however.

SUMMARY

[0002] A system and method for establishing a known timing relationship between two clock signals are disclosed. In one embodiment, a first clock signal is operable to clock data transfer operations from a transmitter domain to a receiver domain and a second clock signal is operable to be transported to the receiver domain. Circuitry is provided for detecting an edge in a global framework clock (GFC) signal that is supplied to the transmitter domain. A common alignment signal is manufactured that is derived at least in part from the GFC signal. A multiplexer and register arrangement is operable to output the second clock signal in response to the common alignment signal which is also used for gating the data transfer operations clocked by the first clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1 depicts a functional block diagram of a digital electronic system embodiment where multiple integrated circuit domains disposed at different locations communicate with each other using clock and data signals having a known timing relationship;

[0004] FIG. 2 depicts a functional block diagram of a generic transmitter and receiver combination of the electronic system embodiment shown in FIG. 1 for clocking data from the transmitter circuit domain to the receiver circuit domain with a clock signal that is disposed in a known relationship with a clock signal transported to the receiver circuit;

[0005] FIG. 3 depicts an embodiment of a circuit system for establishing a known timing relationship between two independent clock signals;

[0006] FIG. 4 depicts a timing diagram relating to the various signals used in establishing a known timing relationship between two independent clock signals by the system shown in FIG. 3; and

[0007] FIG. 5 depicts a flow chart of the operations involved in one embodiment of a method for establishing a known timing relationship between two independent clock signals.

DETAILED DESCRIPTION OF THE DRAWINGS

[0008] In the drawings, like or similar elements are designated with identical reference numerals throughout the several views thereof, and the various elements depicted are not necessarily drawn to scale. Referring now to FIG. 1, depicted therein is a functional block diagram of an exemplary digital electronic system 102 having multiple integrated circuit domains (ICDs) disposed at different locations wherein a circuit design embodiment of the present invention may be advantageously implemented such that ICDs communicate with each other using clock and data signals having a known timing relationship. In one application, the electronic system 102 may comprise a data transfer board in a high-performance computer system such as a multiprocessor system, where data is efficiently transmitted from one source to a number of receiving entities on the board using synchronous signaling. Reference numerals 104-1 through 104-N refer to ICD1 through ICD(N) that communicate with each

other wherein data pulses are clocked out from a transmitting domain with a first clock signal, e.g., clock signal 106-1, that has a known timing relationship with a second clock signal, e.g., clock signal 110, that is transported to the receiving domains. In one implementation, ICD1 104-1 is operable to receive data 108 from another domain external to the electronic system 102, wherein the data is clocked out using CLK-1 106-1 on a data path 112 that fans out to the remaining ICDs. Also, to synchronize data registration operations by the receiving ICDs that are disposed at variable distances with respect to the transmitting ICD1 104-1, a transported clock signal is provided using clock path 110 that extends from ICD-1 104-1 to the remaining ICDs. The transported clock signal may be manufactured as will be set forth below in reference to FIG. 2. Clock receiver circuitry in each receiving ICD uses the transported clock signal to manufacture its own internal clock signal that provides timing with respect to the various operations of its domain, e.g., data capture and cleanup, data processing by core circuitry, et cetera. In FIG. 1, reference numerals 106-2 through 106-N refer to the internal clock signals generated by the receiving ICDs that are derived from the transported clock signal 110, which is in a known timing relationship with CLK-1 106-1 used for clocking out data.

[0009] FIG. 2 depicts a functional block diagram of an embodiment of a generic transmitter and receiver ICD combination subsystem 200. Reference numeral 202 refers to a data/clock transmitting ICD (ICD-TX) that is operable with a clock signal labeled as TX-CLK 222. A global timing source such as a crystal (XTAL) 210 is operable for providing all necessary clock signals with respect to the TX/RX ICD

combination subsystem 200. A divider (DIV) block 212 operates to reduce the frequency of the raw timing signal provided by XTAL 210. A delay logic loop (DLL) block 216 provided as part of ICD-TX 202 conditions the incoming timing signal output by the DIV block 212. The output of DLL 216 is operable as the core clock for ICD-TX 202 which is provided to a number of clock buffers that form a clock tree 218. Reference numerals 220-1 and 220-2 illustrate two such clock buffers, TX-CLK-BUFF(1) and TX-CLK-BUFF(2), respectively. The output of the clock buffers is provided as individual core clock signals TX-CLK 222 that provide timing with respect to various internal operations of the ICD-TX circuitry.

[0010] Another divider block 215 is also provided for generating a global framework clock (GFC) signal 214 that is substantially slower than the core clock signal used by ICD-TX 202. For example, XTAL 210 may generate a raw 500 MHz clock signal that can be divided to a 250 MHz clock for driving the transmitter domain's clock tree 218. On the other hand, the GFC 214 may be manufactured such that it is 32 times slower than the core clock (i.e., the GFC signal has a single tick for every 32 ticks of the core clock). As will be seen in greater detail hereinbelow, the GFC signal 214 is not only used an overall timing/monitoring reference signal that is provided to all ICDs of the system, but it is also used in a circuit embodiment of the present invention for effectuating a known timing relationship between two independent clock signals.

[0011] Data transfer operations are effectuated by a data out block 224 of the transmitter domain that is clocked by

TX-CLK 222. Data 226 that is to be transmitted is registered by a data out register stage 225 whose output is provided to a driver/buffer stage 227 coupled to an outgoing data path 206. A common alignment block 228 is operable responsive at least in part to another TX-CLK signal 222 and GFC 215 for outputting a transported clock (QUAD-CLK) signal that is provided to a receiving domain ICD-RX 204 via a clock path 208. Further, the common alignment block 228 is also operable to generate a common alignment control signal that controls register block 225 of the data out block 224 such that data may be transferred only when the control signal is asserted. Data received via data path 206 is staged through a driver/buffer 230 whose output is provided to data registration circuitry 232 of the receiver domain. Conditioned/captured data may thereafter be forwarded to the internal core circuitry 234 thereof. As will be seen below, by deriving the common alignment control signal from the GFC signal and using it for gating the data out operations as well as for generating the transported clock signal, repeatability and reliability of inter-domain data transfer functionality may be ensured.

[0012] A receiver DLL 236 is operable with reference to the received QUAD-CLK via clock path 208, whose output is provided to a number of clock buffers that form a clock tree 238 of ICD-RX 204. By way of example, reference numerals 240-1 and 240-2 illustrate two such buffers, RX-CLK-BUFF(1) and RX-CLK-BUFF(2), respectively. The output of the clock buffers is operable as a clock signal (RX-CLK) 242 internal to the receiver domain for timing its operations. Since the receiver's clock signal is derived from the transported clock signal provided by the transmitter, it is necessary that the

clock signal used for clocking out data on data path 206 be disposed in a known timing relationship with respect to the transported clock signal so that the incoming data may be accurately registered without incurring transfer-related timing errors.

[0013] Taking FIGS. 1 and 2 together, it should be apparent to one skilled in the art that the subsystem 200 described above is an embodiment that essentially captures a subportion of the electronic system 102 shown in FIG. 1. Accordingly, data signal path 206 and QUAD-CLK 208 illustrated in FIG. 2 are operable analogous to the data signal path 112 and transported clock signal 110 depicted in FIG. 1.

[0014] FIG. 3 depicts an embodiment of a circuit system 300 for establishing a known timing relationship between two independent clock signals by manufacturing a common alignment signal that controls both data out operations (clocked with a first clock signal) and generation of a transported clock signal (i.e., a second clock signal) of a transmitting domain, e.g., ICD-TX 202 shown in FIG. 2 wherein the circuit system 300 is operable as the common alignment block 228 thereof. Circuit means comprising one or more register stages 302 or their well known equivalents is provided for detecting an edge, e.g., a rising edge, in the GFC signal 214 that is applied to the D input of the register stage. The CLK input of the register stage 302 is activated by a first clock signal, e.g., TX-CLK 222. Since it is desirable to establish the timing relationship between the clock signals at the earliest upon a system reset, circuit means comprising one or more register stages 304 or their well known

equivalents is provided for registering an active low reset signal, labeled as PWR-RST-L 306, that is applied to the D input of the register stage. Again, the CLK input of the register stage 304 is activated by the first clock signal, TX-CLK 222. Upon detecting the occurrence of a starting edge in the GFC signal 214, the detector register 302 outputs a GFC-EDGE-DETECT signal 308 that is coupled to a two-input OR gate 312. The other input of the OR gate 312 is driven by a feedback path so that once a common alignment signal 320 is generated upon the system reset and occurrence of the GFC's starting edge, it stays active. Accordingly, circuit means comprising a clearable register 314 or its well known equivalents coupled to OR gate 312 at its D input is provided with a clear (CLR) input terminal that is driven by the output of register 304, i.e., LOG-RST-L 310. Once again, the clearable register is clocked by TX-CLK 222. The Q output of the clearable register 314 is operable as the common alignment (OAQ-ALIGN) signal 320 that is used for controlling both data transfer operations from the transmitting domain as well as the generation of the transported clock signal (e.g., the QUAD-CLK signal) therefrom. With respect to the data transfer, the OAQ-ALIGN 320 signal is used as a gating signal for the data out transfer circuitry 224 to ensure that the data that is clocked out is in a fixed relationship as to the clock signal that is generated for transport.

[0015] As will be set forth below in additional detail, a multiplexer/register arrangement is provided for outputting the transported clock signal in response to the common alignment signal. A master/slave register circuit portion comprising a master register 316 whose Q output is coupled to drive the D input of a slave register 318 is operable to

register the OAQ-ALIGN 320 signal twice such that the outputs of the registers, M-REG 322 and S-REG 324, respectively, are supplied to the logic low and logic high inputs of a 2:1 multiplexer (MUX) element 326. MUX 326 is controlled by the OAQ-ALIGN 320 in the generation of a MUX-SEL control signal 328. Further, MUX 326 operates in such a manner that the creation of runt pulses is avoided. A pair of 2:1 MUXes 330A and 330B are provided whose control inputs are driven by MUX-SEL 328 so as to toggle between TX-CLK 222 and its complement TX-CLK-BAR 223. The "0" or logic low input of MUX 330A is tied to "0" whereas the "0" input of MUX 330B is tied to "1", whereby the MUXes respectively output a logic low and a logic high before a clock signal is generated. Upon the occurrence of MUX-SEL 328, the outputs of the 2:1 MUXes 330A and 330B toggle to their respective active inputs, i.e., TX-CLK and TX-CLK-BAR signals. Each clock output is buffered by a corresponding clock buffer stage 332A or 332B in order to generate a QUAD-CLK-LOW 334A or QUAD-CLK-HIGH 334B that are transmitted to the receiving ICD.

[0016] Referring now to FIG. 4, depicted therein is a timing diagram panel 400 relating to the various signals used in establishing a known timing relationship between two clocks by the system shown in FIG. 3. As can be readily seen, upon detection of a starting edge (e.g., a rising edge) in GFC 214, a corresponding edge (i.e., a rising edge) in OAQ-ALIGN 320 is generated, once the system is taken out of reset. As pointed out earlier, the feedback loop arrangement in the circuitry responsible for generating the OAQ-ALIGN signal maintains the logic high level once a rising edge in the GFC signal is detected that forms the reference point for

establishing timing relationships in the transmitting domain. Subsequently, the master/slave register arrangement registers the OAQ-ALIGN signal twice which results in the rising edges in M-REG 322 and S-REG 324. In response thereto, a rising edge in MUX-SEL 328 is generated, which thereafter controls the 2:1 MUXes used for outputting the transported clock signal and its complement, i.e., QUAD-CLK-LOW 334A or QUAD-CLK-HIGH 334B, towards a receiving domain.

[0017] FIG. 5 is a flow chart of the various operations involved in one embodiment of a method for establishing a known timing relationship between two independent clock signals. At block 502, a starting edge is detected in a GFC clock signal that provides an overall timing reference signal to an electronic system having one or more transmitter ICDs and one or more receiver ICDs. In one implementation, the first rising edge in the GFC signal upon a system reset is detected. Thereafter, a common alignment signal is manufactured that is derived at least in part from the GFC signal (block 504). The common alignment signal is subsequently used in gating the data transfer operations, wherein outgoing data is registered using a first clock signal. Further, the common alignment signal is also used for controlling the generation of a second clock signal in a clock out operation, whereby the second clock signal is transported to a receiver domain. These operations are consolidated at block 506.

[0018] Based on the foregoing Detailed Description, it should be appreciated that an embodiment of the present invention has been provided in accordance herewith for advantageously establishing a known timing relationship

between two clocks in a digital electronic system. The known timing relationship may be used by a receiving domain for properly registering the incoming data whereby data transfer errors can be avoided, especially in high-speed data transmission applications.

[0019] Although the aforesaid Detailed Description has been set forth with reference to certain illustrations, it is to be understood that the forms of the invention shown and described are to be treated as exemplary embodiments only. For instance, various logic modules, control signals and their logic levels illustrated in the FIGURES of the present patent application may be implemented using a number of different electronic devices and/or gate combinations, with any level of integration. Accordingly, various changes, substitutions and modifications can be realized therein without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

1. A system for establishing a known timing relationship between two clock signals, wherein a first clock signal (222) is operable to clock data transfer operations from a transmitter domain (202) to a receiver domain (204) and a second clock signal (334A or 334B) is operable to be transported to said receiver domain (204), comprising:

means (302) for detecting an edge in a global framework clock (GFC) signal (214) that is supplied to said transmitter domain (202);

means (314) for manufacturing a common alignment signal (320) that is derived at least in part from said GFC signal (214); and

a multiplexer arrangement (326,330A,330B) operating to output said second clock signal (334A or 334B) in response to said common alignment signal (320), wherein said data transfer operations are gated with said common alignment signal (320).

2. The system for establishing a known timing relationship between two clocks as set forth in claim 1, wherein said means (302) for detecting an edge in said GFC signal (214) comprises a register arrangement (302) that is clocked using said first clock signal (222).

3. The system for establishing a known timing relationship between two clocks as set forth in claim 1 or claim 2, wherein said means (314) for manufacturing said common alignment signal (320) comprises a register arrangement (314) that is clocked using said first clock signal (222).

4. The system for establishing a known timing relationship between two clocks as set forth in claim 1, claim 2 or claim 3, further including a master and slave register arrangement (316,318) coupled to said means (314) for manufacturing said common alignment signal (320), said master and slave register arrangement (316,318) operating to provide two outputs suppled to a first 2:1 multiplexer (MUX) (326) of said multiplexer arrangement (326,330A,330B).

5. The system for establishing a known timing relationship between two clocks as set forth in claim 4, wherein said first 2:1 MUX's (326) output is provided to control second and third 2:1 MUXes (330A,330B) of said multiplexer arrangement, said second 2:1 MUX (330A) operating to output said second clock signal (334A) and said third 2:1 MUX (330B) operating to output said second clock's complement (334B).

6. A method for establishing a known timing relationship between two clock signals, wherein a first clock signal (222) is operable to clock data transfer operations from a transmitter domain (202) to a receiver domain (204) and a second clock signal (334A or 334B) is operable to be transported to said receiver domain (204), comprising:

detecting an edge in a global framework clock (GFC) signal (214) that is supplied to said transmitter domain (202);

manufacturing a common alignment signal (320) that is at least in part derived from said GFC signal (214); and

using said common alignment signal (320) for gating said data transfer operations and for controlling a multiplexer arrangement (326,330A,330B) in outputting said second clock signal (334A or 334B).

7. A computer system provided with circuitry for establishing a known timing relationship between two clock signals, wherein a first clock signal (222) is operable to clock data transfer operations from a transmitter domain (202) to a receiver domain (204) and a second clock signal (334A or 334B) is operable to be transmitted to said receiver domain (204), said transmitter and receiver domains forming at least a portion of said computer system, said circuitry comprising:

a register (302) operating responsive to said first clock signal (222) for detecting an edge in a global framework clock (GFC) signal (214) that is supplied to said transmitter domain (202);

means (314) for manufacturing a common alignment signal (320) that is derived at least in part from said GFC signal (214); and

a multiplexer arrangement (326,330A,330B) operating to output said second clock signal (334A or 334B) in response to said common alignment signal (320), wherein said data transfer operations are gated with said common alignment signal (320).

8. The computer system provided with circuitry for establishing a known timing relationship between two clocks as set forth in claim 7, further including means (304) for activating said means (314) for manufacturing said common alignment signal (320) upon a system reset.

9. The computer system provided with circuitry for establishing a known timing relationship between two clocks as set forth in claim 7 or claim 8, wherein said GFC signal (214) is generated from a system clock provided by a timing source (210).

10. A circuit for establishing a known timing relationship between two clocks, wherein a first clock signal (222) is operable to clock data transfer operations from a transmitter domain (202) to a receiver domain (204) and a second clock signal (334A or 334B) is operable to be transported to said receiver domain (204), comprising:

a register (302) operating responsive to said first clock signal (222) for detecting an edge in a global framework clock (GFC) signal (214) that is supplied to said transmitter domain (202);

a register (304) operating responsive to said first clock signal (222) for registering a system reset signal (306);

a clearable register (314) having its data input coupled to an OR logic gate (312) and its clear terminal coupled to an output from said register (304) for

registering said system reset signal (306), wherein a first input of said OR logic gate (312) is driven by an output from said register (302) for detecting said edge in said GFC signal (214) and a second input of said OR logic gate (312) is coupled to said clearable register's data output in a feedback loop path, said clearable register (314) operating to manufacture a common alignment signal (320) that is derived at least in part from said GFC signal (214);

a master register (316) operating responsive to said first clock signal (222) for generating a master register output signal (322) by registering said common alignment signal (320);

a slave register (318) operating responsive to said first clock signal (222) for generating a slave register output signal (324) by registering said master register output signal (322);

a first 2:1 multiplexer (MUX) element (326) coupled to said master and slave registers such that its logic low input is driven by said master register output signal (322) and its logic high input is driven by said slave register output signal (324), wherein said common alignment signal (320) operates to control said 2:1 MUX element (326) for generating a MUX selection control signal (328);

a second 2:1 MUX element (330A) operating responsive to said MUX selection control signal (328) for

generating a second clock signal (334A) dependent on said first clock signal (222); and

a third 2:1 MUX element (330B) operating responsive to said MUX selection control signal (328) for generating said second clock signal's complement (334B).