Abstract

SEMICONDUCTOR DEVICE AND METHOD OF FORMING CAVITY IN PCB CONTAINING ENCAPSULANT OR DUMMY DIE HAVING CTE SIMILAR TO CTE OF LARGE ARRAY WLCSP

A semiconductor device has a PCB with a cavity formed in a first surface of the PCB. A stress compensating structure, such as an encapsulant or dummy die, is disposed in the cavity. An insulating layer is formed over the PCB and stress compensating structure. A portion of the insulating layer is removed to expose the stress compensating structure. A conductive layer is formed over the stress compensating structure. A solder masking layer is formed over the conductive layer with openings to the conductive layer. A semiconductor package is mounted over the cavity. The semiconductor package is a large array WLCSP. Bumps electrically connect the semiconductor package and conductive layer. The semiconductor package is electrically connected to the conductive layer. The CTE of the stress compensating structure is selected substantially similar to or matching the CTE of the semiconductor package to reduce stress between the semiconductor package and PCB.
(Fig.4)