

METHOD FOR FORMING ISOLATION TRENCH, MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE, AND PROCESS DEVICE

TECHNICAL FIELD

5 [0001] The present disclosure relates to the field of semiconductor technology, and in particular, to a method for forming an isolation trench, a manufacturing method for a semiconductor device, and a processing device.

BACKGROUND

10 [0002] With the development of semiconductor technology, integrated circuits develop toward smaller sizes and higher integration. As gate sizes of Field Effect Transistors (FETs) are continuously reduced, the FETs gradually develop from Planar Field Effect Transistors (Planar FETs) to Fin Field Effect Transistors (Fin FETs) with higher efficiency.

[0003] At present, a gate is mostly prepared by a gate last process, which generally includes
15 forming a dummy gate on a substrate, then performing ion implantation on the substrate to form a doped region, removing the dummy gate by high-temperature annealing, and finally sequentially depositing a gate dielectric layer and filling a gate material in a region where the dummy gate is removed to form a gate. In the gate last process, the dummy gate is generally designed based on a position and a size of the actual gate. However, with the
20 continuous reduction of sizes of the FETs, for a position with a relatively small design size and a relatively high aspect ratio, dimensional deviation and dielectric damage can be easily caused when the dummy gate is removed, such that voids can be easily formed during subsequent metal filling, which reduces device reliability.

[0004] In order to solve the above problems, in a process flow, a gate structure and a
25 dielectric layer exposing a top wall of the gate structure are formed on a substrate, and the dielectric layer and the gate structure are then respectively etched to form isolation trenches which divide the gate structure into a plurality of gates, so that the steps of forming and removing the dummy gate can be omitted, and requirements for small size and high aspect ratio can be met. However, when feature sizes of devices are further reduced, for example,
30 the feature sizes are reduced from 14 nm to 10 nm, the process flow cannot meet design

requirements of the devices, and is not favorable for improvement in integration of integrated circuits.

SUMMARY

5 [0005] The present disclosure provides a method for forming an isolation trench, a manufacturing method for a semiconductor device, and a process device, and aims to solve the technical problem in the related technology that design requirements of devices cannot be met to facilitate improvement in integration of integrated circuits when feature sizes of the devices are further reduced.

10 [0006] In a first aspect, the present disclosure provides a method for forming an isolation trench, including:

providing a to-be-etched object, which includes a substrate, a gate structure, and an isolation dielectric layer, the gate structure and the isolation dielectric layer being located on a surface of the substrate, and the gate structure extending along a first direction and
15 being disposed on a same layer as the isolation dielectric layer; and

alternately and cyclically etching the isolation dielectric layer and the gate structure to form a first isolation trench, the first isolation trench penetrating through the gate structure along a second direction, and the first direction being perpendicular to the second direction; wherein, in each cycle, the isolation dielectric layer is etched by a predetermined depth to
20 expose a part of the gate structure, and then the exposed part of the gate structure is etched to make a top surface of the gate structure substantially flush with a top surface of the isolation dielectric layer.

[0007] In an implementation, the to-be-etched object further includes an interlayer dielectric layer located between the substrate and the gate structure, and the first isolation
25 trench exposes a top wall of the interlayer dielectric layer; and after forming the first isolation trench, the method further includes:

etching a portion of the interlayer dielectric layer which is exposed through the first isolation trench to form a second isolation trench, the first isolation trench and the second isolation trench communicating with each other to form a target isolation trench.

30 [0008] In an implementation, alternately and cyclically etching the isolation dielectric layer and the gate structure includes: alternately and cyclically performing an isolation dielectric layer etching step and a gate structure etching step until the gate structure is cut off.

[0009] In an implementation, a mask layer is disposed on a side of the isolation dielectric layer away from the substrate, and the method further includes: before each time of alternately and cyclically performing the isolation dielectric layer etching step and the gate structure etching step, performing a sacrificial layer deposition step to deposit a sacrificial layer on a side of the mask layer away from the substrate; and the sacrificial layer is consumed during the isolation dielectric layer etching step and the gate structure etching step.

[0010] In an implementation, a mask layer is disposed on a side of the isolation dielectric layer away from the substrate, the mask layer is provided with a mask opening, and an orthographic projection of the mask opening on the substrate is perpendicular to and partially overlaps an orthographic projection of the gate structure on the substrate; and

etching the interlayer dielectric layer includes: alternately and cyclically performing a sacrificial layer deposition step and an interlayer dielectric layer etching step until the interlayer dielectric layer is etched to a target depth; and the sacrificial layer deposition step is to deposit a sacrificial layer on a side of the mask layer away from the substrate, and the sacrificial layer is consumed during the interlayer dielectric layer etching step.

[0011] In an implementation, the sacrificial layer deposition step and alternately and cyclically etching the isolation dielectric layer and the gate structure are performed in a same process chamber.

[0012] In an implementation, process conditions of the sacrificial layer deposition step include: a process gas including a silicon-containing gas, and the process gas further including at least one of an oxygen-containing gas or a nitrogen-containing gas.

[0013] In an implementation, the process conditions of the sacrificial layer deposition step further include: an upper electrode power range being between 100 W and 400 W, and a pressure range inside the process chamber being between 5 mTorr and 30 mTorr.

[0014] In an implementation, process conditions of the isolation dielectric layer etching step include a process gas including a fluorine-containing gas; and/or, process conditions of the gate structure etching step include a process gas including a chlorine-containing gas.

[0015] In an implementation, the fluorine-containing gas includes tetrafluoromethane and perfluorobutadiene; and/or, the chlorine-containing gas includes boron trichloride and chlorine.

[0016] In an implementation, the to-be-etched object includes a plurality of discrete fins located between the substrate and the gate structure, the plurality of fins extends along the

second direction, and the gate structure spans the plurality of fins and covers a portion of a top wall and a portion of a sidewall of each fin; and forming the first isolation trench includes: forming the first isolation trench between adjacent fins.

[0017] In a second aspect, the present disclosure provides a manufacturing method for a semiconductor device, including: forming a plurality of semiconductor devices, gate structures of the plurality of semiconductor devices being connected to each other; and cutting off the gate structures of adjacent semiconductor devices with the method for forming an isolation trench described in any of the above implementations, so as to make the gate structures into a plurality of gates.

[0018] In a third aspect, the present disclosure provides a semiconductor process device, including: a process chamber, a gas inlet assembly, a gas exhaust assembly, an upper electrode assembly, a lower electrode assembly, and a controller, the controller including at least one processor and at least one storage device, and the at least one storage device having stored therein a computer program which, when executed by the at least one processor, implements the method described in any of the above implantations in the first aspect.

[0019] The advantages or beneficial effects of the above technical solutions at least include: by alternately and cyclically etching the isolation dielectric layer and the gate structure, the isolation dielectric layer and the gate structure can be etched synchronously, the first isolation trench with a relatively small width and a relatively large depth can be formed, and an etching depth and sidewall morphology of the first isolation trench can be accurately controlled. Thus, in a case where feature sizes of semiconductor devices are further reduced, design requirements of the semiconductor devices for high aspect ratio and etching morphology of an isolation trench can be met, which facilitates improvement in integration of integrated circuits.

BRIEF DESCRIPTION OF DRAWINGS

[0020] The drawings here are incorporated into the specification and constitute a part of the specification. The drawings illustrate the embodiments of the present disclosure, and are used to explain, together with the description, the principle of the present disclosure. In addition, the drawings and the description are not intended to limit the scope of the concept

of the present disclosure in any way, but rather to illustrate the subject matter of the present disclosure for those of ordinary skill in the art with reference to specific embodiments.

[0021] FIG. 1A to FIG. 1E are schematic structural diagrams illustrating steps in a method for forming an isolation trench in the related technology.

5 [0022] FIG. 2 is a flowchart illustrating a method for forming an isolation trench according to an embodiment of the present disclosure.

[0023] FIG. 3A to FIG. 3C are three-dimensional schematic structural diagrams illustrating steps in a method for forming an isolation trench according to an embodiment of the present disclosure.

10 [0024] FIG. 4A to FIG. 9B are schematic cross-sectional views illustrating steps in a method for forming an isolation trench according to an embodiment of the present disclosure.

[0025] FIG. 10 is a schematic structural diagram of a semiconductor process device according to an embodiment of the present disclosure.

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DETAIL DESCRIPTION OF EMBODIMENTS

[0026] Only some exemplary embodiments are briefly described below. As can be understood by those of ordinary skill in the art, the embodiments described herein can be modified in various different ways without departing from the spirit or scope of the present disclosure. Therefore, the drawings and the description should be regarded as being illustrative rather than restrictive.

20 [0027] FIG. 1A to FIG. 1E are schematic structural diagrams illustrating steps in a method for forming an isolation trench in the related technology. FIG. 1A is a schematic cross-sectional view of a to-be-etched object from a first viewing angle in the related technology. FIG. 1B is a schematic cross-sectional view of FIG. 1A from a second viewing angle. FIG. 1C is a schematic cross-sectional view of FIG. 1A after etching of an isolation dielectric layer. FIG. 1D is a schematic cross-sectional view of FIG. 1C after etching of a gate structure. FIG. 1E is a schematic cross-sectional view of FIG. 1D after the etching of the isolation dielectric layer and the etching of the gate structure.

30 [0028] The method for forming an isolation trench includes: as shown in FIG. 1A and FIG. 1B, a substrate 110 is provided, a gate structure 120, an interlayer dielectric layer 130, and an isolation dielectric layer 140 are disposed on a surface of the substrate 110, the gate

structure 120 extends along a first direction D1, the gate structure 120 and the isolation dielectric layer 140 are both disposed on the interlayer dielectric layer 130, and the isolation dielectric layer 140 exposes a top wall of the gate structure 120. A plurality of discrete fins 150 are further disposed between the substrate 110 and the gate structure 120, and extend along a second direction perpendicular to the first direction D1; the gate structure 120 spans the plurality of fins 150; as shown in FIG. 1C, a first isolation trench 171 is formed in the isolation dielectric layer 140 using a mask layer 160, and the first isolation trench 171 exposes a sidewall of the gate structure 120 and the interlayer dielectric layer 130; as shown in FIG. 1D and FIG. 1E, the gate structure 120 exposed through the first isolation trench 171 is removed, and a second isolation trench (not labeled in FIG. 1D and FIG. 1E) is formed inside the gate structure 120, and the second isolation trench exposes a top wall of the interlayer dielectric layer 130, is adjacent to the first isolation trench 171, and communicates with the first isolation trench 171, thereby forming a target isolation trench 170.

[0029] It has been found during the implementation of the method that: in the related technology, by etching the isolation dielectric layer 140 to form the first isolation trench 171 first and then etching the gate structure 120 to form the second isolation trench which communicates with the first isolation trench 171 to form the target isolation trench 170, the target isolation trench 170 has a relatively low aspect ratio, and this etching method is suitable for semiconductor devices with feature sizes larger than 14 nm and above; when the feature sizes of the semiconductor devices are further reduced, for example, the feature sizes are reduced from 14 nm to 10 nm, isolation trenches need to be reduced correspondingly to meet requirements of the devices for high aspect ratio, but the isolation trench formed with the method in the related technology cannot meet the requirements of the devices for high aspect ratio; moreover, referring to FIG. 1C and FIG. 1D, in the related technology, after the first isolation trench 171 is formed, the first isolation trench 171 exposes the top wall of the interlayer dielectric layer 130 and a sidewall of the isolation dielectric layer 140, so that the interlayer dielectric layer 130 is subjected to downward etching along the first isolation trench 171 and the isolation dielectric layer 140 is subjected to lateral etching along the first isolation trench 171 while etching the gate structure 120, with the result that a first groove 131 which is recessed downward is formed in the interlayer dielectric layer 130 and a second groove 141 which is laterally recessed is formed in the isolation dielectric layer 140. Therefore, the method in the related technology can

hardly achieve accurate control of an etching depth and sidewall morphology of the target isolation trench 170, such that etching morphology of the target isolation trench 170 cannot meet design requirements of devices.

[0030] In view of this, the present disclosure provides a method for forming an isolation trench. In a case where feature sizes of semiconductor devices are further reduced, the method for forming an isolation trench can meet requirements of the semiconductor devices for high aspect ratio and etching morphology, so that the method for forming an isolation trench is suitable for manufacturing of the semiconductor devices with smaller feature sizes, thereby facilitating improvement in integration of integrated circuits. The embodiments of the present disclosure will be described in detail below with reference to the drawings.

[0031] The method for forming an isolation trench according to the embodiments of the present disclosure is implemented with a semiconductor process device 200 shown in FIG. 10. Taking the semiconductor process device 200 being an Inductive Coupled Plasma (ICP) etching device as an example, the semiconductor process device 200 includes a radio frequency (RF) coil 21 located at a top of a process chamber 20 and outside a dielectric cylinder (not shown), and a carrier 22 located inside the process chamber 20. The RF coil 21 is electrically connected to an upper RF power supply 23 through an upper matcher 25, and the upper RF power supply 23 is configured to apply upper electrode power to the RF coil 21 through the upper matcher 25, so as to enable the RF coil 21 to excite a process gas in the process chamber 20 into plasma. The carrier 22 is configured to bear a to-be-etched object 100; and the carrier 22 is electrically connected to a lower RF power supply 24 through a lower matcher 26, and the lower RF power supply 24 applies lower electrode power to the carrier 22 through the lower matcher 26 to supply RF bias voltage to the carrier 22.

[0032] FIG. 2 is a flowchart illustrating a method for forming an isolation trench according to an embodiment of the present disclosure. FIG. 3A to FIG. 3C are three-dimensional schematic structural diagrams illustrating steps in a method for forming an isolation trench according to an embodiment of the present disclosure. FIG. 4A to FIG. 9B are schematic cross-sectional views illustrating steps in a method for forming an isolation trench according to an embodiment of the present disclosure. An isolation dielectric layer 140, a mask layer 160, and a sacrificial layer 180 shown in FIG. 4A to FIG. 9B are omitted in FIG. 3A to FIG. 3C.

[0033] As shown in FIG. 2, the method for forming an isolation trench includes the following step S310 and step S320.

[0034] Referring to FIG. 3A, FIG. 4A, and FIG. 4B, at step S310, a to-be-etched object 100 is provided and includes a substrate 110, and a gate structure 120 and an isolation dielectric layer 140 which are located on a surface of the substrate 110, and the gate structure 120 extends along a first direction D1 and is disposed on a same layer as the isolation dielectric layer 140.

[0035] Referring to FIG. 3B and FIG. 6A to FIG. 7B, at step S320, the isolation dielectric layer 140 and the gate structure 120 are alternately and cyclically etched to form a first isolation trench 171, which penetrates through the gate structure 120 along a second direction D2. The first direction D1 is perpendicular to the second direction D2. In each cycle, the isolation dielectric layer 140 is etched by a predetermined depth to expose a part of the gate structure, and then the exposed part of the gate structure 120 is etched to make a top surface of the gate structure 120 substantially flush with a top surface of the isolation dielectric layer 140.

[0036] Illustratively, alternately and cyclically etching the isolation dielectric layer 140 and the gate structure 120 may be performed as follows: as shown in FIG. 6A, the isolation dielectric layer 140 is etched downward by the predetermined depth to expose a top wall and part of sidewalls of the gate structure 120; as shown in FIG. 6B, portions of the gate structure 120 which are exposed through the isolation dielectric layer 140 are etched downward to complete one cycle; referring to FIG. 6A, then, the isolation dielectric layer 140 is further etched downward by the predetermined depth to expose a top wall and part of the sidewalls of the remaining gate structure 120; referring to FIG. 6B, portions of the remaining gate structure 120 which are exposed through the remaining isolation dielectric layer 140 are then etched downward to complete another cycle; in this way, the isolation dielectric layer 140 and the gate structure 120 are alternately etched for a plurality of cycles, with the top surface of the gate structure 120 being substantially flush with the top surface of the isolation dielectric layer 140 after each cycle. The alternate and cyclic etching method can achieve synchronous downward etching of the isolation dielectric layer 140 and the gate structure 120 to form the first isolation trench 171 with a relatively small width and a relatively large depth, so that a requirement of a device for high aspect ratio can be met. Moreover, compared with the related technology, in the present disclosure, since the interlayer dielectric layer 130 is not exposed and an exposed area of the isolation dielectric

layer 140 is smaller during the etching of the gate structure 120, the interlayer dielectric layer 130 is not consumed downward and lateral consumption of the isolation dielectric layer 140 is reduced during the etching of the gate structure 120, so that an etching depth and sidewall morphology of the first isolation trench 171 can be accurately controlled during the etching, and a design requirement of the device for etching morphology can be met. As shown in FIG. 3B, FIG. 7A, and FIG. 7B, a width L of the first isolation trench 171 is a minimum distance between two sidewalls of the first isolation trench 171 in the first direction D1, and a depth H of the first isolation trench 171 is a maximum height of the first isolation trench 171 in a direction D3 perpendicular to the substrate 110.

[0037] In addition, referring to FIG. 3B, FIG. 7A, and FIG. 7B, the first isolation trench 171 is formed inside the isolation dielectric layer 140 and inside the gate structure 120, and penetrates through the gate structure 120 along the second direction D2, so that the gate structure 120 is completely cut off in the second direction D2 to form a plurality of gates 120A.

[0038] With the above technical solutions, by alternately and cyclically etching the isolation dielectric layer 140 and the gate structure 120, the isolation dielectric layer 140 and the gate structure 120 can be etched synchronously, the first isolation trench 171 with a relatively small width and a relatively large depth can be formed, and the etching depth and the sidewall morphology of the first isolation trench 171 can be accurately controlled. Thus, in a case where feature sizes of semiconductor devices are further reduced, design requirements of the semiconductor devices for high aspect ratio and etching morphology of an isolation trench can be met, which facilitates improvement in integration of integrated circuits. The above technical solution is particularly suitable for design of advanced process semiconductor devices or integrated circuits with feature sizes of 10 nm or smaller.

[0039] In an implementation, referring to FIG. 3B, FIG. 3C, and FIG. 8A to FIG. 9B, the to-be-etched object 100 further includes the interlayer dielectric layer 130 between the substrate 110 and the gate structure 120, and the first isolation trench 171 exposes a top wall of the interlayer dielectric layer 130. After step S320, the method further includes: step S330, etching a portion 130A of the interlayer dielectric layer 130 which is exposed through the first isolation trench 171 to form a second isolation trench 172 inside the interlayer dielectric layer 130, with the second isolation trench 172 and the first isolation trench 171 communicating with each other to form a target isolation trench 170.

[0040] It should be noted that, as shown in FIG. 3B, FIG. 7A, and FIG. 7B, the first isolation trench 171 formed at step S320 can cut off the gate structure 120 just along the direction D3 perpendicular to the substrate 110 to form the plurality of gates 120A, but cannot ensure no electrical connection between adjacent gates 120A. In view of this, step S330 is performed to continue to etch the portion 130A of the interlayer dielectric layer 130 exposed through the first isolation trench 171 to form the second isolation trench 172, which can ensure that the gate structure 120 is completely cut off along the direction D3 perpendicular to the substrate 110, and electrical connection between adjacent gates 120A can be avoided.

[0041] FIG. 4A is a schematic cross-sectional view of FIG. 3A taken along a line A1-A2, FIG. 4B is a schematic cross-sectional view of FIG. 3A taken along a line B1-B2, and a mask layer 160 shown in FIG. 4A and FIG. 4B is omitted in FIG. 3A. FIG. 5A is a schematic cross-sectional view of FIG. 4A after first deposition of a sacrificial layer, FIG. 5B is a schematic cross-sectional view of FIG. 4B after first deposition of a sacrificial layer, and FIG. 6A is a schematic cross-sectional view of FIG. 5A after first etching of the isolation dielectric layer. FIG. 6B is a schematic cross-sectional view of FIG. 5A after first etching of the gate structure. FIG. 7A is a schematic cross-sectional view of FIG. 6A after etching of the isolation dielectric layer and the gate structure which are exposed through a mask opening. FIG. 7B is a schematic cross-sectional view of FIG. 4B after etching of the gate structure exposed through the mask opening.

[0042] In an implementation, as shown in FIG. 4A and FIG. 4B, a mask layer 160 is disposed on a side of the isolation dielectric layer 140 away from the substrate 110 and is provided with a mask opening 161, and an orthographic projection of the mask opening 161 on the substrate 110 is perpendicular to and partially overlaps an orthographic projection of the gate structure 120 on the substrate 110. Thus, a top wall of the isolation dielectric layer 140 and the top wall of the gate structure 120 may be partially exposed through the mask opening 161, so that the isolation dielectric layer 140 and the gate structure 120 may be etched through the mask opening 161.

[0043] At step S320, alternately and cyclically etching the isolation dielectric layer 140 and the gate structure 120 includes: as shown in FIG. 7A to FIG. 8B, alternately and cyclically performing an isolation dielectric layer etching step and a gate structure etching step until the gate structure 120 is cut off. Thus, the isolation dielectric layer 140 can be etched to a certain depth by performing the isolation dielectric layer etching step, and the gate structure

120 can be etched to a depth similar to an etching depth of the isolation dielectric layer 140 by performing the gate structure etching step. By cyclically performing the steps, the gate structure 120 can be accurately cut off, and the first isolation trench 171 with a high aspect ratio can be formed.

5 [0044] In an implementation, referring to a change of film layers shown in FIG. 4A and FIG. 5A, the mask layer 160 is disposed on the side of the isolation dielectric layer 140 away from the substrate 110, and the method for forming an isolation trench further includes:

10 before each time of alternately and cyclically performing the isolation dielectric layer etching step and the gate structure etching step, performing a sacrificial layer deposition step to form a sacrificial layer 180 on a side of the mask layer 160 away from the substrate 110; and the sacrificial layer 180 is consumed during the isolation dielectric layer etching step and the gate structure etching step, as shown in FIG. 6A and FIG. 6B.

[0045] Illustratively, referring to the change of the film layers shown in FIG. 4A and FIG. 5A and a change of film layers shown in FIG. 4B and FIG. 5B, an orthographic projection of the sacrificial layer 180 on the substrate 110 overlaps an orthographic projection of the mask layer 160 on the substrate 110, the sacrificial layer 180 is provided with an opening 181, which communicates with the mask opening 161, and an orthographic projection of the opening 181 of the sacrificial layer 180 on the substrate 110 overlaps the orthographic projection of the mask opening 161 on the substrate 110. In this way, plasma can enter the mask opening 161 through the opening 181 of the sacrificial layer 180 during the isolation dielectric layer etching step and the gate structure etching step, so as to contact the isolation dielectric layer 140 and the gate structure 120.

25 [0046] The isolation dielectric layer 140 may be made of silicon oxide (SiO_2), silicon nitride (SiN), or other silicide materials, and the mask layer 160 is usually made of silicon nitride (SiN). Since both the isolation dielectric layer 140 and the mask layer 160 are made of silicide materials which may be the same or similar, the mask layer 160 is consumed greatly when the isolation dielectric layer 140 is etched with an etching gas. For example, in practical applications, when the isolation dielectric layer 140 is made of a silicide material, a fluorine-containing gas is generally used to etch the isolation dielectric layer 140; due to a low selection ratio of the etching gas relative to silicon nitride, the mask layer 160 is consumed greatly during the etching of the isolation dielectric layer 140, resulting in

a failure to accurately transfer patterns such as the mask opening 161 to a subsequent etching process.

[0047] On this basis, referring to FIG. 5A, FIG. 6A, and FIG. 6B, with the sacrificial layer 180 formed on the side of the mask layer 160 away from the substrate 110, the sacrificial layer 180 is partially consumed during the isolation dielectric layer etching step, and is completely consumed after the gate structure etching step, so that the mask layer 160 can be protected by the consumption of the sacrificial layer 180 during the synchronous downward etching of the isolation dielectric layer 140 and the gate structure 120, and reduction in accuracy of transferring the patterns such as the mask opening 161 which is caused by excessive consumption of the mask layer 160 can be avoided. In addition, since the sacrificial layer 180 can protect the mask layer 160, the accuracy of transferring the patterns can be further improved by reducing a thickness of the mask layer 160.

[0048] Referring to FIG. 7A and FIG. 7B, after alternately and cyclically performing the isolation dielectric layer etching step and the gate structure etching step, the isolation dielectric layer 140 and the gate structure 120 which are exposed through the mask opening 161 are completely etched off to form the first isolation trench 171, and the mask opening 161 exposes the interlayer dielectric layer 130.

[0049] In an implementation, the number of cycles of the isolation dielectric layer etching step and the gate structure etching step is between 4 and 12. Illustratively, the number of cycles may be any one of 4, 6, 8, or 12. The number of cycles may be selected and adjusted based on a thickness of the gate structure 120. For example, when the thickness of the gate structure 120 is relatively large, the number of cycles may be set to 12; when the thickness of the gate structure 120 is relatively small, the number of cycles may be set to 4. It should be noted that the number of cycles may be selected and adjusted based on other factors, such as the thickness of the mask layer 160 and process parameters of a plasma etching device, but the embodiments of the present disclosure are not limited thereto.

[0050] FIG. 8A is a schematic cross-sectional view of FIG. 7A after etching of a part of the interlayer dielectric layer which is exposed through the mask opening. FIG. 8B is a schematic cross-sectional view of FIG. 7B after etching of the part of the interlayer dielectric layer which is exposed through the mask opening. FIG. 8A is a schematic cross-sectional view of FIG. 7A in a case where the second isolation trench is formed in the interlayer dielectric layer. FIG. 8B is a schematic cross-sectional view of FIG. 7B in a case where the second isolation trench is formed in the interlayer dielectric layer.

[0051] In an implementation, referring to FIG. 8A to FIG. 9B, at step S330, etching the portion 130A of the interlayer dielectric layer 130 which is exposed through the first isolation trench 171 includes: alternately and cyclically performing a sacrificial layer deposition step and an interlayer dielectric layer etching step until the interlayer dielectric layer 130 is etched to a target depth; and the sacrificial layer deposition step is to deposit the sacrificial layer 180 on the side of the mask layer 160 away from the substrate 110, the orthographic projection of the sacrificial layer 180 on the substrate 110 overlaps the orthographic projection of the mask layer 160 on the substrate 110, and the sacrificial layer 180 is configured to be consumed during the interlayer dielectric layer etching step. The target depth may be controlled by controlling the number of cycles of the sacrificial layer deposition step and the interlayer dielectric layer etching step and a thickness of the sacrificial layer 180.

[0052] At step S330, the sacrificial layer deposition step and the interlayer dielectric layer etching step are performed alternately, which facilitates formation of the second isolation trench 172 with a high aspect ratio inside the interlayer dielectric layer 130. Principles of formation and consumption of the sacrificial layer 180 are the same as those described in the above embodiment of step S320. Therefore, the principles can be found in the above embodiment of step S320, and will not be described here.

[0053] With the above technical solutions, by alternately and cyclically performing the sacrificial layer deposition step and the interlayer dielectric layer etching step to form the second isolation trench 172 with a high aspect ratio, it can be further ensured that the finally formed target isolation trench 170 meets a design requirement for high aspect ratio; moreover, during the downward etching of the interlayer dielectric layer 130, by protecting the mask layer 160 through the consumption of the sacrificial layer 180, the reduction in the accuracy of transferring the patterns such as the mask opening 161 caused by excessive consumption of the mask layer 160 can be avoided, which facilitates ensuring that the finally formed target isolation trench 170 meets the requirement for high aspect ratio.

[0054] In an implementation, the number of cycles of the sacrificial layer deposition step and the interlayer dielectric layer etching step is between 3 and 10. Illustratively, the number of cycles may be any one of 3, 5, 7, or 10. The number of cycles may be selected and adjusted based on a thickness of the interlayer dielectric layer 130, the thickness of the mask layer 160, and the process parameters of the plasma etching device, but the embodiments of the present disclosure are not limited thereto.

[0055] In an implementation, the sacrificial layer deposition step and the step of alternately and cyclically etching the isolation dielectric layer and the gate structure are performed in a same process chamber. For example, both the sacrificial layer deposition step and the step of alternately and cyclically etching the isolation dielectric layer and the gate structure may be performed in the process chamber 20 shown in FIG. 2.

[0056] It should be noted that different process steps in the related technology are generally performed in different process chambers, so that switching of the process chambers needs to be performed during execution of the process steps. However, during the switching of the process chambers, purging and vacuum evacuation need to be performed inside each process chamber, and a manipulator needs to be used to take the to-be-etched object out from one process chamber and then place the to-be-etched object into the other process chamber. The switching of the process chambers may reduce production capacity. Compared with the related technology, the embodiments of the present disclosure propose performing the sacrificial layer deposition step and the step of alternately and cyclically etching the isolation dielectric layer and the gate structure in the same process chamber, so that the operations related to the switching of the process chambers can be omitted, which facilitates improvement in the production capacity.

[0057] In an implementation, process conditions of the sacrificial layer deposition step include: a process gas including a silicon-containing gas, and the process gas further including at least one of an oxygen-containing gas or a nitrogen-containing gas.

[0058] For example, the process gas includes the silicon-containing gas and the oxygen-containing gas, then the silicon-containing gas and the oxygen-containing gas may react to form silicon oxide in the process chamber of the plasma etching device. Similarly, in a case where the process gas includes the silicon-containing gas and the nitrogen-containing gas, silicon nitride may be formed. In a case where the process gas includes the silicon-containing gas, the oxygen-containing gas, and the nitrogen-containing gas, silicon oxynitride may be formed. Each of silicon oxide, silicon nitride, and silicon oxynitride may be used as a material of the sacrificial layer.

[0059] In an implementation, referring to FIG. 10, the process conditions of the sacrificial layer deposition step further include: an upper electrode power range being 100 W-400 W, and a pressure range inside the process chamber 20 being 5 mTorr-30 mTorr.

[0060] Illustratively, as shown in FIG. 4A and FIG. 5A, during the deposition, by controlling a deposition rate, a deposition thickness, and a deposition position of the

sacrificial layer 180, it can be ensured that the formed sacrificial layer 180 meets process requirements.

[0061] Exemplarily, as for the deposition rate: if the deposition rate is too high, the formed sacrificial layer 180 can easily block the mask opening 161, resulting in poor uniformity and flatness of the sacrificial layer 180; if the deposition rate is too small, compactness of the sacrificial layer 180 is poor. In practical applications, when upper electrode power is in the range of 100 W-400 W (inclusive), the deposition rate of the sacrificial layer 180 is positively correlated with the upper electrode power; when a pressure inside the process chamber 20 is in the range of 5 mTorr-30 mTorr (inclusive), the deposition rate of the sacrificial layer 180 is positively correlated with the pressure inside the process chamber 20. Therefore, by setting the upper electrode power range to 100 W-400 W and setting the pressure range inside the process chamber 20 to 5 mTorr-30 mTorr, the deposition rate of the sacrificial layer 180 can be easily controlled to ensure that the sacrificial layer 180 is formed at a proper deposition rate, so that the sacrificial layer 180 can have good uniformity and flatness, and the mask opening 161 is not prone to blockage. Further, by controlling a bias power range to 1 W-100 W (inclusive), the compactness of the sacrificial layer 180 can be easily improved.

[0062] It should be noted that the deposition rate of the sacrificial layer 180 is also related to a flow rate and a ratio of the process gas and a deposition time, which will be illustrated below by an example.

[0063] The process conditions of the sacrificial layer deposition step include: the process gas including a silicon chloride gas (e.g., SiCl_4), oxygen (O_2), and helium (He), a flow range of the silicon chloride gas being 30 sccm-100 sccm, a flow range of the oxygen being 30 sccm-300 sccm, a range of a ratio of the silicon chloride gas to the oxygen being 1:1-1:3, and a flow range of the helium being 50 sccm-200 sccm; and a range of a deposition time being 10 s-30 s.

[0064] Illustratively, referring to FIG. 10, the to-be-etched object 100 is placed on the carrier 22 in the process chamber 20, and the carrier 22 absorbs the to-be-etched object 100. After the silicon chloride gas and the oxygen are introduced into the process chamber 20, a sacrificial layer of silicon dioxide is formed on the side of the mask layer 160 away from the substrate 110 under the action of plasma. A main reaction equation of the deposition is shown as the reaction equation (1) below:



[0065] Chlorine (Cl_2) is generated during the deposition as a by-product, and is pumped out from the process chamber 20.

[0066] In control of the process conditions, an inlet flow rate of the silicon chloride gas and the ratio of the silicon chloride gas to the oxygen are also positively correlated with the deposition rate of the sacrificial layer 180, that is, the larger the inlet flow rate of the silicon chloride gas is, the larger the ratio of the silicon chloride gas to the oxygen is, the higher the deposition rate of the sacrificial layer 180 is, the more likely the mask opening 161 is blocked. Therefore, by controlling the flow rate of the silicon chloride gas to be 30 sccm-100 sccm and controlling the ratio of the silicon chloride gas to the oxygen to be 1:1-1:3, it can be further ensured that the sacrificial layer 180 is formed at a proper deposition rate, so that the sacrificial layer 180 can have good uniformity and flatness, and the mask opening 161 is not prone to blockage. In addition, the helium introduced into the process chamber 20 is used as a diluent gas, and can also be used to control the deposition rate of the sacrificial layer 180. Therefore, forming the sacrificial layer 180 at a proper deposition rate can also be facilitated by controlling a range of an inlet flow rate of the helium to be 50 sccm-200 sccm.

[0067] As for the deposition thickness, in addition to controlling the silicon chloride gas, the oxygen, the helium, and the plasma etching device to meet the above conditions, the range of the deposition time also needs to be controlled to be 10 s-30 s. In this way, the sacrificial layer 180 can have a sufficient thickness without blocking the mask opening 161, which facilitates reducing the number of cycles of subsequent alternate etching of the isolation dielectric layer 140 and the gate structure 120, and also facilitates reducing the number of cycles of subsequent etching of the interlayer dielectric layer 130.

[0068] As for the deposition position, by controlling the silicon chloride gas, the oxygen, the helium, and the plasma etching device to meet the above conditions, deposition on a sidewall of the mask opening 161, deposition on the top wall of the isolation dielectric layer 140 which is exposed through the mask opening 161, and deposition on the top wall of the gate structure 120 which is exposed through the mask opening 161 can be reduced as much as possible, and deposition is mainly performed on a surface of the mask layer 160 away from the substrate 110, so that the desired sacrificial layer 180 is formed on the surface of the mask layer 160 away from the substrate 110.

[0069] In an implementation, referring to FIG. 5A and FIG. 6A, process conditions of the isolation dielectric layer etching step include: a process gas including a fluorine-containing

gas. Since most materials of the isolation dielectric layer 140 are silicide materials, a good etching effect on the isolation dielectric layer 140 can be produced by adopting the fluorine-containing gas as an etching gas. In an example, the process gas in the isolation dielectric layer etching step includes tetrafluoromethane (CF₄), perfluorobutadiene (C₄F₆), and argon (Ar), a flow range of the tetrafluoromethane is 5 sccm-50 sccm (inclusive), a flow range of the perfluorobutadiene is 30 sccm-200 sccm (inclusive), and a flow range of the argon is 100 sccm-300 sccm (inclusive); a pressure range inside the process chamber 20 is 5 mTorr-30 mTorr (inclusive); an upper electrode power range is 500 W-1000 W (inclusive); a lower electrode power range is 100 W-500 W (inclusive); and a range of an etching time is 5 s-30 s (inclusive).

[0070] The isolation dielectric layer etching step may include: performing vacuum evacuation inside of the process chamber 20 to maintain a pressure inside the process chamber 20 between 5 mTorr and 30 mTorr; introducing the tetrafluoromethane, the perfluorobutadiene, and the argon into the process chamber 20, with an inlet flow rate of the tetrafluoromethane being between 5 sccm and 50 sccm, an inlet flow rate of the perfluorobutadiene being between 30 sccm and 200 sccm, and an inlet flow rate of the argon being between 100 sccm and 300 sccm; controlling upper electrode power to be between 500 W and 1000 W to generate plasma, and controlling lower electrode power to be between 100 W and 500 W to guide the plasma to vertically bombard the exposed top wall of the isolation dielectric layer 140 through the mask opening 161 to etch the isolation dielectric layer 140; and maintaining the etching time between 5 s and 30 s to produce the desired etching effect.

[0071] Since the isolation dielectric layer 140 is typically made of silicon dioxide, the adoption of the tetrafluoromethane and the perfluorobutadiene as the etching gas can meet etching requirements of the isolation dielectric layer 140. The argon is used as a carrier gas and a diluent gas; and due to a relatively large molecular weight, the argon can promote ionization of the plasma and improve a vertical bombardment capability of the plasma.

[0072] The upper electrode power is configured to control a proportion of the ionized etching gas, and the higher the upper electrode power, the larger the proportion of the ionized etching gas, and the higher the density of the plasma. The lower electrode power is configured to control a bombardment capability of the plasma, and the higher the lower electrode power, the higher the acceleration obtained by the plasma, and the more intense the vertical bombardment on the top wall of the isolation medium layer 140.

[0073] With the above technical solutions, by controlling the process parameters of the isolation dielectric layer etching step to meet the above conditions, etching morphology of the first isolation trench 171 can be controlled to enable the first isolation trench 171 to meet the design requirement for high aspect ratio.

5 [0074] In an implementation, referring to FIG. 6A and FIG. 6B, process conditions of the gate structure etching step include: a process gas including a chlorine-containing gas. Since the gate structure 120 may be made of a metal material, the adoption of the chlorine-containing gas as an etching gas for the gate structure 120 can meet etching requirements of the gate structure 120 to produce a good etching effect.

10 [0075] Illustratively, the process gas includes chlorine (Cl_2), boron trichloride (BCl_3), and nitrogen (N_2), a flow range of the chlorine and a flow range of the boron trichloride are both 30 sccm-150 sccm (inclusive), and a flow range of the nitrogen is 5 sccm-100 sccm (inclusive); a pressure range inside the process chamber 20 is 5 mTorr-30 mTorr (inclusive); an upper electrode power range is 500 W-1000 W (inclusive); a lower electrode power
15 range is 100 W-500 W (inclusive); and a range of an etching time is 5 s-30 s (inclusive). It should be noted that the gate structure etching step is similar to the isolation dielectric layer etching step, so that reference can be made to the above embodiments of the isolation dielectric layer etching step for a specific implementation of the gate structure etching step, and the specific implementation will not be described here.

20 [0076] Illustratively, the gate structure 120 may include a metal gate layer 121 and a high-K dielectric layer 122, the high-K dielectric layer 122 is located between the metal gate layer 121 and the substrate 110, the interlayer dielectric layer 130, and the isolation dielectric layer 140. A material of the metal gate layer 121 includes, but is not limited to, aluminum (Al), titanium nitride (TiN), titanium (Ti), and tungsten (W) among other metal
25 materials, and a material of the high-K dielectric layer 122 includes, but is not limited to, hafnium dioxide (HfO_2). The metal gate layer 121 may be etched by taking the chlorine and the boron trichloride as an etching gas. Since the boron trichloride has a strong bombardment effect, the high-K dielectric layer 122 can be bombarded and etched during the etching of the metal gate layer 121, which produces an effect of simultaneously etching
30 the metal gate layer 121 and the high-K dielectric layer 122. In addition, due to a high selection ratio of the chlorine to the sacrificial layer 180, less of the sacrificial layer 180 is consumed in the gate structure etching step than in the isolation dielectric layer etching step.

[0077] With the above technical solutions, by controlling the gate structure etching step to meet the above conditions, the etching morphology of the first isolation trench 171 can be controlled to enable the first isolation trench 171 to meet the design requirement for high aspect ratio.

5 [0078] In an implementation, referring to FIG. 8A to FIG. 9B and FIG. 10, the interlayer dielectric layer etching step is performed in the plasma etching device, and process conditions of the interlayer dielectric layer etching step include: a process gas including a fluorine-containing gas. Since most materials of the interlayer dielectric layer 130 are silicide materials, a good etching effect on the interlayer dielectric layer 130 can be
10 produced by adopting the fluorine-containing gas as an etching gas.

[0079] Illustratively, the process gas includes tetrafluoromethane, perfluorobutadiene, argon, and oxygen, a flow range of the tetrafluoromethane is 5 sccm-50 sccm (inclusive), a flow range of the perfluorobutadiene is 30 sccm-200 sccm (inclusive), a flow range of the argon is 100 sccm-300 sccm (inclusive), and a flow range of the oxygen is 5 sccm-30 sccm
15 (inclusive); a pressure range inside the process chamber 20 is 5 mTorr-30 mTorr (inclusive); an upper electrode power range is 500 W-1000 W (inclusive); a lower electrode power range is 100 W-500 W (inclusive); and a range of an etching time is 5 s-30 s (inclusive). It should be noted that the interlayer dielectric layer etching step is similar to the isolation dielectric layer etching step, so that reference can be made to the above embodiments of the
20 isolation dielectric layer etching step for a specific implementation of the interlayer dielectric layer etching step, and the specific implementation will not be described here.

[0080] Compared with the isolation dielectric layer etching step, in the above example, the oxygen is further introduced into the process chamber 20 in the interlayer dielectric layer etching step; and by controlling a range of an inlet flow rate of the oxygen to be 5 sccm-30
25 sccm, deposition of a by-product on a sidewall of the first isolation trench 171 can be prevented, and it can be ensured that the plasma enters the first isolation trench 171 through the mask opening 161 and contacts the interlayer dielectric layer 130, so as to etch the interlayer dielectric layer 130 to form the second isolation trench 172.

[0081] With the above technical solutions, by controlling the interlayer dielectric layer
30 etching step to meet the above conditions, etching morphology of the second isolation trench 172 can be controlled to ensure that the formed second isolation trench 172 meets the design requirements.

[0082] It should be noted that the isolation dielectric layer etching step, the gate structure etching step, and the interlayer dielectric layer etching step are all performed in the plasma etching device, which facilitates simplifying process steps, thereby improving etching efficiency.

5 [0083] In an implementation, referring to FIG. 3A to FIG. 3C, the to-be-etched object 100 further includes a plurality of discrete fins 150 located between the substrate 110 and the gate structure 120, the plurality of fins 150 extend along the second direction D2, and the gate structure 120 spans the plurality of fins 150 and covers a portion of a top wall and a portion of a sidewall of each fin 150. Forming the first isolation trench 171 includes:
10 forming the first isolation trench 171 between adjacent fins 150.

[0084] In an example, the number of gate structures 120 may be one, and the first isolation trench 171 formed between the adjacent fins 150 may divide the one gate structure 120 into two gates 120A, thereby forming two independent FinFETs.

[0085] In another example, the number of gate structures 120 may be more than one (i.e.,
15 two or more), a plurality of gate structures 120 are spaced apart and extend along the first direction D1, and each gate structure 120 spans the plurality of fins 150 and partially covers a portion of the top wall and a portion of the sidewall of each fin 150. The first isolation trench 171 formed between the adjacent fins 150 may simultaneously penetrate through the plurality of gate structures 120 along the second direction D2 to divide each gate structure
20 120 into two gates 120A. Therefore, the plurality of gate structures 120 can be cut off at a time, which facilitates improvement in formation efficiency of the gates 120A.

[0086] With the above technical solutions, by forming the first isolation trench 171 between the adjacent fins 150, the method for forming an isolation trench is suitable for a manufacturing scenario of a FinFET.

25 [0087] The present disclosure further provides a manufacturing method for a semiconductor device, including: forming a plurality of semiconductor devices, with gate structures of the plurality of semiconductor devices connected to each other; and cutting off the gate structures of adjacent semiconductor devices with the method for forming an isolation trench provided in any of the above implementations to make the gate structures into a
30 plurality of gates, with the plurality of gates in one-to-one correspondence with the plurality of semiconductor devices. Since the manufacturing method for a semiconductor device adopts all the technical solutions provided in all the above embodiments, the manufacturing method for a semiconductor device at least has all the beneficial effects of

the technical solutions provided in the above embodiments, and thus the beneficial effects will not be described in detail here.

[0088] FIG. 10 is a schematic structural diagram of a semiconductor process device according to an embodiment of the present disclosure.

5 [0089] As shown in FIG. 10, the semiconductor process device 200 includes the process chamber 20, a gas inlet assembly 20A, a gas exhaust assembly (not shown in FIG. 10), an upper electrode assembly 20B, a lower electrode assembly 20C, and a controller (not shown in FIG. 10). The controller includes at least one processor and at least one storage device, and the at least one storage device has stored therein a computer program which, when
10 executed by the processor, implements the method provided in any one of the above implementations.

[0090] Illustratively, the controller may be an upper computer or a lower computer. The controller may control a valve of the gas inlet assembly 20A to open to introduce a corresponding process gas into the process chamber 20; and the controller may further
15 control opening of the valve of the gas inlet assembly 20A to control a flow rate of the process gas. The controller may further control a pressure inside the process chamber 20 by controlling the gas exhaust assembly to evacuate the process chamber 20.

[0091] The upper electrode assembly 20B includes the RF coil 21, the upper RF power supply 23, and the upper matcher 25. The controller is further configured to control the
20 upper RF power supply 23 to supply upper electrode power to the RF coil 21 through the upper matcher 25, so as to enable the RF coil 21 to excite the process gas in the process chamber 20 to generate plasma.

[0092] The lower electrode assembly 20C includes the carrier 22, the lower RF power supply 24, and the lower matcher 26. The controller is further configured to control the
25 lower RF power supply 24 to supply lower electrode power to a lower electrode of the carrier 22 through the lower matcher 26, so that the lower electrode of the carrier 22 may supply RF bias voltage to attract the plasma above the to-be-etched object 100 to bombard the to-be-etched object 100.

[0093] The semiconductor process device 200 according to the embodiment of the present
30 disclosure may be an ICP etching device or a Capacitively Coupled Plasma (CCP) etching device. A type of the semiconductor process device 200 is not limited in the embodiment of the present disclosure.

[0094] In addition, in the present disclosure, unless expressly stated and limited otherwise, the terms, “couple”, “connect”, and “overlap” should be understood broadly, for example, the terms may refer to fixed connection, detachable connection, or integration; and the terms may refer to direct connection, indirect connection through an intermediate medium, communication between interiors of two elements, or an interaction relationship between two elements. The specific meanings of the above terms in the present disclosure can be understood by those of ordinary skill in the art according to specific cases.

[0095] In the description, the reference terms such as “an embodiment”, “some embodiments”, “an example”, “a specific example” and “some examples” are intended to indicate that the specific features, structures, materials or characteristics described in conjunction with the embodiment(s) or example(s) are included in at least one embodiment or example of the present disclosure. Moreover, the specific features, structures, materials or characteristics described can be combined in any suitable way in any one or more embodiments or examples. Further, those of ordinary skill in the art can combine the different embodiments or examples and the features therein which are described in the description if no conflict is incurred. In addition, the terms “first” and “second” are just for the purpose of description, and should not be understood as indicating or implying relative importance or implicitly indicating the number of the indicated technical features. Thus, a feature defined by “first” or “second” may explicitly or implicitly include at least one feature. In the description of the present disclosure, “a plurality” means two or more, unless otherwise stated.

[0096] What is described above is just the preferable embodiments of the present disclosure, and is not intended to limit the present disclosure. Any modification and equivalent substitution made within the spirit and the principle of the present disclosure should be included in the scope of the present disclosure.

What is claimed is:

1. A method for forming an isolation trench, comprising:

providing a to-be-etched object, which comprises a substrate, a gate structure, and
5 an isolation dielectric layer, the gate structure and the isolation dielectric layer being
located on a surface of the substrate, and the gate structure extending along a first
direction and being disposed on a same layer as the isolation dielectric layer; and

alternately and cyclically etching the isolation dielectric layer and the gate
structure to form a first isolation trench, the first isolation trench penetrating through the
10 gate structure along a second direction, and the first direction being perpendicular to the
second direction;

wherein, in each cycle, the isolation dielectric layer is etched by a predetermined
depth to expose a part of the gate structure, and then the exposed part of the gate
structure is etched to make a top surface of the gate structure substantially flush with a
15 top surface of the isolation dielectric layer.

2. The method of claim 1, wherein the to-be-etched object further comprises an
interlayer dielectric layer located between the substrate and the gate structure, and the
first isolation trench exposes a top wall of the interlayer dielectric layer; and after
20 forming the first isolation trench, the method further comprises:

etching a portion of the interlayer dielectric layer which is exposed through the
first isolation trench to form a second isolation trench, the first isolation trench and the
second isolation trench communicating with each other to form a target isolation trench.

3. The method of claim 1, wherein alternately and cyclically etching the isolation
dielectric layer and the gate structure comprises: alternately and cyclically performing
an isolation dielectric layer etching step and a gate structure etching step until the gate
structure is cut off.

4. The method of claim 3, wherein a mask layer is disposed on a side of the
isolation dielectric layer away from the substrate, and the method further comprises:

before each time of alternately and cyclically performing the isolation dielectric
layer etching step and the gate structure etching step, performing a sacrificial layer

deposition step to form a sacrificial layer on a side of the mask layer away from the substrate; and the sacrificial layer is consumed during the isolation dielectric layer etching step and the gate structure etching step.

5 5. The method of claim 2, wherein a mask layer is disposed on a side of the isolation dielectric layer away from the substrate, the mask layer is provided with a mask opening, and an orthographic projection of the mask opening on the substrate is perpendicular to and partially overlaps an orthographic projection of the gate structure on the substrate; and

10 etching the interlayer dielectric layer comprises: alternately and cyclically performing a sacrificial layer deposition step and an interlayer dielectric layer etching step until the interlayer dielectric layer is etched to a target depth; and the sacrificial layer deposition step is to deposit a sacrificial layer on a side of the mask layer away from the substrate, and the sacrificial layer is consumed during the interlayer dielectric
15 layer etching step.

 6. The method of claim 4 or 5, wherein the sacrificial layer deposition step and alternately and cyclically etching the isolation dielectric layer and the gate structure are performed in a same process chamber.

20 7. The method of claim 6, wherein process conditions of the sacrificial layer deposition step comprise: a process gas comprising a silicon-containing gas, and the process gas further comprising at least one of an oxygen-containing gas or a nitrogen-containing gas.

25 8. The method of claim 7, wherein the process conditions of the sacrificial layer deposition step further comprise: an upper electrode power range being between 100 W and 400 W, and a pressure range inside the process chamber being between 5 mTorr and 30 mTorr.

30 9. The method of claim 3, wherein process conditions of the isolation dielectric layer etching step comprise a process gas comprising a fluorine-containing gas; and/or,

process conditions of the gate structure etching step comprise a process gas comprising a chlorine-containing gas.

10. The method of claim 9, wherein the fluorine-containing gas comprises
5 tetrafluoromethane and perfluorobutadiene; and/or, the chlorine-containing gas comprises boron trichloride and chlorine.

11. The method of claim 1, wherein the to-be-etched object comprises a plurality
of discrete fins located between the substrate and the gate structure, the plurality of fins
10 extends along the second direction, and the gate structure spans the plurality of fins and covers a portion of a top wall and a portion of a sidewall of each fin; and

forming the first isolation trench comprises: forming the first isolation trench
between adjacent fins.

12. A manufacturing method for a semiconductor device, comprising:
15 forming a plurality of semiconductor devices, gate structures of the plurality of semiconductor devices being connected to each other; and
cutting off the gate structures of adjacent semiconductor devices with the method
for forming an isolation trench of any one of claims 1 to 11, so as to make the gate
20 structures into a plurality of gates.

13. A semiconductor process device, comprising: a process chamber, a gas inlet
assembly, an upper electrode assembly, a lower electrode assembly, and a controller, the
controller comprising at least one processor and at least one storage device, and the at
25 least one storage device having stored therein a computer program which, when
executed by the at least one processor, implements the method of any one of claims 1 to
11.