ABSTRACT

A semiconductor device and a fabrication method thereof are disclosed. The device includes a substrate including an active pattern, a channel pattern on the active pattern, the channel pattern including a plurality of vertically-stacked semiconductor patterns, a source/drain pattern connected to the semiconductor patterns, a gate electrode on the semiconductor patterns, the gate electrode including a first portion interposed between first and second semiconductor patterns, which are two adjacent ones of the semiconductor patterns, and a gate insulating layer interposed between the first portion of the gate electrode and the first and second semiconductor patterns. The second semiconductor pattern is located at a tier higher than the first semiconductor pattern. The first semiconductor pattern includes a first channel recess having a first depth, and the second semiconductor pattern includes a second channel recess having a second depth smaller than the first depth.

FIG. 6A