

Title

METHOD FOR FABRICATING TRANSISTOR

5 Background of the Invention

1. Field of the Invention

The present invention relates generally to a method for fabricating semiconductor devices. More particularly, the present invention relates
10 to a method for fabricating a metal-oxide-semiconductor (MOS) transistor by utilizing poly shadow effect (or gate shadow effect) and two-stage LDD/pocket implant.

2. Description of the Prior Art

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Semiconductor devices are continually getting smaller, faster and requiring less power. There is a need in the industry for smaller and faster MOS transistors used to provide the core functionality of the integrated circuits used in the semiconductor devices. Gate oxide
20 thickness, junction scaling, and well engineering in MOS devices has enabled channel length scaling by improving short channel characteristics. It is known that by changing the doping profile in the channel region, the distribution of the electric field and potential contours can be changed.

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In order to reduce the overlap between a lightly doped drain (LDD) or source/drain extension area and the gate electrode, which benefits high device speed, an offset spacer is typically provided on the vertical sidewalls of the gate electrode. This offset spacer is also known as
30 spacer-1 in the art. However, the processing steps of depositing and etching the offset spacer may induce defect problems such as particle, polymer and so on.

Halo or Pocket implants have been used as a means to scale the channel
35 length and increase the transistor drive current without causing an increase in the off-state leakage current. Halos are generally known for their ability to stop unwanted source/drain leakage conduction or

punch-through current. A large-tilt-angle implant can be used to fabricate halo-type structures, usually with the use of a side spacer to protect the gate structure from unwanted dopant contamination. A quad high-angle (QHA) implant is typically used to form the halo structures in the transistor, wherein four separate high angle implants are done on the device wafer, each implant performed on the wafer held in a position, then rotationally indexed by 90 degrees.

Although the QHA implant beneficially permits implantation of dopant underlying the gate structure, the gate structure, STI, and the photoresist also shield some areas of the semiconductor substrate from being implanted at one or more of the four implant angles. . Further, the bulk of the implant is received in other unwanted open areas (e.g., in the source/drain regions). Dopant received in these unwanted areas increases junction capacitance and may cause body leakage, resulting in reduced switching speeds and higher Rsd. The unwanted areas (e.g., in the source/drain regions) receive higher concentration than that underlying gate, which is harmful for device performance. In light of the above, there is a need in this industry to provide an improved method for fabricating a MOS transistor without over doping the unwanted area in the source/drain area, thereby improving device performance.

Summary of the Invention

One objective of the present invention is to provide a method for fabricating a metal-oxide-semiconductor (MOS) transistor that is capable of avoiding the above-mentioned prior art problems.

According to the claimed invention, in one aspect, a method for fabricating a transistor includes providing a gate electrode on a main surface of a semiconductor substrate; masking a drain-forming region on one side of the gate electrode with a first photoresist pattern; performing a first lightly doped drain (LDD) implant with a tilt angle to dope a source-forming region on the other side of the gate electrode, thereby forming a first LDD region therein; stripping the first photoresist pattern; masking the source-forming region with a second photoresist pattern; and performing a second LDD implant with the tilt

angle to dope the drain-forming region, thereby forming a second LDD region therein.

From another aspect of the invention, a method for fabricating a transistor includes providing a gate electrode on a main surface of a semiconductor substrate; masking a drain-forming region on one side of the gate electrode with a first photoresist pattern; performing a first lightly doped drain (LDD) implant with a first tilt angle and a first twist angle to dope a source-forming region on the other side of the gate electrode, thereby forming a first LDD region therein; performing a first pocket implant with a second tilt angle and a second twist angle to dope the source-forming region, thereby forming a first pocket region in the semiconductor substrate; stripping the first photoresist pattern; masking the source-forming region with a second photoresist pattern; performing a second LDD implant with the first tilt angle and the first twist angle to dope the drain-forming region, thereby forming a second LDD region therein; and performing a second pocket implant with the second tilt angle and the second twist angle to dope the drain-forming region, thereby forming a second pocket region in the semiconductor substrate.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

FIGS. 1-7 are schematic, cross-sectional diagrams showing an exemplary method for fabricating a MOS transistor by utilizing poly shadowing effect and two-stage LDD/pocket implant in accordance with one embodiment of this invention.

Detailed Description

The present invention has been particularly shown and described with respect to certain embodiments and specific features thereof. The embodiments set forth hereinbelow are to be taken as illustrative rather

than limiting. It should be readily apparent to those of ordinary skill in the art that various changes and modifications in form and detail may be made without departing from the spirit and scope of the invention.

5 FIGS. 1-7 are schematic, cross-sectional diagrams showing an exemplary method for fabricating a metal-oxide-semiconductor (MOS) transistor in accordance with one embodiment of this invention. As shown in FIG. 1, a semiconductor substrate 10 is provided. The semiconductor substrate 10 may include but not limited to silicon
10 substrate, silicon substrate with an epitaxial layer, SiGe substrate, silicon-on-insulator (SOI) substrate, gallium arsenide (GaAs) substrate, gallium arsenide-phosphide (GaAsP) substrate, indium phosphide (InP) substrate, gallium aluminum arsenic (GaAlAs) substrate, or indium gallium phosphide (InGaP) substrate. Optionally, an ion well (not
15 explicitly shown) such as N well or P well may be formed in the semiconductor substrate 10 in some cases. For example, a PMOS transistor device is typically fabricated in an N well.

A gate electrode 12 having a gate length L and height H is provided on a
20 main surface 10a of the semiconductor substrate 10. The gate electrode 12 may include but not limited to polysilicon, metal, composite metal or silicide. A cap layer (not explicitly shown) such as silicon nitride cap may be provided as a part of the gate electrode 12 in some embodiments. A gate dielectric layer 14 such as silicon dioxide or high- k material may
25 be interposed between the gate electrode 12 and the main surface 10a of the semiconductor substrate 10. On two opposite sides of the gate electrode 12, there are source-forming region 202 and drain-forming region 204. Shallow trench isolation (STI) region 11 may be provided to surround and isolate an active area that includes the source-forming
30 region 202 and the drain-forming region 204.

As shown in FIG. 2, subsequently, a photoresist pattern 16 is formed on the semiconductor substrate 10 and partially overlaps with the gate electrode 12. Preferably, the width w_1 (in source-drain direction) of the
35 overlapping portion 16a of the photoresist pattern 16 that overlaps with the gate electrode 12 may range between $L/5 \sim L/2$. The photoresist pattern 16 has an opening 16b that exposes the entire, or at least a

portion of, source-forming region 202. Preferably, the entire drain-forming region 204 and a portion of the STI region 11 is covered by the photoresist pattern 16. It is noteworthy that, at this point, no offset spacer is formed on two opposite sidewalls of the gate electrode 12.

Thereafter, a lightly doped drain (LDD) implant 20 is carried out to form a first LDD region 120 in the exposed source-forming region 202. The first LDD region 120 can be kept a prescribed distance or an offset d from an edge of the gate electrode 12 because of the poly shadowing effect of the gate electrode 12. According to the embodiment of this invention, the LDD implant 20 is performed with a tilt angle θ_1 of about 8° from a vertical axis 101 and with a twist angle of 45° from a reference direction. However, it is to be understood that the tilt angle θ_1 of the LDD implant 20 may vary depending upon the height H of the gate electrode 12 in order to acquire the desired offset d .

It is advantageous to use the present invention because by taking advantage of the poly shadow effect, a conventional offset spacer (spacer-1) can be omitted and the potential defects that stems from the deposition and/or etching of the offset spacer can be avoided. Further, it is to be understood that in one wafer (substrate) there may be gate electrodes disposed in orthogonal orientation with respect to each other, so it is necessary, in this circumstance, to satisfy gate electrodes in both directions by implanting respectively.

As shown in FIG. 3, a pocket implant 30 is then carried out to place a packet region 130 around one edge of the gate electrode 12 in the exposed source-forming region 202 of the semiconductor substrate 10 and underlying a portion of the gate electrode 12. According to the embodiment of this invention, the pocket implant 30 may be performed with a tilt angle θ_2 of about 30° from a vertical axis 101 and with a twist angle of 45° from a reference direction. However, it is to be understood that the tilt angle θ_2 of the pocket implant 30 may vary depending upon the requirements of the processes and devices. After the pocket implant 30, the photoresist pattern 16 is stripped off.

As shown in FIG. 4, subsequently, a photoresist pattern 26 is formed on the semiconductor substrate 10 and partially overlaps with the gate electrode 12. Preferably, the width w_2 (in source-drain direction) of the overlapping portion 26a of the photoresist pattern 26 that overlaps with the gate electrode 12 may range between $L/5 \sim L/2$. The photoresist pattern 26 has an opening 26b that exposes the entire, or at least a portion of, drain-forming region 204. Preferably, the entire source-forming region 202 and a portion of the STI region 11 is covered by the photoresist pattern 26. Still, no offset spacer is formed on two opposite sidewalls of the gate electrode 12 at this point.

Thereafter, an LDD implant 40 is carried out to form a second LDD region 140 in the exposed drain-forming region 204. Likewise, the second LDD region 140 can be kept a prescribed distance or an offset d from an edge of the gate electrode 12 because of the poly shadowing effect of the gate electrode 12. According to the embodiment of this invention, the LDD implant 40 is performed with a tilt angle θ_1 of about 8° from a vertical axis 101 and with a twist angle of 45° from a reference direction. It is to be understood that the tilt angle θ_1 of the LDD implant 40 may vary depending upon the height H of the gate electrode 12 in order to acquire the desired offset d .

As shown in FIG. 5, a pocket implant 50 is then carried out to place a packet region 150 around the other edge of the gate electrode 12 in the exposed drain-forming region 204 of the semiconductor substrate 10 and underlying a portion of the gate electrode 12. According to the embodiment of this invention, the pocket implant 50 may be performed with a tilt angle θ_2 of about 30° from a vertical axis 101 and with a twist angle of 45° from a reference direction. However, it is to be understood that the tilt angle θ_2 of the pocket implant 50 may vary depending upon the requirements of the processes and devices. While the method of the invention herein is described as a series of steps or events, it will be appreciated that the present invention is not limited by the illustrated ordering of such steps or events. After the pocket implant 50, the photoresist pattern 26 is stripped off.

As shown in FIG. 6, a pair of sidewall spacers 62 such as silicon oxide

spacer or silicon nitride spacer may be formed on two opposite sidewalls of the gate electrode 12. The formation of the sidewall spacers 62 is well known in the art. For example, a chemical vapor deposition (CVD) is performed to deposit a conformal layer of dielectric such as silicon oxide or silicon nitride, followed by an anisotropic dry etching process to etch the conformal layer of dielectric until the source-forming region 202 and the drain-forming region 204 of the semiconductor substrate 10 are exposed.

As shown in FIG. 7, using the gate electrode 12 and the sidewall spacers as a mask, a source/drain implant 80 is carried out to form a heavily doped source region 220 in the source-forming region 202 and a heavily doped drain region 240 in the drain-forming region 204. A salicide process may be performed thereafter to form salicide (not shown) on the source-forming region 202 and the drain-forming region 204.

It is advantageous to use the present invention method because no offset spacer is required during the formation of the LDD region of the transistor. By skipping the deposition and etching steps used to form the conventional offset spacer, the possibility of generating process defect is decreased. Besides, the open area in the source-forming region 202 and the drain-forming region 204 only receives 1/4 dose of the pocket implant, whereby the quiescent current leakage current (I_{DDQ}) characteristic can be improved.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention.

Claims:

1. A method for fabricating a transistor, comprising:
providing a gate electrode on a main surface of a semiconductor
5 substrate;
masking a drain-forming region on one side of the gate electrode
with a first photoresist pattern;
performing a first lightly doped drain (LDD) implant with a first tilt
angle and a first twist angle to dope a source-forming region on the
10 other side of the gate electrode, thereby forming a first LDD region
therein;
performing a first pocket implant with a second tilt angle and a
second twist angle to dope the source-forming region, thereby forming
a first pocket region in the semiconductor substrate; and
15 stripping the first photoresist pattern.
2. The method for fabricating a transistor according to claim 1
wherein the first photoresist pattern partially overlaps with the gate
electrode.
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3. The method for fabricating a transistor according to claim 1
wherein the first tilt angle is about 8° from vertical.
4. The method for fabricating a transistor according to claim 1
25 wherein the first twist angle is 45°.
5. The method for fabricating a transistor according to claim 1
wherein the second tilt angle is about 30° from vertical.
- 30 6. The method for fabricating a transistor according to claim 1
wherein the second twist angle is 45°.
7. The method for fabricating a transistor according to claim 1
wherein the first LDD implant is shadowed by the gate electrode.
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8. The method for fabricating a transistor according to claim 1 further
comprising the steps of:

masking the source-forming region with a second photoresist pattern;

performing a second LDD implant with the first tilt angle and the first twist angle to dope the drain-forming region, thereby forming a second LDD region therein; and

performing a second pocket implant with the second tilt angle and the second twist angle to dope the drain-forming region, thereby forming a second pocket region in the semiconductor substrate.

9. The method for fabricating a transistor according to claim 8 wherein the second photoresist pattern partially overlaps with the gate electrode.

10. The method for fabricating a transistor according to claim 8 wherein the first tilt angle is about 8° from vertical.

11. The method for fabricating a transistor according to claim 8 wherein the first twist angle is 45°.

12. The method for fabricating a transistor according to claim 8 wherein the second tilt angle is about 30° from vertical.

13. The method for fabricating a transistor according to claim 8 wherein the second twist angle is 45°.

14. The method for fabricating a transistor according to claim 8 wherein the second LDD implant is shadowed by the gate electrode.

15. The method for fabricating a transistor according to claim 8 wherein after the second LDD implant, the second photoresist pattern is stripped.

16. The method for fabricating a transistor according to claim 8 wherein after the second photoresist pattern is stripped, a pair of sidewall spacers are formed on two opposite sidewalls of the gate electrode.

17. The method for fabricating a transistor according to claim 16 wherein after forming the sidewall spacers, heavily doped source and drain regions are formed on two sides of the gate electrode.