
对半导体叠层结构执行第一刻蚀工艺，以形成多个相互间隔的鳍形结构
S101
对鳍形结构执行第二刻蚀工艺，以选择性地刻蚀第一半导体层与第二半导体层中的一者的至少部分
S102

图 1

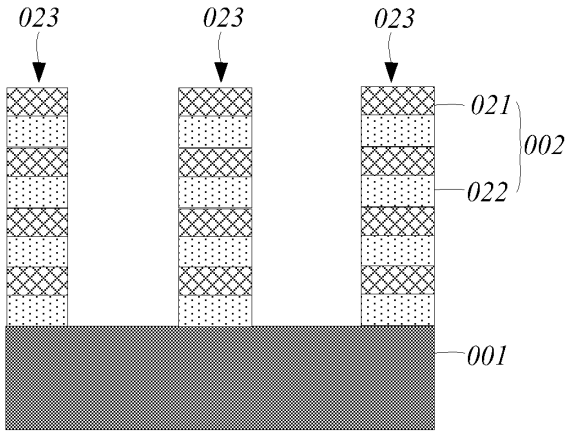

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图 2

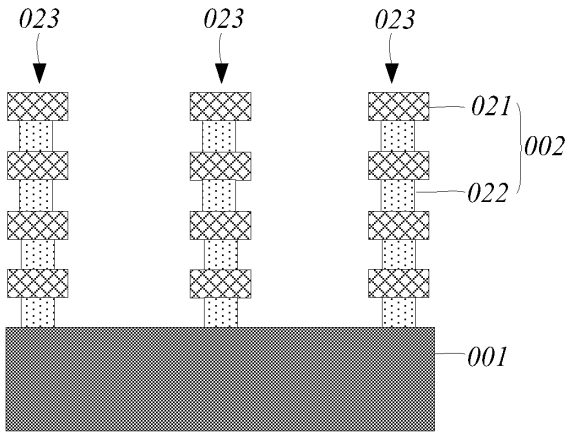

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图 3

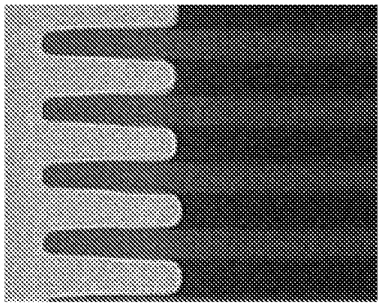


图 4

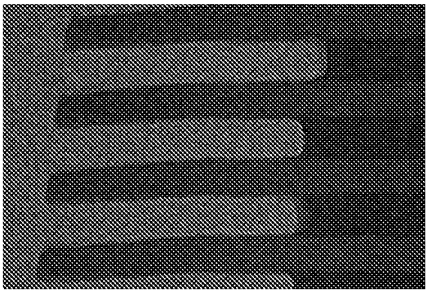


图 5

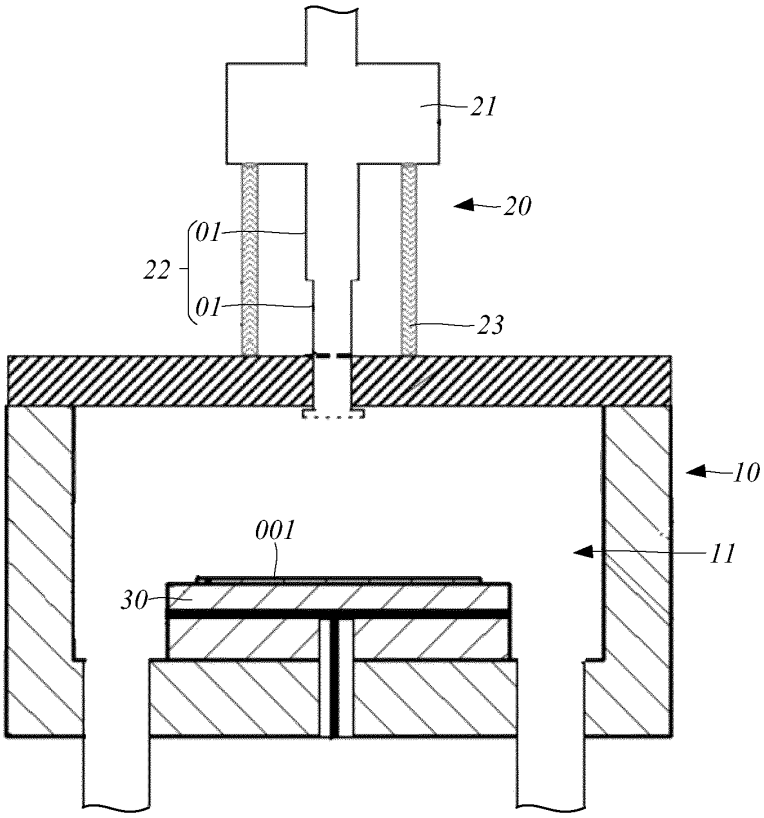


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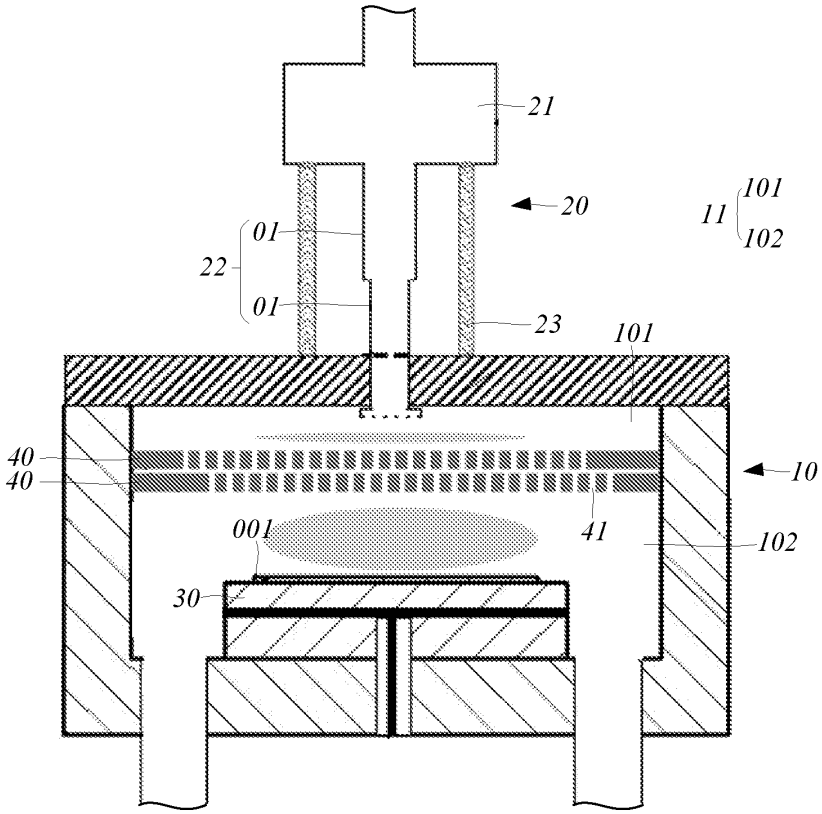

21
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图 7

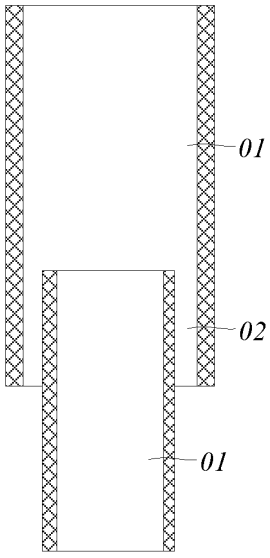

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图 8

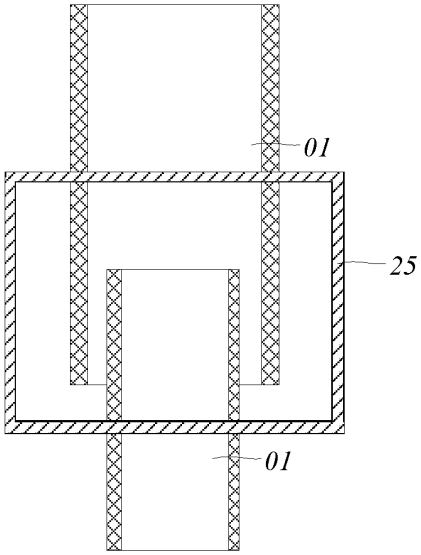

01
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图 9

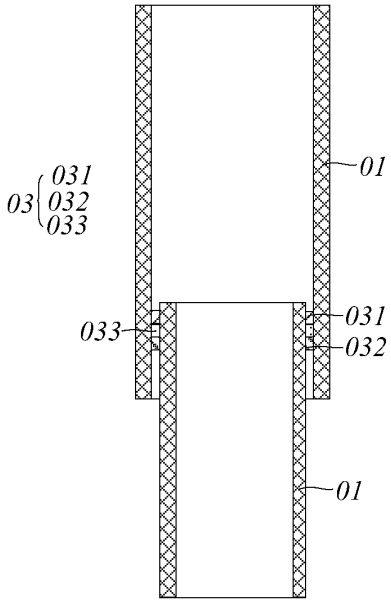

031
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图 10

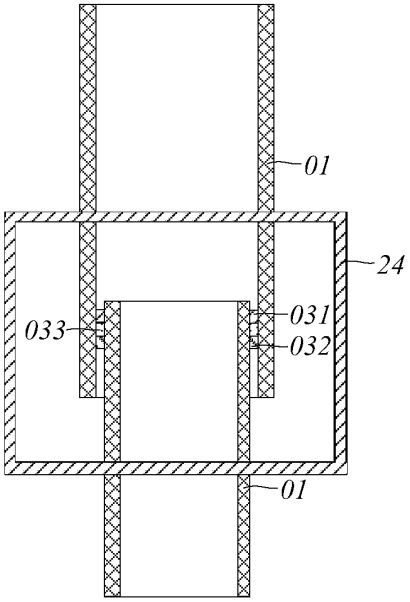

01
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图 11

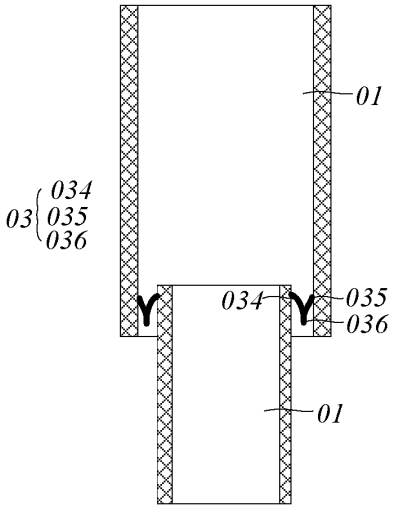

034
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图 12

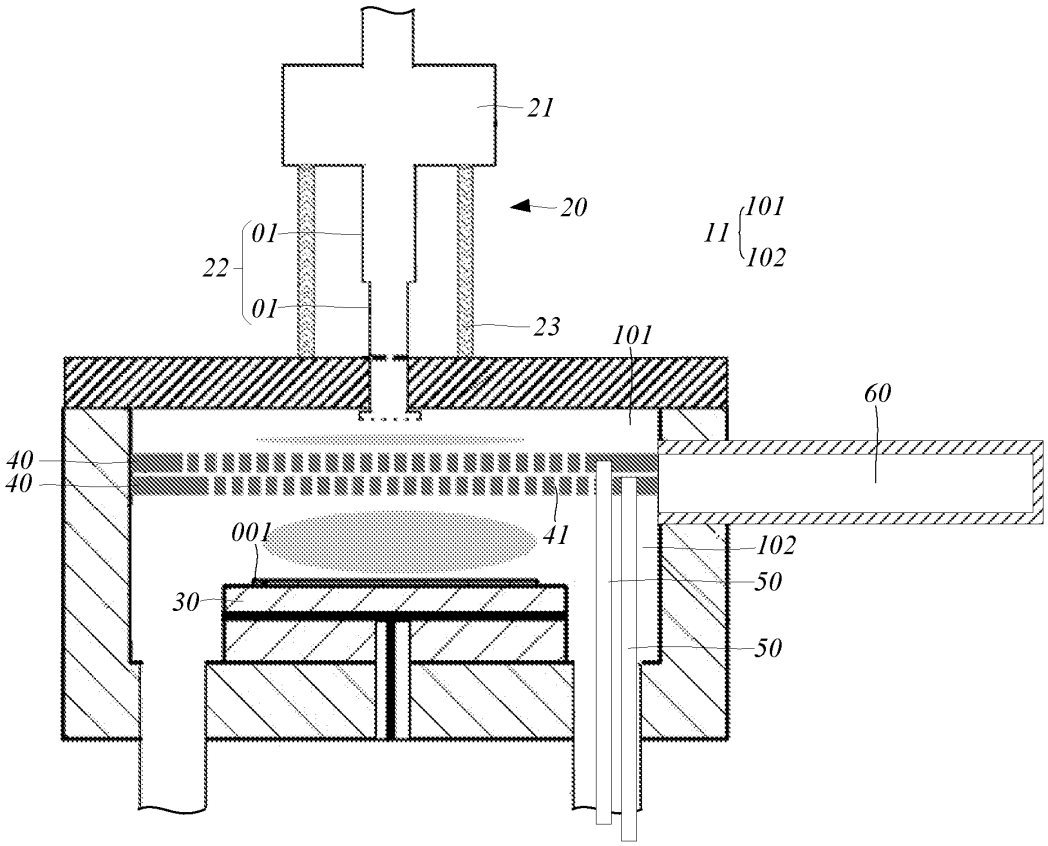


图 13

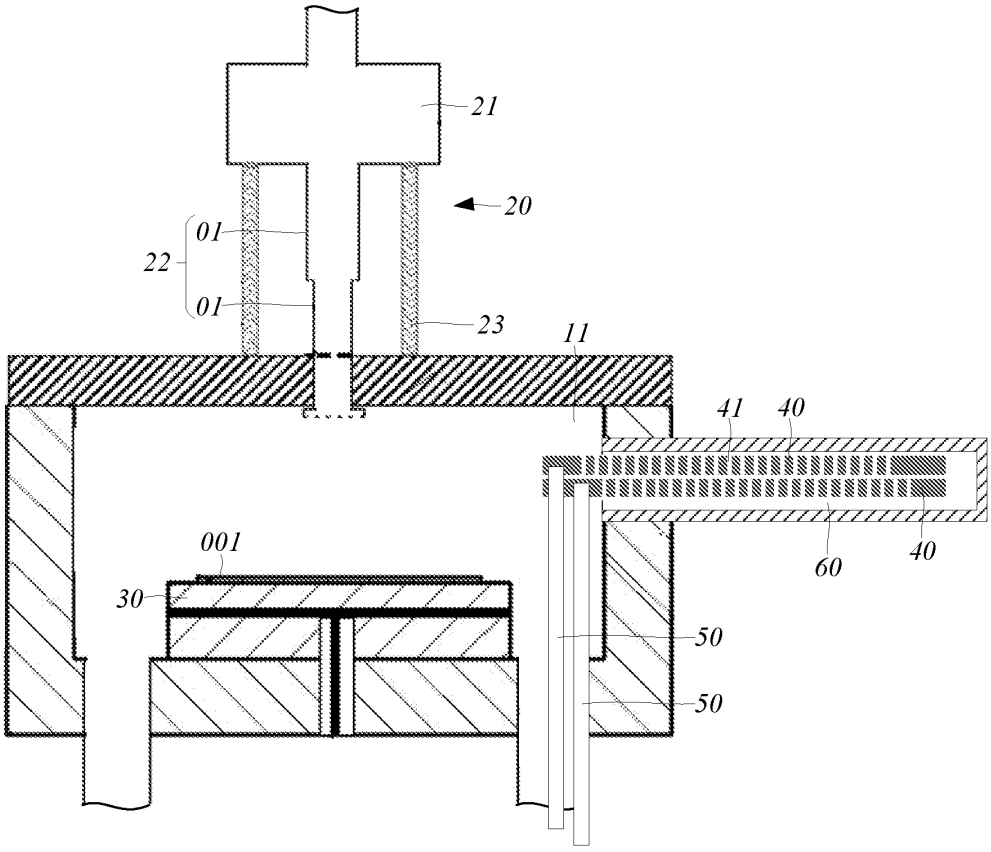


图 14



图 15