

## CLAIMS

1. ——— A computer program product for facilitating processing within a computing environment, the computer program product comprising:

——— ~~aat least one~~ computer readable storage medium readable by ~~aat least one~~ processing circuit and storing instructions for performing a method comprising:

——— obtaining an instruction to perform a sort operation, the instruction being a single architected machine instruction of an instruction set architecture, and wherein the instruction uses information of a register employed by the instruction to locate a parameter block to be used by the instruction, the parameter block including information used by the instruction depending on a function to be performed by the instruction; and

——— executing, by a general-purpose processor of the computing environment, the instruction, the executing comprising:

——— sorting a plurality of input lists to obtain one or more sorted output lists;

and

——— providing as output the one or more sorted output lists.

2. ——— The computer program product of claim 1, wherein the instruction includes an operation code field including an operation code to specify a sort list operation, and one field to be used to designate one location, the one location to be used in storing the one or more sorted output lists.

3. ——— The computer program product of claim 2, wherein the instruction further includes another field to be used to designate another location, the other location to store one or more output list delineations.

4. ——— The computer program product of claim 3, wherein the one field is a register field, the register field designating a selected register, the selected register including an address of the one location, and the other field is another register field, the other register field designating another selected register, the other selected register including an address of the other location.

5. ——— The computer program product of claim 1, wherein the instruction employs ~~one implied another~~ register to determine athe function to be performed by the instruction.

6. — The computer program product of claim 51, wherein the function is selected from a group of functions consisting of: a query available functions function, a sort fixed-length records function, and a sort variable-length records function.

7. — The computer program product of claim 5, wherein the ~~instruction employs another~~ register is an implied register to locate ~~the~~ parameter block in memory used by the instruction, ~~the parameter block including information used by and~~ the ~~instruction depending on~~ other register is another implied register to ~~determine~~ the function to be performed ~~by the instruction~~.

8. — The computer program product of claim 71, wherein the function to be performed is a sort fixed-length records function or a sort variable-length records function, and the parameter block includes information to locate the plurality of input lists and information to continue the sorting, based on the sorting being interrupted.

9. — The computer program product of claim 5, wherein the ~~one implied~~ other register further comprises a mode of operation indicator, the mode of operation indicator to be used to specify whether a merge of the one or more sorted output lists is to be performed.

10. — The computer program product of claim 1, wherein the instruction includes an operation code field including an operation code to specify a sort list operation; a first register field including a designation of a first register, the first register including an address used in storing the one or more sorted output lists; and a second register field including a designation of a second register, the second register including an address used in storing one or more output list delineations, and wherein the instruction employs a first implied register to determine ~~the~~ function to be performed by the instruction and a second implied register to locate ~~the~~ parameter block in memory used by the instruction.

11. — A computer system for facilitating processing within a computing environment, the computer system comprising:

a memory; and

a general-purpose processor coupled to the memory, wherein the computer system is configured to perform a method comprising:

obtaining an instruction to perform a sort operation, the instruction being a single architected machine instruction of an instruction set architecture, ~~and wherein the instruction uses~~

information of a register employed by the instruction to locate a parameter block to be used by the instruction, the parameter block including information used by the instruction depending on a function to be performed by the instruction; and

executing, by the general-purpose processor of the computing environment, the instruction, the executing comprising:

sorting a plurality of input lists to obtain one or more sorted output lists; and  
providing as output the one or more sorted output lists.

12. — The computer system of claim 11, wherein the instruction includes an operation code field including an operation code to specify a sort list operation, and one field to be used to designate one location, the one location to be used in storing the one or more sorted output lists.

13. — The computer system of claim 12, wherein the instruction further includes another field to be used to designate another location, the other location to store one or more output list delineations.

14. — The computer system of claim 11, wherein the instruction employs ~~one implied~~ another register to determine athe function to be performed by the instruction.

15. — The computer system of claim 14, wherein the ~~instruction employs another register is an~~ implied register to locate athe parameter block in memory used by the instruction, ~~the parameter block including information used by the instruction depending on~~ and the other register is another implied register to determine the function to be performed by the instruction.

16. — A computer-implemented method of facilitating processing within a computing environment, the computer-implemented method comprising:

obtaining an instruction to perform a sort operation, the instruction being a single architected machine instruction of an instruction set architecture, and wherein the instruction uses information of a register employed by the instruction to locate a parameter block to be used by the instruction, the parameter block including information used by the instruction depending on a function to be performed by the instruction; and

executing, by the general-purpose processor of the computing environment, the instruction, the executing comprising:

sorting a plurality of input lists to obtain one or more sorted output lists; and

providing as output the one or more sorted output lists.

17. — The computer-implemented method of claim 16, wherein the instruction includes an operation code field including an operation code to specify a sort list operation, and one field to be used to designate one location, the one location to be used in storing the one or more sorted output lists.

18. — The computer-implemented method of claim 17, wherein the instruction further includes another field to be used to designate another location, the other location to store one or more output list delineations.

19. — The computer-implemented method of claim 16, wherein the instruction employs ~~one~~ implied another register to determine ~~a~~the function to be performed by the instruction.

20. — The computer-implemented method of claim 19, wherein the ~~instruction employs another register is~~ an implied register to locate ~~a~~the parameter block in memory used by the instruction, ~~the parameter block including information used by the instruction depending on~~ and the other register is another implied register to determine the function to be performed by the instruction.