UNITED METHOD AND APPARATUS TO PREVENT LATERAL OXIDATION IN A TRANSISTOR UTILIZING AN ULTRA THIN OXYGEN-DIFFUSION BARRIER

FIELD

[0001] The present invention relates generally to the field of semiconductor technology and, more specifically, to preventing lateral oxidation in transistors utilizing an ultra thin oxygen-diffusion barrier.

BACKGROUND

[0002] Typically, in semiconductor processes, a transistor device includes a gate characterized by a gate dielectric overlying a substrate, and a gate electrode overlying the gate dielectric. The gate electrode is an electrically conductive material, such as doped polysilicon or metal. The gate dielectric has traditionally been a low-k dielectric material, such as silicon dioxide (SiO2).

[0003] However, due to the great need for smaller transistor devices, the low-k dielectric has had to become increasingly thinner. At a certain thinness, however, the low-k gate dielectric begins to loose its dielectric qualities. Consequently, a more conventional practice has been to replace the low-k dielectric with a high-k dielectric. A high-k dielectric can provide greater dielectric qualities at a lower thickness than low-k dielectrics. Unfortunately, high-k dielectrics are not without their problems as well. For example, high-k dielectrics are highly permeable to oxygen diffusion. **Figure 1** illustrates the potential effects of oxygen diffusion through a high-k gate dielectric 102 in a transistor gate structure 100 according to

the prior art. Referring to **Figure 1**, a high-k gate dielectric 102 overlies a silicon substrate 101. Over the high-k gate dielectric 102 is formed a gate electrode 104, also known as a gate terminal, made of an electrically conductive material, such as doped polysilicon. Subsequently, processes such as lithographies, anneals, and spacer depositions can introduce oxygen 106, either as part of the process or unintentionally, as ambient oxygen, which diffuses laterally (horizontally) into the high-k gate dielectric 102 and oxidizes portions of the underlying silicon substrate 101 and the overlying polysilicon gate electrode 104, to form undesirable SiO2 deposits 108.

[0004] These SiO_2 deposits 108 are very undesirable because they effectively increase the thickness of the gate dielectric 102 and decrease the thickness of the gate electrode 104. Furthermore, the SiO_2 deposits 108 reduce the net dielectric constant of the gate dielectric 102, increasing the capacitance of the circuit. Consequently, the benefit of utilizing a high-k gate dielectric is lost. Additionally, the SiO_2 deposits 108 are undesirable because they attack the area of the silicon substrate 101 where the channel will be, thus detrimentally affecting the performance of the transistor that will be formed from the gate structure 100.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention is illustrated by way of example and should not be limited by the figures of the accompanying drawings in which like references indicate similar elements and in which:

[0006] **Figure 1** illustrates the potential effects of oxygen diffusion through a high-k gate dielectric in a transistor gate structure according to the prior art.

[0007] **Figure 2** illustrates a transistor with a thin oxygen-diffusion barrier, according to one embodiment of the invention.

[0008] Figures 3A – 3M illustrate a method of forming a transistor with a thin oxygen-diffusion barrier to prevent lateral oxygen diffusion through an oxygen-permeable gate dielectric, according to one embodiment of the invention.

DETAILED DESCRIPTION

[0009] Described herein is a method and apparatus to prevent lateral oxidation in transistors. In the following description numerous specific details are set forth. One of ordinary skill in the art, however, will appreciate that these specific details are not necessary to practice embodiments of the invention. While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive of the current invention, and that this invention is not restricted to the specific constructions and arrangements shown and described since modifications may occur to those ordinarily skilled in the art. In other instances well-known semiconductor fabrication processes, techniques, materials, equipment, etc., have not been set forth in particular detail in order to not unnecessarily obscure embodiments of the present invention.

[0010] According to embodiments of the invention described herein, a method and apparatus are described to form an oxygen-resistant diffusion barrier on the sides of a transistor. The oxygen-resistant diffusion barrier prevents oxygen from diffusing laterally into the sidewalls of a gate-dielectric that has very low resistance to oxygen diffusion, or in other words, that has a high permeability to oxygen diffusion. By preventing lateral diffusion of oxygen, the underlying substrate, or the overlying gate electrode, is protected from undesireable oxidation. Application is particular advantageous for high-k gate dielectrics since most high-k

gate dielectrics are highly permeable to oxygen diffusion. Consequently, an advantage of the oxygen-resistant diffusion barrier is that transistors can have very thin gate dielectrics yet not suffer from lateral oxidation that normally occurs with high-k gate dielectrics. As a result, integrated circuitry can be formed smaller without experiencing loss in performance or reliability.

[0011] **Figure 2** illustrates a transistor 200 with a thin oxygen-diffusion barrier 206, according to one embodiment of the invention. Referring to **Figure 2**, a transistor 200 is formed on a silicon substrate 201. An oxygen- permeable gate dielectric 202, such as a high-k dielectric being highly permeable to oxygen diffusion, is formed on the surface of the substrate 201 and a gate electrode 204 is in turn formed on the oxygen-permeable gate dielectric 202. A thin oxygen-diffusion barrier 206 is formed on the sidewalls of the gate electrode 204 and on the sidewalls of the oxygen-permeable gate dielectric 202. The transistor 200 also includes a pair of thick sidewall spacers 208 formed adjacent to the outside edges of the oxygen-diffusion barrier 206. The transistor 200 includes a pair of source/drain regions 210 each comprising a pair of tips or source/drain extensions 211 and a deep junction source/drain contact region 212.

[0012] Still referring to **Figure 2**, the thin oxygen-diffusion barrier 206 is made of a material that is highly resistant to the diffusion of oxygen. Conventionally, during processing of a transistor, certain processes could be performed that would incidentally expose the oxygen-permeable gate dielectric 202 to oxygen, usually during an oxidation process or via other processes containing ambient oxygen. The oxygen would easily pass through the oxygen-permeable gate dielectric 202 and oxidize the underlying substrate 201 or the overlying gate electrode 204. The oxidation would form undesirable silicon dioxide deposits that would adversely

affect the performance of the transistor, perhaps even rendering the transistor inoperable. The thin oxygen-diffusion barrier 206, however, covers and seals the sidewalls of the oxygen-permeable gate dielectric 206 and prevents the lateral diffusion of oxygen into the oxygen-permeable gate dielectric 206.

[0013] Figures 3A – 3M illustrate a method of forming a transistor with a thin oxygen-diffusion barrier to prevent lateral diffusion of oxygen through an oxygen-permeable gate dielectric, according to one embodiment of the invention. Referring to **Figure 3A**, a plurality of field isolation regions 302 are formed in a substrate 300. The term "substrate" encompasses a semiconductor wafer, such as monocrystalline silicon, as well as structures that have one or more insulative, semi-insulative, conductive, or semiconductive layers and materials. Thus, for example, the term embraces silicon-on-insulator, silicon-on-sapphire, and other advanced structures. Isolation regions 302 may be shallow trench isolation (STI) or deep trench isolation regions formed by etching a trench into the substrate 300 and then filling the trench with a deposited oxide, nitride, or other dielectric material. Field isolation regions 302 may also be formed utilizing other methods, such as LOCOS, recessed LOCOS, or silicon on insulator (SOI) methods.

[0014] The plurality of isolation regions 302 isolate a well 303 of one type conductivity from wells 301 of other type conductivity. For example, well 303 may be a region of a p-type conductivity while wells 301 may be regions of n-type conductivity, or vice-versa. A well of p-type conductivity may be formed by a first implant of boron atoms at a dose of $3.0 \times 10^{13}/cm^2$ at an energy of 230 keV followed by a second implant of boron ions at a dose of $4.2 \times 10^{13}/cm^2$ and an energy of 50 keV into substrate 300 in order to produce a p-well having a concentration of $7.0 \times 10^{17}/cm^3$. A well of n-type conductivity may be formed by a

first implant of phosphorous atoms at a dose of $4x10^{13}/cm^2$ and an energy of 475 keV, a second implant of phosphorous atoms at a dose of $2.5x10^{12}/cm^2$ at an energy of 60keV, and a final implant of arsenic atoms at a dose of $1.10^{13}/cm^2$ at an energy of 180 keV into a silicon substrate having a concentration of $1x10^{16}/cm^3$ in order to produce an n-well having an n-type concentration of approximately $7.0x10^{17}/cm^3$. It is to be appreciated that p-type conductivity regions and n-type conductivity regions may be formed by other means well known to those of ordinary skill in the art.

[0015] The method may continue, as shown in **Figure 3B**, with blanket depositing an electrically insulative ("dielectric") layer 304 on the substrate 300 and on isolation regions 302, the dielectric layer 304 being highly permeable to the diffusion of oxygen, or, in other words, an oxygen-permeable dielectric layer 304. In one embodiment of the invention, the oxygen-permeable dielectric layer 304 is a high-k dielectric material and may be deposited between 2 Å to 50 Å thick. Conventional techniques for blanket depositing a layer of high-k dielectric material include sputter deposition or evaporation techniques.

[0016] The term "high-k" is a relative term that refers to a material with a dielectric constant (k) substantially higher than that of silicon dioxide (SiO_2), or in other words substantially higher than k=3.9. Exemplary high-k materials used in the formation of integrated devices include metal oxides (Al_2O_3, ZrO_2, HfO_2, TiO_2, Y_2O_3, La_2O_3, etc.), ferroelectrics (PZT, BST, etc.), amorphous metal silicates (Hf, Zr), amorphous silicate oxides (HfO_2, ZrO_2), and paralectrics ($Ba_xSr_{1-x}TiO_3$, $PbZr_xTi_{1-x}O_3$).

[0017] High-k dielectrics are very useful to the formation of transistors because of the effective electrically insulative properties of the high-k material compared to its

physical thickness. The high dielectric qualities allow high-k dielectric materials to be deposited very thin yet still possess very good effective electrical "thickness" – in many cases much greater than the effective electrical thickness of SiO_2 at an equivalent physical thickness.

[0018] Despite the many advantages of utilizing a high-k dielectric in the formation of a transistor, however, many classes of high-k dielectrics have an unfortunate disadvantage, they are highly permeable to oxygen diffusion, or in other words, oxygen molecules (or molecules of oxygen compounds) can easily pass through pores in the high-k dielectric material. Consequently, according to one embodiment of the invention, the oxygen-permeable dielectric layer 304 may synonymously be referred as a high-k dielectric. However, other embodiments of the invention may utilize other dielectric materials that are not necessarily high-k materials, but that are still highly permeable to oxygen diffusion.

[0019] The method may continue, as shown in **Figure 3C**, with blanket depositing an electrically conductive material 306 over the oxygen-permeable dielectric layer 304, to a thickness scaled with the technology. In one embodiment of the invention the electrically conductive material 306 is polycrystalline silicon, or polysilicon, and is deposited to a thickness of between approximately 600 Å to 2000 Å, 1600 Å being preferable. Conventional polysilicon blanket deposition processes are well known in the art, including chemical vapor deposition (CVD) and physical vapor deposition (PVD). Such deposition processes typically take place at temperatures in the range of 600 to 650 °C, however these deposition processes may take place at higher temperatures. Silane or gas streams containing N_2 or H_2, at 100%, may be used in the polysilicon deposition process. The electrically conductive layer 306 can be ion implanted to the desired

conductivity type and level prior to, or after, patterning. In other embodiments of the invention, other materials may be utilized in conjunction with, or in place of, polysilicon, such as metal, metal alloy, and metal oxide, single crystalline silicon, amorphous silicon, silicide, or other materials well known in the art to form a gate electrode.

[0020] The method may continue with forming a hard-mask 312 on the electrically conductive layer 306, as shown in **Figures 3D – 3E**. Several well-known methods may be employed for forming a hard-mask on an electrically conductive layer 306. In the embodiment of the invention shown in **Figure 3D**, the hard-mask 312 may be formed by depositing a hard mask layer 308, such as a nitride layer, via a chemical vapor deposition (CVD) over the electrically conductive layer 306. A typical photolithography process can then be performed including the well-known steps of masking, exposing, and developing a photoresist layer to form a photoresist mask 310, shown in **Figure 3D**. Then, as shown in **Figure 3E**, the pattern of the photoresist mask 310 is transferred to the masking layer 308 by etching the masking layer 308 to the top of the electrically conductive layer 306, using the photoresist mask 310 to align the etch, thus producing a hard-mask 312 over the electrically conductive layer 306.

[0021] The method continues, as shown in **Figure 3F**, with removing the photoresist mask 310 and etching the electrically conductive layer 306 down to the top of the oxygen-permeable dielectric layer 304 using the hard-mask 312 to align the etch, thus creating a conductive structure 318, also known as a gate electrode or gate terminal, underneath the hard-mask 312. The etchant 316 should etch the electrically conductive layer 306, but not the hard-mask 312 or the oxygen-permeable dielectric layer 304. To prevent lateral etching into the

sidewalls of the gate electrode 318, a dry etch is preferable utilizing a Chlorine based chemistry. A hot phosphorous etch may then be applied to remove the hard-mask 312.

[0022] Next, the method may continue, as shown in **Figure 3G**, with etching the oxygen-permeable dielectric layer 304 to the top of the substrate 300 and to the tops of the isolation regions 302. The etch chemistry should be such that the oxygen-permeable dielectric layer 304 is etched but neither the substrate 300, the gate electrode 318, nor the isolation regions 302 are etched. The etch leaves a portion 319 of the oxygen-permeable dielectric layer 304 directly underneath the gate electrode 318. This portion 319 of the dielectric layer 304 is also known as a gate dielectric and is the same material as the oxygen-permeable dielectric layer 304. The portion 319 of the oxygen-permeable dielectric layer underneath the gate electrode 318 will herein be referred to as a "gate dielectric", or "oxygen-permeable gate dielectric". In one embodiment of the invention, as described in further detail above, the oxygen-permeable gate dielectric 319 comprises a high-k dielectric material. The gate electrode 318 aligns the etch so that the sidewalls of the oxygen-permeable gate dielectric 319 are vertically aligned to the sidewalls of the gate electrode 318. To minimize the risk of etching the substrate, a wet etch may be preferable to a dry etch. In one embodiment of the invention an exemplary etch chemistry may include a 50:1 HF etch for 40 seconds, or until the oxygen-permeable dielectric layer 304 is completely removed from the surface of the isolation regions 302 and from the surface the substrate 300, except for directly underneath the gate electrode 318. Because of the highly diffusible nature of the oxygen-permeable gate dielectric 319, the etching of the oxygen-permeable dielectric layer 304 should be careful not to introduce oxygen, whether

directly as part of the process since the oxygen-permeable gate dielectric 319 will be exposed and the oxygen would diffuse laterally into the oxygen-permeable gate dielectric 319.

[0023] The gate electrode 318 and the oxygen-permeable gate dielectric 319 together define a composite structure 324, sometimes known as a gate structure, or gate, of an integrated device, such as a transistor. As shown in **Figure 3G**, the sidewalls of the gate structure 324 begin at the top edge 320 of the gate electrode 319 and extend downward along the entire length of the sidewalls of both the gate electrode 318 and the oxygen-permeable gate dielectric 319.

[0024] Next, as shown in **Figure 3H**, a thin oxygen-resistant layer 326 is blanket deposited over the top of the gate structure 324 and along the entire length of the sides of the gate structure 324, including on (touching) the entire length of the sidewalls of the gate electrode 318 and the gate dielectric 319. At the same time, the thin-oxygen resistant layer 326 is deposited on top of any exposed portion of the substrate 300 or isolation regions 302. The oxygen-resistant layer 326 is a material that should be resistant to the diffusion of oxygen and also does not contain oxygen molecules that may interfacially diffuse into the touching oxygen-permeable gate dielectric 319. In other words, the oxygen-resistant layer 326 is highly resistant to oxygen diffusion and is free from diffusible oxygen. An exemplary material for the oxygen-resistant layer 326 is a nitride, such as silicon nitride, boron nitride, magnesium nitride, etc., formed by any well-known process of depositing a thin nitride film. Exemplary blanket deposition processes include a Bistertiarybutylaminosilane (BTBAS) process, an atomic layer deposition (ALD) process, or a hotwall process (ammonia + Silane).

[0025] During the formation of the thin oxygen-resistant layer 326, just as during

the etching of the oxygen-permeable dielectric layer 304 described above, care should be taken to prevent oxygen from being introduced into the process when the oxygen-permeable gate dielectric 319 may be exposed including during the patterning of the oxygen-permeable dielectric layer 304 and during the formation of the thin oxygen-resistant layer 326. Oxygen exposure may be substantially limited by performing all, or part, of the method in a substantially oxygen-free environment, such as a vacuum. However, even with best efforts, minute amounts of ambient oxygen may inadvertently be introduced during the process and may laterally diffuse into the oxygen-permeable dielectric layer 304. Thus, the method of depositing the thin oxygen-resistant layer 326 may further be optimized to prevent lateral oxidation, or, in other words, to prevent oxidation to the area 327 of the substrate 300 underneath the oxygen-permeable gate dielectric 319 by lateral diffusion of oxygen. For example, a low-temperature method of depositing the oxygen-resistant layer 326 may be advantageous since oxidation of the substrate 300 is less likely to occur at low temperatures (e.g., less than approximately 650°C). The low temperature reduces the chances of even minor oxidation to the portion 327 of the substrate 300 if, by chance, a small portion of oxygen is somehow introduced. A BTBAS process is advantageous because it can be performed at a low temperature, between approximately 550° C – 650° C, compared to some other methods, such as a hotwall process, which is typically performed at a temperature of approximately 800° C. Therefore, in one embodiment of the invention, a BTBAS process may be utilized to deposit the oxygen-resistant layer 326.

[0026] An exemplary BTBAS process is a CVD process that may include heating at least the surface of the substrate 300, the sides of the oxygen-permeable gate

dielectric 319, and the sides and top of the gate electrode 318 to a temperature between approximately 500° C to 650° C, preferably 600° C. Then, at a pressure of approximately 600 Torr, simultaneously flowing molecular nitrogen (N_2) at approximately 2,000 standard cubic centimeters per second (sccm), ammonia (NH_3) at approximately 200 sccm, and BTBAS at approximately 800 milligrams per minute (mgm). The N_2, NH_3, and BTBAS combine to form silicon nitride at a rate of approximately 1 Å per second. The BTBAS process hermetically seals the oxygen-resistant layer 326 to the sides of gate electrode 318 and the gate dielectric 319.

[0027] One ordinarily skilled in the art will recognize that in some embodiments of the invention, other low temperature processes of depositing the thin oxygen-resistant layer 326 may also be advantageously utilized. At the same time, it should be important to note that a low-temperature process is advantageous to limit oxidation of the area 327 if some oxygen has somehow laterally diffused into the oxygen-permeable gate dielectric 319, but high-temperature methods may also be utilized in depositing the oxygen-resistant layer 326 if no oxygen has laterally diffused into the oxygen-permeable gate dielectric 319. Furthermore, high-temperature methods may also be utilized if only a minor amount of oxygen has laterally diffused into the oxygen-permeable gate dielectric 310 since minor oxidation may be acceptable to a certain degree.

[0028] In one embodiment of the invention, the thin oxygen-resistant layer 326 should be deposited thick enough to act as a diffusion barrier to oxygen, to prevent oxygen from diffusing laterally into the sidewalls of the oxygen-permeable gate dielectric 319 during subsequent processes. However, the thin oxygen-resistant layer 326 should not be deposited so thick that it will interfere with the

subsequent formation of tip-implants, described in detail further below. Therefore, in one embodiment of the invention, the thin oxygen-resistant layer 326 is deposited between approximately 2Å to 300Å.

[0029] Next, as shown in **Figure 3I**, the thin oxygen-resistant layer 326 is etched using a substantially vertical, or anisotropic, etch technique. An anisotropic etch technique uses an etch chemistry that etches primarily in the vertical (anisotropic) direction, although a small amount of horizontal (isotropic) etching may occur. An exemplary chemistry for the etch may be a standard nitride etch with a carbon tetraflouride (CF_4) chemistry (e.g., CF_4H_2, or $CF_4 + O_2$ in a plasma generator). The anisotropic etch removes the thin oxygen-resistant layer 326 from the top of the gate electrode 318 as well as from the top surface of the isolation regions 302 and from most of the top surface of the substrate 300 except immediately to either side of the gate structure 324. The anisotropic etch, however, leaves a portion 330 of the oxygen-resistant layer 326 along the entire length of the sidewalls of both the gate electrode 318 and the oxygen-permeable gate dielectric 319.

[0030] The portion 330 may be referred to as a "thin oxygen-resistant spacer" since it is similar in appearance to conventional thick spacers typically formed during the fabrication of a transistor. However, the typical function of a thick spacer is to prevent vertical doping of impurities to certain regions of the substrate, whereas the function of the portion 330 left on the sidewalls is to prevent the lateral diffusion of oxygen into the oxygen permeable gate dielectric 319. In addition, typical thick spacers may not necessarily be oxygen-resistant, may contain interfacially diffusive oxygen, and are formed much thicker. Consequently, herein the portion 330 left on the sidewalls will be referred to as a "thin oxygen-diffusion barrier" since one of its functions is to act as a barrier to

oxygen diffusion.

[0031] The thin oxygen-diffusion barrier 330 covers and hermetically seals the sidewalls of the oxygen-permeable gate dielectric 319. If the thin oxygen-diffusion barrier 330 were not present, oxygen (O_2, O_3, etc.) that is directly applied during a subsequent process, or ambient oxygen that exists in the atmosphere, would pass laterally through fine pores in the oxygen-permeable gate dielectric 310 and into the silicon substrate 300 underneath the oxygen-permeable gate dielectric 310, oxidizing the silicon substrate in the channel area 327 forming silicon dioxide deposits. The silicon dioxide deposits would affect the eventual performance of the integrated device by interfering with current flow through the channel 327. At the same time, if not for the a thin oxygen-diffusion barrier 330 oxygen would laterally diffuse into the oxygen-permeable gate dielectric 319 into the touching gate electrode 318 directly above the oxygen-permeable gate dielectric 319. If the gate electrode 318 is made of a material that can be oxidized, such as polysilicon, silicon dioxide deposits may also form at the interface between the gate electrode 318 and the gate dielectric 319. Since silicon dioxide is a dielectric, formation of silicon dioxide deposits in the substrate 300, or in the gate electrode 318, would increase the physical thickness of the gate dielectric 319. Furthermore, since silicon dioxide has a relatively low-k dielectric value compared to that of the oxygen-permeable gate dielectric 319, the effective electrical k value of the gate dielectric 319 would dramatically decrease, essentially negating the advantageous purposes for using a high-k dielectric material.

[0032] Another advantage of the thin oxygen-diffusion barrier 330 is that the edges of the gate electrode 318 touching the oxygen-resistant spacers 330 are sealed as well. The seal of the thin oxygen-diffusion barrier 330 to the edges of the gate

electrode 318 and to the edges of the oxygen-permeable gate dielectric 319 help to improve the hot electron lifetime of the transistor.

[0033] Immediately after forming the oxygen-diffusion barrier, the method may continue, as shown in **Figure 3J**, with forming tips 340, or shallow source/drain extensions, by utilizing a tip implant process. Numerous well-known techniques may be utilized to form tips 340 in the substrate 300. In one embodiment of the invention, the substrate 300 is doped with ions having an opposite conductivity to that of the conductivity of the well 303. For example, if well 303 had a p-type conductivity, then the tip implant would include implanting n-type conductivity ions, such as arsenic ions, into the top of the substrate 300 to form conventional N-tip regions. If however, the well 303 had an n-type conductivity, then the tip implant would include implanting p-type conductivity ions, such as boron ions, into the top of the substrate 300 to form convention P-tip regions. The gate electrode 318 protects the substrate region beneath the gate dielectric 319 from being implanted with ions.

[0034] The dose of the implantation is lower than that used to form deep source/drain junctions described in further detail below. For example, in one embodiment of the invention, the n-type conductivity ions may be deposited with a dose in the range of approximately $1x10^{15}$ ions/cm^2. In addition, to ensure that the tips 340 are formed to a shallow depth, the implant energy should be low, for example around 10 keV.

[0035] In one embodiment of the invention, the ions are implanted at a directly vertical angle (90°) forming tips 340 that are in alignment with the outside edges of the oxygen-diffusion barrier 330. A rapid thermal process (RTP) anneal may then be performed to drive the tips 340 underneath the oxygen-diffusion barrier 340

and partially underneath the oxygen-permeable gate dielectric 319.

[0036] One ordinarily skilled in the art, however, will recognize that other techniques may be performed to implant the shallow tips 340 at an angle other than 90°. An angled ion implantation may require a slightly higher implant energy since the angle of the ion implantation may require the ions to be implanted through the lower portions of oxygen-diffusion barrier 340 or the oxygen-permeable gate dielectric 319 to reach the substrate underlying the oxygen-diffusion barrier 340 or the oxygen-permeable gate dielectric 319.

[0037] Next, as shown in **Figures 3K – 3L**, the method may continue by forming thick spacers 344 adjacent to, and touching the outer sidewalls of the thin oxygen-diffusion barrier 330. Thick spacers 344 may consist of silicon nitride or may be a combination of silicon nitride and silicon oxide. In one embodiment of the invention, the thick spacers 344 are an oxide/nitride/oxide (ONO) composite formed by a rapid thermal oxidation process. In another embodiment of the invention, thick spacers 344 are a nitride/oxide composite. The nitride/oxide spacers may be formed by blanket depositing a thin, approximately 50-100Å, oxide layer 341 over the isolation regions 302, the tip implants 340, the thin oxygen-diffusion barrier 330, and the gate electrode 318, as shown in **Figure 3K**. The blanket deposition of the oxide layer 341 may include any well-known CVD process, including a BTBAS process. It is advantageous to keep the deposition temperature low, preferably at 650°C so that the thermal energy does not disturb the implanted tips 340. Next a 500 - 1800Å thick silicon nitride layer 342 is deposited onto the oxide layer 341. Silicon nitride layer may be formed by standard CVD deposition methods, including BTBAS deposition techniques. Again, it is advantageous to keep the deposition temperature low. Then, silicon

nitride layer 342 and oxide layer 341 are anisotropically etched to form thick spacers 344, as shown in **Figure 3L**. The thick spacers 344 ensure that a subsequent deep implant does not disturb the tip 340 underlying the thick spacers 344. Consequently, the thick spacers 344 should be formed thick and wide enough to prevent the subsequent deep, high dose ion implantation, described below in **Figure 3M**, from overwhelming the portion of the shallow tip 340 underneath the thick spacers 344.

[0038] Next, as shown in **Figure 3M**, the substrate 300 is subjected to a deep, high dose implant process to form deep junction source/drain regions 348 in the well region 303. The deep implant includes implanting ions with the same conductivity type impurities used to form the tips 340. For example, if well 303 is of a p-type conductivity, an n-type ion is implanted, whereas for an n-type conductivity well, a p-type ion is implanted. Exemplary n-type ions include arsenic and phosphorous, whereas exemplary p-type ions include boron. At the same time, if the electrically conductive gate electrode 318 comprises polysilicon, the deep implant process can be used to dope the polysilicon in the gate electrode if not previously doped. In one embodiment of the invention, the deep implants 348 are formed to a concentration of between $1x10^{19}/cm^3$ – $5x10^{20}/cm^3$ and a depth of approximately 0.15-0.25 micrometers. An activation anneal may be performed to activate the tips 340 and deep implants 348. The anneal may be performed with a RTP at a temperature of between 900° C – 1200° C, with 1050° C being preferred, for approximately 10 – 300 seconds, with 20 seconds being preferred, in a nitrogen atmosphere.

[0039] Several embodiments of the invention have thus been described. However, those skilled in the art will recognize that the invention is not limited to

the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims that follow.

What is claimed:

1. A method, comprising:

forming a gate structure on a silicon substrate, the gate structure comprising an electrically conductive gate electrode on an oxygen-permeable gate dielectric, the gate structure having sidewalls;

forming a thin oxygen-resistant layer on an entire sidewall length of the gate structure, the thin oxygen-resistant layer to prevent oxygen from diffusing laterally into the oxygen-permeable gate dielectric, wherein the forming the thin oxygen-resistant layer is performed at a temperature less than 650C to prevent lateral oxidation; and

forming a pair of relatively thick sidewall spacers, each of the pair of relatively thick sidewall spacers formed from a first layer and a second layer, wherein the first layer comprises silicon oxide and the second layer comprises silicon nitride, wherein the first layer is formed adjacent to, and in contact with, the outside edges of the thin oxygen-diffusion barrier and adjacent to and in contact with the silicon substrate between the thin oxygen-diffusion barrier and the second layer.

2. The method of claim 1, further comprising forming shallow source/drain extensions in the silicon substrate adjacent to the gate structure immediately after forming the thin oxygen-diffusion barrier.

3. The method of claim 1, wherein the oxygen-permeable dielectric layer is a high-k dielectric material.

4. The method of claim 1, wherein the thin oxygen-resistant layer is formed to a thickness between approximately 2 Å to 300 Å.

5. The method of claim 1, wherein the thin oxygen-resistant layer does not contain diffusible oxygen.

6. The method of claim 1, wherein the thin oxygen-resistant layer is a nitride.

7. The method of claim 1, wherein the thin oxygen-resistant layer is formed via a BTBAS process.

8. The method of claim 1, further including performing the method in a substantially oxygen-free environment.

9. A method comprising:

depositing a high-k dielectric layer on a substrate, the high-k dielectric layer being highly permeable to oxygen diffusion;

depositing an electrically conductive layer on the high-k dielectric layer;

patterning the electrically conductive layer and high-k dielectric layer to form a gate structure on the substrate, the gate structure having an electrically conductive gate electrode and a high-k gate dielectric, the electrically conductive gate electrode and high-k gate dielectric having vertically aligned sidewalls;

blanket depositing a thin oxygen-resistant layer over the gate structure and on the vertically aligned sidewalls of the electrically conductive gate electrode and high-k gate dielectric, the thin oxygen-resistant layer deposited to a thickness between approximately 2Å to 300Å;

anisotropically etching the thin oxygen-resistant layer to form a thin oxygen-resistant layer layer on the vertically aligned sidewalls of the gate electrode and the high-k gate dielectric; and

forming thick spacers adjacent to outer sidewalls of the thin oxygen-diffusion barrier, wherein the thick spacers comprise a substantially thin oxygen layer deposited on the outer sidewalls of the thin oxygen-resistant layer and a substantially thick silicon nitride layer deposited on the substantially thin oxygen layer.

10. The method of claim 9, wherein the electrically conductive layer comprises polysilicon.

11. The method of claim 9, wherein the thin oxygen-resistant insulating layer comprises nitride.

12. The method of claim 9, wherein the thin oxygen-resistant layer is deposited utilizing a low-temperature process.

13. The method of claim 9, wherein the thin oxygen-resistant layer is deposited at a temperature of less than 650°C.

14. The method of claim 9, wherein the thin oxygen-resistant layer is free from diffusible oxygen.

15. An apparatus, comprising:

an oxygen-permeable gate dielectric overlying a substrate;

an electrically conductive gate electrode over the oxygen-permeable gate dielectric;

a thin oxygen-resistant layer covering the entire sidewall length of the gate dielectric, the thin oxygen diffusion barrier to prevent oxygen from diffusing laterally into the gate dielectric; and

thick spacers adjacent to outer sidewalls of the thin oxygen-diffusion barrier, wherein the thick spacers comprise a substantially thin oxygen layer deposited on the outer sidewalls of the thin oxygen-resistant layer and a substantially thick silicon nitride layer deposited on the substantially thin oxygen layer.

16. The apparatus of claim 15, wherein the gate dielectric is a high-k dielectric material.

17. The apparatus of claim 15, wherein the electrically conductive structure is polysilicon.

18. The apparatus of claim 15, wherein the thin oxygen-resistant layer has a thickness between approximately 2 Å to 300 Å.

19. The apparatus of claim 15, wherein the thin oxygen-resistant layer comprises a nitride material.

20. The apparatus of claim 15, wherein the thin oxygen-resistant layer is free from diffusible oxygen.

21. An integrated circuit, comprising:

a silicon substrate;

a high-k gate dielectric overlying the silicon substrate, the high-k gate dielectric having sidewalls;

an electrically conductive gate electrode overlying the high-k gate dielectric;

a thin oxygen-resistant layer covering the entire sidewall length of the high-k gate dielectric, the thin oxygen-resistant layer to prevent oxygen from diffusing laterally into the gate dielectric; and

thick spacers adjacent to outer sidewalls of the thin oxygen-diffusion barrier, wherein the thick spacers comprise an oxygen layer deposited on the outer sidewalls of the thin oxygen-diffusion barrier, and a silicon nitride layer deposited on the oxygen layer.

22. The integrated circuit of claim 21, wherein the thin oxygen-resistant layer comprises a nitride material.

23. The integrated circuit of claim 21, wherein the thin oxygen-resistant layer is free from diffusible oxygen.

24. The integrated circuit of claim 21, wherein the high-k gate dielectric has a dielectric constant substantially higher than that of silicon dioxide.

25. The integrated circuit of claim 21, wherein the high-k gate dielectric comprises a material from the group consisting of metal oxides, ferroelectrics, amorphous metal silicates and silicate oxides, and paralectrics.