~~What is claimed is:~~

1. A semiconductor substrate, characterized in that, the semiconductor substrate comprises a first semiconductor layer and a second semiconductor layer located on the first semiconductor layer; wherein the first semiconductor layer and the second semiconductor layer have different cleavage planes in a vertical direction; a semiconductor layer obtained by symmetrically rotating the first semiconductor layer according to a lattice structure of the first semiconductor layer has a different cleavage plane in the vertical direction as that of the second semiconductor layer; a semiconductor layer obtained by symmetrically rotating the second semiconductor layer according to a lattice structure of the second semiconductor layer has a different cleavage plane in the vertical direction as that of the first semiconductor layer; or the semiconductor layer obtained by symmetrically rotating the first semiconductor layer according to the lattice structure of the first semiconductor layer and the semiconductor layer obtained by symmetrically rotating the second semiconductor layer according to the lattice structure of the second semiconductor layer have different cleavage planes in the vertical direction.

2. The semiconductor substrate according to claim 1, wherein the first semiconductor layer and the second semiconductor layer have a same material or different materials.

3. The semiconductor substrate according to claim 2, wherein the first semiconductor layer and the second semiconductor layer have a same lattice structure, a same crystallographic direction in the vertical direction, and non-coincident crystallographic directions in a horizontal direction.

4. The semiconductor substrate according to claim 2, wherein the first semiconductor layer and the second semiconductor layer have different lattice structures, and non-coincident crystallographic directions in a horizontal direction.

5. The semiconductor substrate according to claim 1, wherein a material of the first semiconductor layer is one of a crystalline material and an amorphous material or a combination thereof.

6. The semiconductor substrate according to claim 5, wherein the material of the first semiconductor layer is the amorphous material, the amorphous material comprises a non-semiconductor material, the non-semiconductor material is one of aluminum nitride, polycrystalline silicon carbide, ceramics and quartz.

7. The semiconductor substrate according to claim 5, wherein the material of the first ~~semiconductor layer is the amorphous material, a bonding direction of the first~~

semiconductor layer and the second semiconductor layer is not limited.

8. The semiconductor substrate according to claim 1, wherein the second semiconductor layer is a crystalline layer.

9. The semiconductor substrate according to claim 1, wherein the first semiconductor layer and the second semiconductor layer are laminated sequentially and alternately to form a laminated structure having three or more layers.

10. The semiconductor substrate according to claim 9, wherein the laminated structure comprises a dielectric layer between the first semiconductor layer and the second semiconductor layer.

11. The semiconductor substrate according to claim 10, wherein the dielectric layer and an adjacent first semiconductor layer have a same crystallographic direction in the vertical direction, and non-coincident crystallographic directions in a horizontal direction;

and/or,

the dielectric layer and an adjacent second semiconductor layer have a same crystallographic direction in the vertical direction, and non-coincident crystallographic directions in the horizontal direction.

12. The semiconductor substrate according to claim 10, wherein the dielectric layer and an adjacent first semiconductor layer have different crystal structures, and non-coincident crystallographic directions in a horizontal direction;

and/or,

the dielectric layer and an adjacent second semiconductor layer have different crystal structures, and non-coincident crystallographic directions in the horizontal direction.

13. A semiconductor device, characterized in that the semiconductor device comprises a semiconductor substrate and a semiconductor epitaxial layer located on the semiconductor substrate, the semiconductor substrate is a semiconductor substrate according to any of claims 1 to 12.

14. The semiconductor device according to claim 13, wherein the semiconductor epitaxial layer comprises one of silicon, gallium arsenide, gallium nitride, aluminum gallium nitride, indium gallium nitride, aluminum gallium indium nitrogen or a combination thereof.

15. The semiconductor device according to claim 13, wherein the semiconductor device is one of a light emitting diode, a laser diode, a high electron mobility transistor, a field effect transistor, a Schottky diode, a PIN diode and a solar cell.

16. A manufacturing method of a semiconductor substrate, characterized in that the method comprises:

S1. providing a first semiconductor layer;

S2. preparing a second semiconductor layer on the first semiconductor layer, wherein the first semiconductor layer and the second semiconductor layer have different cleavage planes in a vertical direction; a semiconductor layer obtained by symmetrically rotating the first semiconductor layer according to a lattice structure of the first semiconductor layer has a different cleavage plane in the vertical direction as that of the second semiconductor layer; a semiconductor layer obtained by symmetrically rotating the second semiconductor layer according to a lattice structure of the second semiconductor layer has a different cleavage plane in the vertical direction as that of the first semiconductor layer; or the semiconductor layer obtained by symmetrically rotating the first semiconductor layer according to the lattice structure of the first semiconductor layer and the semiconductor layer obtained by symmetrically rotating the second semiconductor layer according to the lattice structure of the second semiconductor layer have different cleavage planes in the vertical direction.

17. The manufacturing method according to claim 16, after the step S2 further comprising:

preparing a semiconductor epitaxial layer on the second semiconductor layer.

18. The manufacturing method according to claim 16, wherein the first semiconductor layer and the second semiconductor layer are prepared with one of a Czochralski method, a zone melting method, a physical vapor deposition method and a chemical vapor deposition method or a combination thereof.

19. The manufacturing method according to claim 16, wherein in the step S2, wafer bonding is used to prepare the second semiconductor layer on the first semiconductor layer.

20. The manufacturing method according to claim 16, wherein the semiconductor epitaxial layer is prepared with one of a metal organic chemical vapor deposition method, a molecular beam epitaxy method and a hydride vapor phase epitaxy method or a combination thereof.

21. The manufacturing method according to claim 16, after the step S2 further comprising:

preparing a first semiconductor layer on the second semiconductor layer to form a

laminated structure having three layers;

or, preparing a first semiconductor layer and a second semiconductor layer sequentially and alternately on the second semiconductor layer to form a laminated structure having more than three layers.

22. The manufacturing method according to claim 21, further comprising:

growing a dielectric layer between the first semiconductor layer and the second semiconductor layer.

23. The manufacturing method according to claim 22, wherein the dielectric layer is made with one of deposition, thermal oxidation and nitridation, the deposition is one of CVD, PECVD, LPCVD, RTCVD, MOCVD, MBE, ALD or a combination thereof.

What is claimed is:

1. A semiconductor substrate, comprising a first semiconductor layer and a second semiconductor layer located on the first semiconductor layer; wherein

the first semiconductor layer and the second semiconductor layer have different cleavage planes in a vertical direction; or

a semiconductor layer obtained by symmetrically rotating the first semiconductor layer according to a lattice structure of the first semiconductor layer has a different cleavage plane in the vertical direction as that of the second semiconductor layer; or

a semiconductor layer obtained by symmetrically rotating the second semiconductor layer according to a lattice structure of the second semiconductor layer has a different cleavage plane in the vertical direction as that of the first semiconductor layer; or

the semiconductor layer obtained by symmetrically rotating the first semiconductor layer according to the lattice structure of the first semiconductor layer and the semiconductor layer obtained by symmetrically rotating the second semiconductor layer according to the lattice structure of the second semiconductor layer have different cleavage planes in the vertical direction.

2. The semiconductor substrate according to claim 1, wherein the first semiconductor layer and the second semiconductor layer have a same lattice structure, a same crystallographic direction in the vertical direction, and non-coincident crystallographic directions in a horizontal direction.

3. The semiconductor substrate according to claim 1, wherein the first semiconductor layer and the second semiconductor layer have different lattice structures, and non-coincident crystallographic directions in a horizontal direction.

4. The semiconductor substrate according to claim 1, wherein a material of the first semiconductor layer is one of a crystalline material and an amorphous material or a combination thereof.

5. The semiconductor substrate according to claim 4, wherein the material of the first semiconductor layer is the amorphous material, the amorphous material comprises a non-semiconductor material, the non-semiconductor material is one of aluminum nitride, polycrystalline silicon carbide, ceramics and quartz.

6. The semiconductor substrate according to claim 4, wherein the material of the first semiconductor layer is the amorphous material, a bonding direction of the first semiconductor layer and the second semiconductor layer is not limited.

7. The semiconductor substrate according to claim 1, wherein the second semiconductor layer is a crystalline layer.

8. The semiconductor substrate according to claim 1, wherein the first semiconductor layer and the second semiconductor layer are laminated sequentially and alternately to form a laminated structure having three or more layers.

9. The semiconductor substrate according to claim 8, wherein the laminated structure comprises a dielectric layer between the first semiconductor layer and the second semiconductor layer.

10. The semiconductor substrate according to claim 9, wherein the dielectric layer and an adjacent first semiconductor layer have a same crystallographic direction in the vertical direction, and non-coincident crystallographic directions in a horizontal direction;

and/or,

the dielectric layer and an adjacent second semiconductor layer have a same crystallographic direction in the vertical direction, and non-coincident crystallographic directions in the horizontal direction.

11. The semiconductor substrate according to claim 9, wherein the dielectric layer and an adjacent first semiconductor layer have different crystal structures, and non-coincident crystallographic directions in a horizontal direction;

and/or,

the dielectric layer and an adjacent second semiconductor layer have different crystal structures, and non-coincident crystallographic directions in the horizontal direction.

12. A semiconductor device, comprising a semiconductor substrate and a semiconductor epitaxial layer located on the semiconductor substrate, the semiconductor substrate is a semiconductor substrate according to any of claims 1 to 11.

13. The semiconductor device according to claim 12, wherein the semiconductor epitaxial layer comprises one of silicon, gallium arsenide, gallium nitride, aluminum gallium nitride, indium gallium nitride, aluminum gallium indium nitrogen or a combination thereof.

14. The semiconductor device according to claim 12, wherein the semiconductor device is one of a light emitting diode, a laser diode, a high electron mobility transistor, a field effect transistor, a Schottky diode, a PIN diode and a solar cell.

15. A manufacturing method of a semiconductor substrate, comprising:

S1. providing a first semiconductor layer; and

S2. preparing a second semiconductor layer on the first semiconductor layer, wherein

the first semiconductor layer and the second semiconductor layer have different cleavage planes in a vertical direction; or

a semiconductor layer obtained by symmetrically rotating the first semiconductor layer according to a lattice structure of the first semiconductor layer has a different cleavage plane in the vertical direction as that of the second semiconductor layer; or

a semiconductor layer obtained by symmetrically rotating the second semiconductor layer according to a lattice structure of the second semiconductor layer has a different cleavage plane in the vertical direction as that of the first semiconductor layer; or

the semiconductor layer obtained by symmetrically rotating the first semiconductor layer according to the lattice structure of the first semiconductor layer and the semiconductor layer obtained by symmetrically rotating the second semiconductor layer according to the lattice structure of the second semiconductor layer have different cleavage planes in the vertical direction.

16. The manufacturing method according to claim 15, wherein the first semiconductor layer and the second semiconductor layer are prepared with one of a Czochralski method, a zone melting method, a physical vapor deposition method and a chemical vapor deposition method or a combination thereof.

17. The manufacturing method according to claim 15, wherein in the step S2, wafer bonding is used to prepare the second semiconductor layer on the first semiconductor layer.

18. The manufacturing method according to claim 15, wherein the semiconductor epitaxial layer is prepared with one of a metal organic chemical vapor deposition method, a molecular beam epitaxy method and a hydride vapor phase epitaxy method or a combination thereof.

19. The manufacturing method according to claim 15, after the step S2 further comprising:

preparing a first semiconductor layer on the second semiconductor layer to form a laminated structure having three layers;

or, preparing a first semiconductor layer and a second semiconductor layer sequentially and alternately on the second semiconductor layer to form a laminated structure having more than three layers.

20. The manufacturing method according to claim 19, further comprising:

growing a dielectric layer between the first semiconductor layer and the second semiconductor layer.

21. The manufacturing method according to claim 20, wherein the dielectric layer is made with one of deposition, thermal oxidation and nitridation, the deposition is one of CVD, PECVD, LPCVD, RTCVD, MOCVD, MBE, ALD or a combination thereof.