

Abstract

Digital Signal Processor

5 A Digital Signal Processor (DSP) includes a Random Access
Memory (RAM) (12) for storing predetermined coefficients and data
samples and a first latch (13) coupled to the RAM (12) for
temporarily storing either a coefficient or a data sample from the
RAM. A multiplier (14) is arranged for multiplying a value from a
10 first input, which is coupled to the first latch (13), and a
multiplicand from a second input to produce a product. A second
latch (16) is coupled to temporarily store the product from the
multiplier (14). An output of the second latch (16) is coupled back
to the second input of the multiplier (14), via a multiplexer (20), to
15 enable the multiplier (14) to multiply the product by the value in
the first latch without requiring further reading of the RAM, thus
enabling efficient calculation of a term including X^i . The output of
the second latch (16) is also coupled to an adder (17) and an
accumulator (19).

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FIG. 2