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(54) A LIQUID CRYSTAL DISPLAY SYSTEM

(71) We, HITACHI LIMITED, of 1—5—1 Marunouchi, Chiyoda-ku, Tokyo, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a liquid crystal display system which behaves from a mechanical point of view as a liquid and from an optical point of view as a solid crystal.

By virtue of their low power consumption, liquid crystal display devices have been used extensively in electronic wrist watches, small-sized electronic desk calculators and the like battery driven apparatus.

Two of the known modes of physical operation of liquid crystal display devices are the dynamic scattering mode (DSM) and the field effect mode (FEM). Known optical operational modes for liquid crystal display devices result in reflection type devices, transmission type devices or absorption type devices.

The present invention can be applied to all the various types of liquid crystal display devices.

The following explanation will be made with reference to the DSM reflection type liquid crystal display.

A DSM reflection type liquid crystal display device exploits the phenomena of dynamic scattering wherein when a liquid crystal is placed between two electrodes and a voltage is applied across the electrodes, the molecules of the liquid crystal which were previously oriented in one given direction are then irregularly oriented, and hence incident light is scattered and the liquid crystal is changed from its transparent state to a semi-transparent (whitish) state. The construction and behaviour of such liquid crystal display devices are described in, for example, the following papers: "Electronics", July 6, 1970, pp. 64—70; and "Transistor Gijutsu" (a Japanese publication), August 1971, pp. 104—109.

When designing a driver circuit for a liquid crystal display device, care need be taken

as detailed below in order to ensure an adequate lifetime for the liquid crystal.

When a D.C. component is applied to a liquid crystal for a long time, the life of the liquid crystal is shortened. Therefore, the general practice is to drive the liquid crystal bidirectionally. To do this in practice, a predetermined voltage is applied across the electrodes which connect with the liquid crystal for a certain period of time and subsequently, the polarity of this voltage is inverted, and the inverted voltage is applied for an equal period of time. A bidirectional liquid-crystal drive circuit of this type is described in "Nikkei Electronics" (a Japanese publication), July 31, 1972 or "Electronics", April 10, 1972.

A problem that arises in a bidirectional liquid-crystal drive system is that, since the potentials of the common electrodes (i.e. the digit electrodes) change during the selection period, it is difficult to adopt a dynamic display system of the type conventionally employed in driver circuits for discharge type display tubes, light emitting diodes and the like display elements.

To take account of this problem, the above-mentioned papers describe a technique for dynamic display wherein the selection of a common electrode is performed by low-frequency pulses and high-frequency pulses which exploit the frequency response characteristics of the liquid crystal. This system has however the disadvantages that, high driving frequencies increase the electric power required by the display, adjustment of the cut-off frequency of the liquid crystal is delicate, and application of the system is expensive.

According to the present invention there is provided a display system including: a plurality of liquid crystal display devices of the type whereof the optical state changes in the region of a predetermined threshold voltage each display device having a first common electrode and a plurality of second electrodes by means of which potentials may be applied across the liquid crystal, respective second electrodes of each display device being connected in common; means for selectively applying to said first electrodes potentials of a high, medium or low level; and means for

selectively applying to said second electrodes potentials of a high or low level, the potential difference existing between said first and any of said second electrodes, when a high level potential is applied to one of them and a low level potential is applied to the other, being in excess of said threshold voltage, and the potential difference existing between said first and any of said second electrodes, when a medium level potential is applied to said first electrode, being below said threshold voltage.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:—

Figure 1 is a graph showing the response characteristics of a liquid crystal;

Figure 2a shows a first embodiment of a liquid crystal display system according to the present invention;

Figure 2b is a waveform timing chart for the circuit of Figure 2a;

Figure 3a shows a second embodiment of a liquid crystal display system according to the present invention;

Figure 3b is a waveform timing chart for the circuit of Figure 3a;

Figure 4a shows a third embodiment of a liquid crystal display system according to the present invention; and

Figure 4b is a waveform timing chart for the circuit of Figure 4a.

Liquid crystal display devices utilized in the following embodiments exhibit a visual threshold voltage V_{th} , so the visual (optical) state of a device may be controlled by means of the applied voltage level as disclosed and claimed in our co-pending Application No. 53,747/73. (Serial No. 1,447,639).

Referring to the first embodiment of a liquid crystal display system shown in Figure 2a, the circuit is arranged to drive n liquid crystal display devices designated LCD1 to LCD n . A liquid crystal in each display device is shown by oblique lines. The n display devices are connected to the driver circuit via n electrodes, one of which is connected to each device, while m segments of each digit are connected to the driver circuit via m corresponding electrodes. The segment electrodes are so arranged that predetermined characters, letters or the like symbols can be displayed. The corresponding segment elec-

trodes of the respective devices are connected in common to the driver circuit.

The circuit of Figure 2a includes two p-channel insulated gate field-effect transistors (hereinbelow simply termed "transistors") M1 and M3 and two n-channel field-effect transistors M2 and M4. The four transistors M1 to M4 constitute two complementary circuits. The source electrodes of the transistors M1 and M3 are connected to a voltage source V_H , whilst the source electrodes of the transistors M2 and M4 are earthed (or connected to a potential V_L).

The circuit includes a logical AND circuit AG1, an OR circuit OG1, an exclusive OR circuit EG1 and an inverter IN1.

To the digit electrode of the first liquid crystal display device LCD1 is applied an output voltage derived from the upper complementary circuit comprised of the transistors M1 and M2. To the first (leftmost in Figure 2a) segment electrode of the display device LCD1 is applied an output signal derived from the complementary circuit comprised of the transistors M3 and M4.

A bidirectional liquid-crystal drive pulse BD is provided to drive the liquid crystal bidirectionally. A digit selecting signal (one of DT1 to DT n) and a segment selecting signal (one of S1 to S m) are provided to drive respective digits and segments.

The AND gate AG1, whose output is connected to the gate electrode of the transistor M1, receives the drive pulses BD and the digit selecting pulses DT1 on respective inputs. The OR gate OG1, whose output is connected to the gate electrode of the transistor M2, receives the drive pulses BD and the inverted digit selecting pulses DT1 on respective inputs. The exclusive-OR gate EG1, whose output is connected to the gate electrodes of the transistors M3 and M4, receives the drive pulses BD and the segment selecting signals S1 on respective inputs.

The operation of the circuit shown in Figure 2a will now be described. In order to facilitate the description, the logical relationship of the bidirectional drive pulse BD with the device and segment selecting signals DT1 and S1, and the potentials V_{c1} and V_{s1} applied to the first digit electrode and the first segment electrode respectively are shown in the timing chart of Figure 2b and in Table 1 below:

TABLE 1

DT1	BD	Vc1
"1"	"1"	VL
"1"	"0"	VH
"0"	"1"	VM
"0"	"0"	VM

S1	BD	Vs1
"1"	"1"	VH
"1"	"0"	VL
"0"	"1"	VL
"0"	"0"	VH

(the logical "1" level corresponds to a positive potential, and the logical "0" level corresponds to earth potential).

The transistors M1 and M2 are both rendered conductive when the digit selecting signal DT1 takes a logical "0" level. Then, the complementary circuit including the transistors M1 and M2 constitutes a voltage divider which provides a potential VM which is the divided voltage. The values of each of the three potentials VM, VH and VL are predetermined so as to satisfy the following inequalities:

$$|VH - VL| \geq V_{th}, |VH - VM| < V_{th},$$

$$|VM - VL| < V_{th}$$

If, when the digit selecting signal DT1 takes a logical "1" level, so selecting the first (leftmost) digit electrode, the leftmost segment electrode, due to the segment selecting signal S1 taking a logical "1" level, is selected, then pulses having opposite phases are applied to both the aforementioned electrodes, that is, the potential difference $|VH - VL|$ is applied bidirectionally between the electrodes. Since the potential $|VH - VL|$ is greater than the voltage V_{th} , the liquid crystal of the applied potential induces scattering. If the segment selecting signal S1 is at a logical "0" level at this time, in-phase pulses are applied to both the electrodes across the crystal. The potential difference between the electrodes across the liquid crystal is thus zero so that scattering is not induced in the liquid crystal.

When the digit selecting signal DT1 takes a logical "0" level, the value of the potential Vc1 which is applied to the leftmost digit electrode is set to the medium potential level VM irrespective of the level of the bidirectional drive pulse BD. Even if the voltages applied to any of the segment electrodes reach the potential levels VH and VL, the liquid crystal corresponding to the leftmost common electrode in the display device LCD1 exhibits no scattering providing the condition $|VH - VM| < V_{th}$ and $|VM - VL| < V_{th}$ are met. In this case, in order to avoid driving the liquid crystal with a D.C. component,

the medium potential level VM is preferably set at or near to the value VM which is defined by the equations:

$$VH - VM = VM - VL, \therefore VM = \frac{VH + VL}{2}$$

As described above, since selection of a digit electrode is made by control of a voltage level, exploiting the fact that the liquid crystal has a visual threshold voltage V_{th} , the problems which arise in the frequency dependant selection system of the prior art are not encountered. Furthermore, since three driving voltage levels are utilized, dynamic display can be readily accomplished even with the bidirectional drive system.

Referring to the second embodiment of the liquid crystal display system shown in Figure 3a, this circuit differs from that shown in Figure 2a in that, to the non-selected segment electrodes is applied the medium potential level VM.

To this end the driving circuitry for the transistors M3 and M4 is modified in the second embodiment with respect to the first embodiment.

The circuit includes AND gates AG1 and AG2; OR gates OG1 and OG2; and inverters IN1 and IN2 and IN3. The AND gate AG1, the OR gate OG1 and the inverter IN1 are connected as in the first embodiment. The AND gate AG2, whose output is connected to the gate electrode of the transistor M3, receives on one input through the inverter IN2, the inverted drive pulses BD and on the other input the segment selecting signals S1. The OR gate OG2, whose output is connected to the gate electrode of the transistor M4, receives on one input through the inverter IN2, the inverted drive pulses BD and on the other input through the inverter IN3 the inverted segment selecting signals S1.

The logical relationship of the bidirectional drive pulse BD and the digit selecting signal DT1 with the potential Vc1 applied to the

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leftmost digit electrode is the same as tabulated with respect to the circuit of the first embodiment shown in Figure 2a. The logical relationship of the bidirectional drive pulse BD and the segment selecting signal S1 with the potential Vs1 applied to the leftmost segment electrodes is tabulated in Table 2 and the timing relationships between all these quantities are illustrated in the waveform timing chart of Figure 3b. The two transistors M3 and M4 constitute a voltage divider when the segment signal S1 takes a logical "0" level which renders them conductive. The divided voltage level VM is predetermined at the value defined above.

TABLE 2

S1	BD	Vs1
"1"	"1"	VH
"1"	"0"	VL
"0"	"1"	VM
"0"	"0"	VM

Hence, according to the second embodiment, a potential difference not in excess of $|VH-VM|$ or $|VM-VL|$ is applied between a selected segment electrode and a non-selected segment electrode rather than the potential difference $|VH-VL|$. The potential difference applied across the segment electrodes is made smaller, so any change in the visual state of the liquid crystal due to a potential difference between the segment electrodes is prevented.

Referring now to the third embodiment of a liquid crystal display driver circuit shown in Figure 4a, this circuit exhibits a lower power consumption than the circuit of the second embodiment shown in Figure 3a.

In this third embodiment, the circuit is arranged to drive four liquid crystal display devices LCD1 to LCD4. Each display device has seven segments for the display of a digit. The circuit includes transistors M5 and M15;

transistors M6 to M9 arranged in a first chain; transistors M16 to M19 arranged in a second chain; inverters IN4 to IN6, IN14 and IN15; and NOR gates NG1 and NG11.

The drive pulses BD are applied to the commoned gate electrodes of the transistors M7 and M8 and to the commoned gate electrodes of the transistors M17 and M18 having passed through the inverter IN6. The digit selecting signals are applied to the gate electrode of the transistor M5 and to one input of the NOR gate NG1 through the inverter IN4. The segment selecting signals S1 are applied to the gate electrode of the transistor M15 and to one input of the NOR gate NG11 through the inverter IN14. Blanking pulses BL are applied to the other inputs of both NOR gates NG1 and NG11.

The output from the NOR gate NG1 is applied firstly to the gate electrode of the transistor M6 through the inverter IN5 and secondly to the gate electrode of the transistor M9. The output from the NOR gate NG11 is applied firstly to the gate electrode of the transistor M16 through the inverter IN15 and secondly to the gate electrode of the transistor M19.

To produce the medium level potential, VM, a voltage divider composed of transistors is not employed in this embodiment. Instead, a separate power source VM is connected to the source electrode of the transistors M5 and M15. In order to prevent the establishment of a current path between the power source VM and either of the power sources VH or VL at switching, transistors M6 and M9, and transistors M16 and M19, are rendered non-conductive during switching by a blanking signal BL as shown in Figure 4b. The pulse width of the blanking signal BL must be longer than the switching time. If, however, the pulse width of the blanking signal BL is made longer than is necessary, the potential of an electrode contacting the liquid crystal is allowed to float for a comparatively long time, and hence, a crosstalk problem arises. Care is required to avoid this snag.

The relationship between the potential Vs1 and Vs1 applied to the electrodes of the liquid crystal display device and the logical signals DT1, S1, BD and BL is shown in Figure 4b and Table 3 below:

TABLE 3

DT1	BD	BL	Vc1
"0"	"0"	"0"	VM
"0"	"0"	"1"	VM
"0"	"1"	"0"	VM
"0"	"1"	"2"	VM
"1"	"0"	"0"	VH
"1"	"0"	"1"	FL
"1"	"1"	"0"	VL
"1"	"1"	"1"	FL

S1	BD	BL	Vs1
"0"	"0"	"0"	VM
"0"	"0"	"1"	VM
"0"	"1"	"0"	VM
"0"	"1"	"1"	VM
"1"	"0"	"0"	VL
"1"	"0"	"1"	FL
"1"	"1"	"0"	VH
"1"	"1"	"1"	FL

FL denotes the floating state (floating potential)

Although the present invention has been described with reference to the preferred embodiments, modifications may be made to the system without departing from the principles of the invention.

To provide the medium voltage VM, a pulse, the potential level of which varies with time can also be used as long as the previously detailed conditions are met. This implies that the mean value of the medium level potential VM should be made

$$(VH+VL)/2,$$

so that the D.C. component can be fully eliminated. To constitute the driver circuit, single channel or bipolar transistors may be utilized. Further, the liquid crystal display devices may be separately arranged so as to correspond to the respective segment electrodes, or may be commonly arranged so as to correspond to one or more digits.

WHAT WE CLAIM IS:—

1. A display system including: a plurality of liquid crystal display devices of the type whereof the optical state changes in the region of a predetermined threshold voltage, each display device having a first common electrode and a plurality of second electrodes by means of which potentials may be applied across the liquid crystal, respective second electrodes of each display device being connected in common; means for selectively applying to said first electrodes potentials of a high, medium or low level; and means for selectively applying to said second electrodes potentials of a high or low level, the potential difference existing between said first and any of said second electrodes, when a high level potential is applied to one of them and a low level

potential is applied to the other, being in excess of said threshold voltage, and the potential difference existing between said first and any of said second electrodes, when a medium level potential is applied to said first electrode, being below said threshold voltage.

2. A display system according to claim 1, including means for selectively applying to said second electrodes potentials of a high, medium or low level.

3. A display system according to claim 1 or claim 2, wherein said means for applying a high or a low level potential includes first and second transistors of complementary conductivity types, said first transistor being connected between a source of high potential and one of said electrodes, and said second transistor being connected between a source of low potential and said one of said electrodes, said transistors being controlled to conduct alternately by means of potentials applied to their control electrodes.

4. A display system according to claim 1 or claim 2, wherein said means for applying potentials of a high, medium or low level includes first and second transistors of complementary conductivity types, said first transistor being connected between a source of high potential and one of said electrodes, and said second transistor being connected between a source of low potential and said one of said electrodes, said transistors being controlled to conduct simultaneously or alternately by means of potentials applied to their control electrodes, the simultaneous conduction of said transistors resulting in the production of a medium level potential at the junction of said transistors.

5. A display system according to claim 3, including third and fourth transistors connected in series between said first and second

TABLE 3

DT1	BD	BL	Vc1
"0"	"0"	"0"	VM
"0"	"0"	"1"	VM
"0"	"1"	"0"	VM
"0"	"1"	"2"	VM
"1"	"0"	"0"	VH
"1"	"0"	"1"	FL
"1"	"1"	"0"	VL
"1"	"1"	"1"	FL

S1	BD	BL	Vs1
"0"	"0"	"0"	VM
"0"	"0"	"1"	VM
"0"	"1"	"0"	VM
"0"	"1"	"1"	VM
"1"	"0"	"0"	VL
"1"	"0"	"1"	FL
"1"	"1"	"0"	VH
"1"	"1"	"1"	FL

FL denotes the floating state (floating potential)

Although the present invention has been described with reference to the preferred embodiments, modifications may be made to the system without departing from the principles of the invention.

To provide the medium voltage VM, a pulse, the potential level of which varies with time can also be used as long as the previously detailed conditions are met. This implies that the mean value of the medium level potential VM should be made

$$(VH + VL)/2,$$

so that the D.C. component can be fully eliminated. To constitute the driver circuit, single channel or bipolar transistors may be utilized. Further, the liquid crystal display devices may be separately arranged so as to correspond to the respective segment electrodes, or may be commonly arranged so as to correspond to one or more digits.

WHAT WE CLAIM IS:—

1. A display system including: a plurality of liquid crystal display devices of the type whereof the optical state changes in the region of a predetermined threshold voltage, each display device having a first common electrode and a plurality of second electrodes by means of which potentials may be applied across the liquid crystal, respective second electrodes of each display device being connected in common; means for selectively applying to said first electrodes potentials of a high, medium or low level; and means for selectively applying to said second electrodes potentials of a high or low level, the potential difference existing between said first and any of said second electrodes, when a high level potential is applied to one of them and a low level

potential is applied to the other, being in excess of said threshold voltage, and the potential difference existing between said first and any of said second electrodes, when a medium level potential is applied to said first electrode, being below said threshold voltage.

2. A display system according to claim 1, including means for selectively applying to said second electrodes potentials of a high, medium or low level.

3. A display system according to claim 1 or claim 2, wherein said means for applying a high or a low level potential includes first and second transistors of complementary conductivity types, said first transistor being connected between a source of high potential and one of said electrodes, and said second transistor being connected between a source of low potential and said one of said electrodes, said transistors being controlled to conduct alternately by means of potentials applied to their control electrodes.

4. A display system according to claim 1 or claim 2, wherein said means for applying potentials of a high, medium or low level includes first and second transistors of complementary conductivity types, said first transistor being connected between a source of high potential and one of said electrodes, and said second transistor being connected between a source of low potential and said one of said electrodes, said transistors being controlled to conduct simultaneously or alternately by means of potentials applied to their control electrodes, the simultaneous conduction of said transistors resulting in the production of a medium level potential at the junction of said transistors.

5. A display system according to claim 3, including third and fourth transistors connected in series between said first and second



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- transistors and said sources of high and low potentials respectively, a source of medium potential level and fifth and sixth transistors connected between said source of medium potential level and said first and second electrodes respectively, said third and fourth transistors being controlled to be non-conductive during switching of said first and second transistors.
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- 10 6. A display system according to any one of claims 3 to 5, wherein said transistors are field-effect transistors.

7. A liquid crystal display system constructed and arranged substantially as herein described with reference to and as illustrated in Figure 2a or Figure 3a or Figure 4a of the accompanying drawings.
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