

Description

Field of the Invention

5 This invention pertains to methods for forming heteroepitaxial structures.

Background of the Invention

10 From the beginning of semiconductor device technology physicists have postulated a host of heterostructures, i.e., combinations of layers of different materials in a single composite crystal. The interest in this kind of structure is traceable to the wide variety of characteristics that can potentially be achieved in devices incorporating such structures.

In the last few years, considerable progress has been made in this field, and techniques are now known that permit production of various combinations of materials. For instance, U.S. patent 4,554,045 teaches a method for producing metal silicide/silicon heterostructures, such that the silicide is essentially monocrys-
15 taline and epitaxial with the underlying silicon substrate.

The known techniques are not restricted to techniques for forming heterostructures comprising a metal silicide layer. For instance, Ishiwara et al, Applied Physics Letters, Vol. 40, pages 66-68 (1982), disclose a technique for growing an epitaxial dielectric layer, namely CaF_2 , on silicon.

20 All of the prior art techniques for growing a heteroepitaxial structure have in common that they involve deposition of material onto the surface of the single crystal substrate. Obviously, once the epitaxial single crystal overlayer is formed it can become the substrate for formation of a further heteroepitaxial layer. Thus, the prior art knows $\text{Si}/\text{CoSi}_2/\text{Si}$ and $\text{Si}/\text{CaF}_2/\text{Si}$ heterostructures formed by particular embodiments of the deposition technique.

25 The prior art also knows several techniques for forming a particular heterostructure, namely, $\text{Si}/\text{SiO}_2/\text{Si}$ (also referred to as SOI). Structurally, SOI differs fundamentally from the above referred to heterostructures since the SiO_2 layer is not a single crystal layer, and, in fact, typically is amorphous. Thus SOI structures are not heteroepitaxial structures in the way the term is used herein, although, through seeding techniques, the orientation of the silicon overlayer can be caused to be the same as that of the silicon wafer upon which
30 the combination was formed.

One particular technique for forming a SOI heterostructure involves implantation of oxygen ions into a silicon substrate. See U.S. Patent 3,855,009. After appropriate preparation of a major surface of a silicon wafer, oxygen ions are implanted into the wafer through the major surface. As is well known, such ions come to rest in a relatively narrow subsurface region of the matrix, with the mean depth of penetration (and
35 thickness of the oxygen-rich layer) depending on the energy of the ions. The '009 patent teaches that, after heat treating of the implanted wafer at a temperature between 1000 and 1200 °C to anneal out damage in the Si overlayer and to cause formation of the SiO_2 layer from the implant, the thickness of the Si overlayer is increased by deposition of Si. Semiconductor devices can then be formed in the epitaxial silicon overlayer in a known manner.

40 The '009 patent also teaches that buried silicon carbide and silicon nitride layers can be formed in substantially the same manner, by implantation of, respectively, carbon or nitrogen ions. This prior art technique for forming a silicon heterostructure thus comprises implantation of relatively light ions into a silicon wafer, with the resulting buried silicon compound layer being non single crystal and nonepitaxial with the silicon matrix.

45 Recently some work has also been done that involves implantation of relatively heavy ions into silicon. See M. N. Kozicki et al, Institute of Physics Conference Series, No. 67, Section 3, pages 137-142 (1983). These authors report on the implantation of cobalt and chromium ions into polycrystalline silicon. The use of relatively high implantation energies (350 keV) resulted in the formation of a buried region of average composition of one metal atom to two silicon atoms. The implanted samples were subjected to a
50 conventional furnace anneal (900, 950, or 1025 °C) or to an electron beam anneal. The technique did not result in the formation of a homogeneous epitaxial buried layer. F. H. Sanchez et al, Proceedings of the Materials Research Society Symposium, Vol. 51, pages 439-444, (1985) discloses implantation of Cr, Fe, Co, and Ni ions into single crystal silicon samples. No buried layer was formed.

55 The prior art thus does not know any implantation method that results in formation of a buried single crystal layer that is epitaxial with the matrix. Furthermore, silicide layers formed by the prior art implantation process typically have a relatively low conductivity, due to the presence of grain boundaries, line and point defects, and possibly two or more phases. The relatively low conductivity and high defect density make such prior art buried silicide layers unacceptable for applications such as metal base transistors, and at

least reduce their usefulness as a conductor material in multilayer integrated devices. On the other hand, the prior art deposition method can be used to produce epitaxial layers of silicide or other materials on silicon, and to form epitaxial silicon thereon, resulting in formation of buried layers of epitaxial silicide or other materials. However, these deposition processes are slow, can only be successfully practiced under
 5 extremely clean high vacuum conditions (thus typically do not lend themselves readily to practice in a manufacturing environment), tend to result in structures with interfacial impurities, and lead to incorporation of substantially all of the impurities in the starting material into the silicide.

In view of the potential significance of articles such as semiconductor devices comprising buried, high quality epitaxial single crystal layers of metal silicides and possibly other materials, a method for forming
 10 such buried layers that can be practiced in a manufacturing environment with commonly available apparatus that has the potential of high throughput, that inherently leads to substantially impurity-free interfaces and to the elimination of impurities that are present in at least one of the starting materials, is of substantial interest. This application discloses such a method.

15 Glossary and Definitions

By "mesotaxy" we mean herein the process of direct formation of a substantially single crystal second material body (typically a thin layer) within a substantially single crystal first material matrix (with the first and second materials differing in their chemical composition), such that the second material body is
 20 epitaxial with the first material matrix. Mesotaxy is thus fundamentally different from epitaxy, which refers to the formation of a second material layer on a first material, with the layer being epitaxial with the substrate.

A "single crystal" or "monocrystalline" body herein is a body of crystalline material that has essentially the same crystalline orientation throughout the body. In agreement with current usage, a body is considered to be a single crystal body even though it may contain defects such as dislocations.

25 One crystalline body herein is "epitaxial" with another crystalline body in contact with the former if at least two crystal lattice directions are continuous across the interface between the two bodies.

By a "heterostructure" we mean herein a structure (typically a multilayer structure) that comprises a multiplicity of compositionally distinct regions (typically compositionally distinct layers).

30 A "heteroepitaxial" structure herein is a heterostructure in which at least one region is epitaxial with another, compositionally distinct, region. Typically, one layer is epitaxial with a chemically distinct contact-ing layer.

Summary of the Invention

35 We describe here a new approach (to be referred to as "mesotaxy") to the formation of a heteroepitax-ial structure that comprises a second material layer embedded in a first material matrix. It involves implantation of ions into a single crystal body and appropriate heat treatment of the implanted body.

Although the new method is described herein largely in terms of the formation of a buried metal silicide (primarily CoSi_2 , CrSi_2 , TiSi_2 and NiSi_2) layer in a silicon matrix, we expect that other semiconductors (e.g.,
 40 Ge), and possible compound semiconductors such as III-V and II-VI semiconductor and even other classes of matrices (e.g., metals or insulators), and other atomic implantation species (e.g., Y or Mg into Si, and combinations of implantation species, e.g., Co and Ni) can be found that are thermodynamically and crystallographically suited for mesotaxy. Therefore, we present first a general description of the technique.

The inventive method comprises providing a single crystal body (exemplarily a semiconductor wafer)
 45 having a major surface, and implanting ions of at least one (frequently relatively heavy) chemical species at a predetermined mean depth below the major surface of the body, such that a buried layer that is relatively rich in the implanted species is formed. Subsequent to the implantation the implanted body is heat treated. The implantation and heat treatment conditions are chosen such that the buried species-rich layer is transformed into the second material layer. The second material is a substantially stoichiometric compound
 50 that differs from the first material and comprises the implanted species. The conditions are also chosen such that the resulting buried second material layer is substantially single crystal and epitaxial with the first material matrix. The second material layer and the first material/second material interfaces are substantially free of impurities.

The thus produced heterostructure can then be processed in any appropriate way to form an article,
 55 exemplarily an electronic, optical or optoelectronic device or devices. Processing techniques are well known in the art. See, for instance, D. J. Elliot, "Integrated Circuit Fabrication Technology," McGraw-Hill, 1982.

We know of no existing technologically significant process that meets the above description. However general the method may be, we currently consider its application to heteroepitaxial Si/metal silicide/Si

structures to be especially significant since, inter alia, it can result in buried silicide layers of exceptionally high crystalline and/or electronic quality that offer promise for high quality device applications. Furthermore, we know of nothing in the prior art to suggest that mesotaxy might be possible, and we consider our discovery of mesotaxy to be indeed surprising. This object is achieved by a method as claimed in claim 1.

Brief Description of the Drawing

FIG. 1 is a schematic representation of an exemplary three-layer heteroepitaxial structure according to the invention;

FIG. 2 shows as-implanted RBS yields for a Co-implanted Si matrix;

FIG. 3 shows RBS yields for the Co-implanted Si matrix after heat treatment; and

FIG. 4 schematically depicts an exemplary device according to the invention.

Detailed Description

A feature of the inventive technique is the implantation of (frequently relatively heavy) ions into a substrate body such that a buried layer rich in the implanted species is formed. Although the prior art knows an example of the high energy (350 keV) implantation of Co and Cr into polycrystalline Si such that a buried metal-rich layer was formed (see Kozicki et al, op. cit.), those skilled in the art generally expect that sputtering of the semiconductor target by the ions will impose a relatively low limit on the achievable concentration of the implanted species. See, for instance, Z. L. Liau et al, *Journal of Vacuum Science and Technology*, Vol. 15, pp. 1629-1635 (1978). Also, see FIG. 1 of Sanchez et al (op. cit.), which shows that a buried layer was not formed under the conditions of the implantation. However, we have shown that, despite the widespread expectation to the contrary, buried layers rich in a relatively heavy (atomic number > 8, typically > 20) element can indeed be formed by ion implantation using commercially available implanters.

A further and very significant feature of the inventive technique is a solid state reaction between the semiconductor and the implanted species under conditions that favor formation of the desired compound, and also favor formation of the compound as a buried single crystal epitaxial with the matrix in which it is embedded. This typically requires, inter alia, that the lattice structure and lattice constant of the semiconductor and of the compound be substantially matched, with the lattice constants generally differing by less than about 5%.

FIG. 1 schematically represents an exemplary three-layer heterostructure according to the invention. It shows essentially single crystal lower and upper first material (e.g., semiconductor) layers 10 and 12, with an essentially single crystal compound layer 11 therebetween. As discussed above, 11 is epitaxial with both 10 and 12.

As will be readily appreciated by those skilled in the art, devices can be formed directly in a semiconductor overlayer 12, or 12 can form the substrate for the formation of one or more further layers. For instance, the thickness of 12 can be increased by a known method for the growth of an epitaxial semiconductor layer on a substrate of the same semiconductor, and subsequently, devices can be formed in the top layer. See, for instance, the '009 patent. On the other hand, a heteroepitaxial layer of another semiconductor (e.g., GaAs) could be grown on, e.g., a Si layer 12 by a known technique, and devices formed in the top layer.

It will also be appreciated by those skilled in the art that a controlled dose of the ions can be implanted substantially uniformly into either all or a significant part of the major surface of a semiconductor substrate, or that the implantation can be localized such as to yield a patterned implant layer (possibly using different doses in different regions). In the latter case a patterned mask layer on the substrate or a programmable focused ion beam can be used to produce the patterned implant. Furthermore, since the implant depth is directly related to the ion energy, it is possible to create buried compound regions of varying distance from the surface. This ability may, for instance, be advantageously used to create a multilevel conductor arrangement in VLSI chips.

We now describe in detail a particular exemplary embodiment of the invention, namely, the formation by mesotaxy of a buried epitaxial layer of CoSi_2 in a Si matrix. As is well known, Co and Si form a number of compounds, Co_2Si , CoSi , CoSi_2 , of which only the last has the requisite crystal structure and lattice constant to make epitaxy with Si possible. Thus, the implant conditions and the heat treatment have to be chosen such that CoSi_2 is formed. Other constraints will be discussed below.

Exemplarily, we used a 200 keV, $\sim 20 \mu\text{A}/\text{cm}^2$, scanned $^{59}\text{Co}^+$ beam. Both (100) and (111) orientation Si wafers were used as substrates. The major surface was prepared in a conventional manner, and the substrate typically was tightly clamped to a stainless steel block typically maintained at a temperature in the

range 300-500 °C. However, some beam heating of the substrate cannot be ruled out.

After implantation, the sample is subjected to a heat treatment, as will be described in more detail below. Since the heat treatment causes essentially all of the implanted Co to contribute to the formation of the buried CoSi₂ layer, it is easy to determine the dose required to result in a given thickness of buried layer. For instance, a thickness of 0.1 μm CoSi₂ requires implantation of approximately $2.5 \cdot 10^{17}/\text{cm}^2$ of Co.

FIG. 2 shows Rutherford Backscattering Spectroscopy (RBS) yields for a random and a channeled (100) direction in an as-implanted (100) Si substrate, with 20 and 21 indicating the (100) channeled and random yields, respectively. Such RBS yields are a commonly accepted indicator of crystalline quality. The implant conditions were: substrate nominally at 350 °C, 200 keV, $3 \cdot 10^{17}/\text{cm}^2$ Co. FIG. 2 shows that the implanted Co is buried beneath the Si surface, with the peak Co concentration of 27.5 atomic % appearing at a depth of about 115 nm. FIG. 2 also shows that the as-implanted Co-rich region has some degree of crystalline order in registry with the Si matrix, (χ_{min} about 55%) but definitely is not device-grade material. χ_{min} is the minimum observed ratio of RBS yield in the channeling direction to that in the random direction, and is a standard measure of crystalline quality. A low temperature anneal (1 hour at 600 °C) resulted in only slight changes in the RBS Co profile, indicating some redistribution of the Co with little improvement in crystallinity.

A subsequent high temperature treatment (1/2 hour at 1000 °C), however, produced a dramatic transformation, as can be seen from FIG. 3, wherein 30 and 31 refer to the channeled and random yields, respectively. The Co profile has abrupt edges, the characteristic yield for stoichiometric CoSi₂, and a greatly reduced channeling yield (the latter being indicative of the high crystalline quality of the buried layer), e.g., χ_{min} about 12%.

FIG. 3 also indicates that the buried layer is epitaxial with the Si matrix, and that the crystalline quality of the top Si layer is substantially improved, as compared to the as-implanted condition. The dashed line 31 was obtained by computer simulation of the random RBS spectrum for a 110 nm layer of CoSi₂ sandwiched between a 60 nm top layer of Si and a Si bottom layer of effectively infinite thickness, and is in excellent agreement with the measured spectrum. Buried layers according to the invention typically have a χ_{min} substantially smaller (at least 50% smaller) than the as-implanted χ_{min} in the same sample.

In summary, FIGS. 2 and 3 show that under the indicated conditions, a heteroepitaxial structure (Si/CoSi₂/Si) of high crystalline quality can be produced by mesotaxy. Other experimental results agree with and amplify this conclusion. For instance, cross-section transmission electron microscopy also shows that the CoSi₂ region is single crystal material epitaxial with the matrix. High resolution transmission electron microscopy of the Si/CoSi₂ interfaces shows them to be abrupt, epitaxial, and essentially smooth. The relative smoothness of the interface in the (100) orientation is of particular interest, since CoSi₂ (and other silicides) cannot be grown without substantial faceting on (100) Si by other solid state methods. Since devices are most commonly fabricated on (100) Si, the presence of faceted interfaces in prior art Si/CoSi₂ heteroepitaxial structures is a considerable disadvantage. The inventive technique is essentially free of this shortcoming.

Another problem associated with prior art techniques is the difficulty of obtaining high purity buried layers and atomically clean interfaces. As will be appreciated by those skilled in the art, the presence of impurities results in higher resistivity and/or interface states which can negatively affect the operating characteristics of devices formed in such material. This problem is not present in the inventive technique, since the implantation technique inherently results in removal of all but the wanted atomic species from the beam, and since the interfaces are never exposed.

RBS is not the only experimental technique to yield quantitative information on the quality of the buried layer. The resistance ratio (RR, defined as $R(T = 300 \cdot \text{K})/R(T = 4.2 \cdot \text{K})$, where R is the resistivity and T the absolute temperature) of a buried conductive layer can be determined and is known to be a sensitive indicator of the structural integrity, crystalline defect density, interface roughness, chemical purity and deviations from stoichiometry of the layer, with a large value of the RR being indicative of high quality material. In buried metallic layers produced according to the invention the RR typically is substantially greater than 1, preferably > 5. For instance, the RR of a CoSi₂ layer embedded in Si and produced by mesotaxy substantially as described above was found to be 15.48, which is almost a factor of 2 greater than that of the best prior art epitaxial CoSi₂.

Typically several process parameters have to be chosen properly in order to achieve mesotaxy. Among these parameters generally are the substrate temperature during implantation, the ion energy and dose, and the annealing temperature and time. Since the proper parameter values are expected to be, at least to some extent, dependent on the nature of the substrate and of the implant species, no generally valid parameter values can be given. However, based in part on our experience in the mesotaxy of CoSi₂ in Si, it

appears that the substrate advantageously is maintained above room temperature (e.g., 300-500 °C for Si) to avoid amorphization and/or to aid in the diffusion of the implanted species in the matrix. Furthermore, the ion energy has to be relatively high (e.g., above 100 keV) in order to form a buried layer and to avoid loss of the implanted species due to sputtering, and the ion dose has to be high enough such that stoichiometry can be attained by annealing. Still further, the annealing temperature has to be high enough such that compound formation as well as atomic rearrangement in the matrix can take place, yet be low enough such that degradation of the buried compound layer (manifested, for instance, by an increase in resistivity) is avoided. For instance, in the Si/CoSi₂/Si system we found that annealing in the 600-850 °C range generally results in some improvement of the quality of the buried layer (RR increases by about 3-4 from the as-implanted condition), but that annealing in the range 850-1100 °C (preferably about 1000 °C) results in much greater improvement. Annealing above about 1100 °C resulted in deterioration of the quality of the buried layer. However, at least in some cases it may be advantageous to have a multi-step heat treatment, e.g., with a low temperature anneal followed by a high temperature anneal.

In mesotaxy the buried layer is protected at all times by the top semiconductor layer. As a consequence the annealing temperature can be higher than is possible in the prior art deposition method. This is a further advantage of the inventive technique, since higher annealing temperature typically results in improved quality of the buried layer as well as of the top semiconductor layer.

TABLE 1

Orientation	Dose (ions/cm ³)	SS Stage T	Annealing T/time	X _{min}	RR
(100)	2x10 ¹⁷	RT	as implanted + 500 °C, 1 hr + 600 °C, 1 hr		1.69 2.70
(100)	3x10 ¹⁷	350 °C	as implanted + 600 °C, 1 hr + 1000 °C, 1/2 hr + 1200 °C, 1/2 hr	55% 49% 12% 12%	1.19 4.30 15.48 11.91
(100)	3x10 ¹⁷	450 °C	as implanted + 600 °C, 1 hr + 1000 °C, 1/2 hr + 1100 °C, 1/2 hr	50% 29% 12% 12.7%	84 5.03 11.48 10.75
(111)	3x10 ¹⁷	350 °C	as implanted + 600 °C, 1 hr + 1000 °C, 1/2 hr	43% 25% 7.8%	1.11 6.50 6.50
(111)	3x10 ¹⁷	450 °C	as implanted + 600 °C, 1 hr + 1000 °C, 1/2 hr	59% 35% 6.9%	1.04 4.00 7.82
(111)	2x10 ¹⁷	450 °C	as implanted + 600 °C, 1 hr + 1000 °C, 1 hr	67% 49% 6.4%	1.00 2.51 5.37
Notes: The third column gives the nominal temperature (T) of the stainless steel stage during ion implantation, and the last column gives values of the previously defined resistance ratio (RR).					

Some of these results are exemplified by the data contained in Table 1, which pertains to the Si/CoSi₂/Si system, with Co implantation at 200 keV. As can be seen from the data in Table 1, the detailed characteristics of the buried layer may depend on the substrate orientation. For instance, whereas the (100) orientation yielded buried layers having X_{min} of about 12% and RR > 10, the (111) orientation yielded layers with X_{min} of about 7% and RR < 7.

We would like to further illustrate the above points by citing conditions which we found not to result in successful growth of a buried CoSi₂ layer in Si. Implantation temperatures of 77 °K, room temperature, and 260 °C all resulted in an amorphous Si surface and/or failure to form a buried Co-rich layer. Frequently, when annealing such low temperature implant samples at 1000 °C, migration of the Co to the surface was

also observed. Doses of $1 \cdot 10^{16}$, $5 \cdot 10^{16}$, and $1 \cdot 10^{17}/\text{cm}^2$ did not result in formation of a stoichiometric layer under the annealing conditions used by us.

Various device applications based on the basic structure depicted in FIG. 1 are contemplated. An exemplary schematic device structure is shown in FIG. 3 of the '009 patent and described in columns 4 and 5 of the patent. Mesotaxy may also be advantageously used in optical and optoelectronic devices.

Other contemplated device applications of mesotaxy include a MOSFET comprising a backside gate, and a MOSFET or other device comprising a buried ground plane. The latter application is schematically illustrated in FIG. 4, wherein regions 40, 41, and 42 exemplarily are p, p⁺ and p⁺ conductivity type, respectively, 43 refers to patterned oxide, 44 refers to metallization regions, and 45 is a metallized via hole whereby contact is made to the buried ground plane 11, formed by mesotaxy. Indicated are also means for making electrical contact to the source and drain regions and the gate.

By means of mesotaxy it may also be possible to form a semiconductor layer within another semiconductor (e.g., CrSi₂ within Si), the two semiconductors having different bandgaps. Such combinations, which previously have only been produced by MBE, are known to have interesting characteristics that make possible useful electronic devices such as heterojunction transistors. By means of a further implant (e.g., Co) a portion of the buried epitaxial semiconductor layer can be converted into a metal, opening up device design possibilities not previously available. Furthermore, more than one atomic species can be implanted into the same region. For instance, implantation of Co and Ni into Si is expected to result in formation of the epitaxial ternary silicide Co_xNi_{1-x}Si₂, which is known to have advantageous conductive characteristics.

Example I: A (100) oriented Si wafer, cleaned by means of a conventional technique, was attached in a commercially available ion implanter to a stainless steel block maintained at about 350 °C, with this temperature considered to be the nominal implant temperature. A mass analyzed beam (200keV, 40 μA, about 10 μA/cm²) of ⁵⁹Co⁺ from a Freeman ion source was directed 7° off normal at the Si wafer. The implanted dose was $3 \cdot 10^{17}/\text{cm}^2$. After completion of the implant the wafer was maintained in vacuum ($\sim 10^{-7}$ Torr) for about 1 hour at 600 °C, followed by a 30 minute vacuum anneal at 1000 °C. The thus produced heterostructure contains an approximately 100 nm thick buried single crystal CoSi₂ layer, with a 60 nm single crystal Si overlayer. The structure is heteroepitaxial, with the CoSi₂ layer having $x_{\text{min}} \sim 12\%$ and RR ~ 15 , and the Si overlayer having $x_{\text{min}} \sim 15\%$.

Example II: A CoSi₂ layer is formed by mesotaxy in a (111)-oriented Si wafer substantially as described in Example I, except that the nominal implant temperature is about 300 °C, the ion energy is 400keV, the implant dose is $5 \cdot 10^{17}/\text{cm}^2$, the thickness of the epitaxial CoSi₂ layer is about 170 nm, and that of the Si overlayer is about 130 nm.

Example III: A Co_{0.5}Ni_{0.5}Si₂ layer is formed by mesotaxy in a (100) oriented Si wafer substantially as described in Example I, except that substantially equal numbers of Co and Ni ions are implanted sequentially. The resulting epitaxial tertiary silicide layer has high conductivity and is of good crystalline quality.

Example IV: A buried epitaxial CoSi₂ layer is formed by mesotaxy substantially as described in Example I, except that the nominal implant temperature is about 500 °C, the ion energy is about 1.5 MeV and the ion dose is about $7 \cdot 10^{17}/\text{cm}^2$. In the Si overlayer of the resulting heteroepitaxial structure MOS devices are produced by conventional techniques, including providing electrical contact to the buried CoSi₂ layer such that the buried layer serves as buried ground plane.

Example V: A Si/CoSi₂/Si heteroepitaxial structure is formed substantially as described in Example I. On the Si overlayer a 0.5 μm epitaxial layer of Si is grown by MBE.

Example VI: A heteroepitaxial structure is formed substantially as in Example V, except that on the Si overlayer a 0.5 μm epitaxial layer of GaAs is grown by MBE.

Example VII: A (100) oriented Ge wafer is cleaned by a conventional process and Co implanted therein substantially as described in Example I, except that the nominal implant temperature is 150 °C, the ion energy is 300 keV, and the implanted wafer is annealed at 750 °C. A buried epitaxial layer of CoGe₂ is thus formed.

Claims

1. A method of manufacturing a semiconductor device comprising a first material body and a second material layer embedded within the body, the method comprising
 - a) providing a single crystal semiconductor first material body having a major surface;
 - b) implanting at least one chemical species into the first material body at a predetermined mean depth below the major surface of the body such that a buried species-rich layer results;



also observed. Doses of $1 \cdot 10^{16}$, $5 \cdot 10^{16}$, and $1 \cdot 10^{17}/\text{cm}^2$ did not result in formation of a stoichiometric layer under the annealing conditions used by us.

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By means of mesotaxy it may also be possible to form a semiconductor layer within another semiconductor (e.g., CrSi₂ within Si), the two semiconductors having different bandgaps. Such combinations, which previously have only been produced by MBE, are known to have interesting characteristics that make possible useful electronic devices such as heterojunction transistors. By means of a further implant (e.g., Co) a portion of the buried epitaxial semiconductor layer can be converted into a metal, opening up device design possibilities not previously available. Furthermore, more than one atomic species can be implanted into the same region. For instance, implantation of Co and Ni into Si is expected to result in formation of the epitaxial ternary silicide Co_xNi_{1-x}Si₂, which is known to have advantageous conductive characteristics.

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Example II: A CoSi₂ layer is formed by mesotaxy in a (111)-oriented Si wafer substantially as described in Example I, except that the nominal implant temperature is about 300 °C, the ion energy is 400keV, the implant dose is $5 \cdot 10^{17}/\text{cm}^2$, the thickness of the epitaxial CoSi₂ layer is about 170 nm, and that of the Si overlayer is about 130 nm.

Example III: A Co_{0.5}Ni_{0.5}Si₂ layer is formed by mesotaxy in a (100) oriented Si wafer substantially as described in Example I, except that substantially equal numbers of Co and Ni ions are implanted sequentially. The resulting epitaxial tertiary silicide layer has high conductivity and is of good crystalline quality.

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Claims

1. A method of manufacturing a semiconductor device comprising a first material body and a second material layer embedded within the body, the method comprising
 - a) providing a single crystal semiconductor first material body having a major surface;
 - b) implanting at least one chemical species into the first material body at a predetermined mean depth below the major surface of the body such that a buried species-rich layer results;



- c) heat treating the implanted body such that the buried species-rich layer is transformed into the second material layer, the second material being a substantially stoichiometric compound different from the first material and comprising the implanted chemical species; and
d) completing the manufacture of the semiconductor device;

CHARACTERIZED IN THAT

- e) the chemical species, implant and heat treatment conditions are chosen such that the second material layer is a substantially single crystal layer (11) epitaxial with the first material body (10,12) in which the second material layer is embedded, with the lattice mismatch between first and second material being less than 5%, and with the first material body during ion implantation having a nominal temperature above room temperature.
2. The method of claim 1, wherein the ions are implanted with an energy of at least about 100keV, and wherein said chemical species is selected from the group of elements having atomic number greater than 8.
 3. The method of claim 1, wherein the semiconductor is selected from the group consisting of Si and Ge.
 4. The method of claim 3, wherein the semiconductor is silicon, and wherein the chemical species is selected from the group consisting of Co, Ni, Cr, Ti, Y, and Mg.
 5. The method of claim 4, wherein during ion implantation the semiconductor body has a nominal temperature in the range from about 300 °C to about 500 °C, the ions are implanted with an energy of at least about 100 keV, and step c) comprises heating the ion implanted substrate to a temperature in the range from about 800 °C to about 1100 °C.
 6. The method of claim 4, wherein the second material is a member of the group consisting of CoSi_2 , NiSi_2 , CrSi_2 , TiSi_2 and $\text{Co}_x\text{Ni}_{1-x}\text{Si}_2$, with $0 < x < 1.0$.
 7. The method of claim 1, wherein the article comprises an electronic device, and step d) comprises providing means for making electrical contact with the second material layer.
 8. The method of claim 4, wherein the major surface is at least approximately a (100) surface.
 9. The method of claim 3, wherein the semiconductor body is a Ge body, and wherein the chemical species is Co.
 10. The method of claim 1, wherein step d) comprises epitaxially depositing material on the major surface.
 11. The method of claim 10, wherein the semiconductor body is a Si body, and wherein the epitaxially deposited material is chosen from the group consisting of Si and GaAs.

Patentansprüche

1. Verfahren zur Herstellung einer Halbleitereinrichtung mit einem Körper eines ersten Materials und einer in dem Körper eingebetteten Schicht eines zweiten Materials, wobei das Verfahren umfaßt:
 - a) Bereitstellen eines einkristallinen Körpers des ersten Materials mit einer Hauptoberfläche,
 - b) Implantieren wenigstens einer chemischen Spezies in den Körper des ersten Materials bei einer vorbestimmten mittleren Tiefe unter der Hauptoberfläche des Körpers, sodaß sich eine vergrabene Schicht, die reich an der Spezies ist, ergibt,
 - c) Wärmebehandeln des implantierten Körpers, sodaß die vergrabene an der Spezies reiche Schicht in die zweite Materialschicht umgesetzt wird, wobei das zweite Material eine im wesentlichen stöchiometrische Zusammensetzung ist, die verschieden vom ersten Material ist und die implantierte chemische Spezies umfaßt, und
 - d) Vervollständigen der Herstellung des Halbleiterkörpers, dadurch gekennzeichnet, daß
 - e) die chemische Spezies, die Implantierungs- und Wärmebehandlungsbedingungen so ausgewählt sind, daß die Schicht zweiten Materials eine im wesentlichen einkristalline Schicht (11) ist, die zu dem Körper ersten Materials (10, 12) in welchem die Schicht zweiten Materials eingebettet ist, im



wesentlichen epitaxial ist, wobei die Gitterfehlpassung zwischen erstem und zweitem Material weniger als 5% beträgt und wobei der Körper ersten Materials während der Ionenimplantierung eine Nenntemperatur oberhalb von Raumtemperatur hat.

- 5 2. Verfahren nach Anspruch 1, in welchem die Ionen mit einer Energie von wenigstens 100 keV implantiert werden, und in welchem die chemische Spezies aus der Gruppe der Elemente mit einer Protonenzahl größer als 8 ausgewählt ist.
3. Verfahren nach Anspruch 1, in welchem der Halbleiter aus der aus Si und Ge bestehenden Gruppe ausgewählt ist.
4. Verfahren nach Anspruch 3, in welchem der Halbleiter Silicium ist und in welchem die chemische Spezies aus der aus Co, Ni, Cr, Ti, Y und Mg bestehenden Gruppe ausgewählt ist.
- 15 5. Verfahren nach Anspruch 4, in welchem während der Ionenimplantation der Halbleiterkörper eine Nenntemperatur im Bereich von ungefähr 300 °C bis ungefähr 500 °C hat, die Ionen mit einer Energie von wenigstens 100 keV implantiert werden und Schritt c) das Heizen des mit Ionen implantierten Substrats auf eine Temperatur im Bereich von ungefähr 800 °C bis ungefähr 1100 °C umfaßt.
- 20 6. Verfahren nach Anspruch 4, in welchem das zweite Material ein Mitglied der Gruppe ist, die aus CoSi_2 , NiSi_2 , CrSi_2 , TiSi_2 und $\text{Co}_x\text{Ni}_{1-x}\text{Si}_2$, mit $0 < x < 1,0$, besteht.
7. Verfahren nach Anspruch 1, in welchem der Gegenstand eine elektronische Einrichtung umfaßt und Schritt d) die Bereitstellung von Einrichtungen zur Herstellung elektrischen Kontaktes zur Schicht zweiten Materials umfaßt.
- 25 8. Verfahren nach Anspruch 4, in welchem die Hauptoberfläche wenigstens angenähert eine (100)-Oberfläche ist.
- 30 9. Verfahren nach Anspruch 3, in welchem der Halbleiterkörper ein Ge-Körper ist und in welchem die chemische Spezies Co ist.
10. Verfahren nach Anspruch 1, in welchem Schritt d) das epitaxiale Abscheiden von Material auf der Hauptoberfläche umfaßt.
- 35 11. Verfahren nach Anspruch 10, in welchem der Halbleiterkörper ein Si-Körper ist und in welchem das epitaxial abgeschiedene Material aus der Gruppe ausgewählt ist, die aus Si und GaAs besteht.

Revendications

- 40 1. Procédé de fabrication d'un dispositif semi-conducteur comprenant un corps de premier matériau et une couche de second matériau incluse dans le corps, le procédé comprenant les étapes qui consistent à
 - 45 a) se munir d'un corps de premier matériau semi-conducteur monocristallin ayant une surface majeure;
 - b) implanter au moins une espèce chimique dans le corps de premier matériau sur une épaisseur moyenne pré-déterminée au-dessous de la surface majeure du corps, pour obtenir une couche enfouie riche en espèces;
 - 50 c) soumettre le corps comportant l'implantation à un traitement thermique, pour que la couche enfouie riche en espèces se transforme en couche de second matériau, le second matériau étant un composé sensiblement stoechiométrique différent du premier matériau et comprenant l'espèce chimique implantée; et
 - d) terminer la fabrication du dispositif semi-conducteur;
- CARACTERISE EN CE QUE
- 55 e) l'espèce chimique, les conditions d'implantation et de traitement thermique sont choisies de manière à ce que la couche de second matériau soit sensiblement une couche monocristalline (11) épitaxiale avec le corps de premier matériau (10, 12) dans lequel est incluse la couche de second matériau, le décalage de réseau entre le premier matériau et le second matériau étant inférieur à



5%, et le corps de premier matériau ayant une température nominale supérieure à la température ambiante durant l'implantation des ions.

- 5 2. Procédé selon la revendication 1, dans lequel les ions sont implantés avec une énergie d'au moins environ 100 keV et dans lequel ladite espèce chimique est choisie dans le groupe d'éléments ayant un numéro atomique supérieur à 8.
- 10 3. Procédé selon la revendication 1, dans lequel le semi-conducteur est choisi dans le groupe constitué de Si et Ge.
- 15 4. Procédé selon la revendication 3, dans lequel le semi-conducteur est du silicium et dans lequel l'espèce chimique est choisie dans le groupe constitué de Co, Ni, Cr, Ti, Y et Mg.
- 20 5. Procédé selon la revendication 4, dans lequel, au cours de l'implantation des ions, le corps semi-conducteur a une température nominale dans la gamme d'environ 300 °C à environ 500 °C, les ions sont implantés avec une énergie d'au moins environ 100 keV et l'étape c) comprend le chauffage du substrat comportant les ions implantés à une température dans la gamme d'environ 800 °C à environ 1100 °C.
- 25 6. Procédé selon la revendication 4, dans lequel le second matériau appartient au groupe constitué par CoSi_2 , NiSi_2 , CrSi_2 , TiSi_2 et $\text{CO}_x\text{N}_{1-x}\text{Si}_2$ avec $0 < x < 1,0$.
7. Procédé selon la revendication 1, dans lequel l'article comprend un dispositif électronique et l'étape d) comprend la fourniture d'un moyen pour effectuer le contact électrique avec la couche de second matériau.
- 30 8. Procédé selon la revendication 4, dans lequel la surface majeure est au moins environ une surface (100).
- 35 9. Procédé selon la revendication 3, dans lequel le corps semi-conducteur est un corps de Ge, et dans lequel l'espèce chimique est Co.
10. Procédé selon la revendication 1, dans lequel l'étape d) comprend le dépôt épitaxial du matériau sur la surface majeure.
- 40 11. Procédé selon la revendication 10, dans lequel le corps semi-conducteur est un corps de Si et dans lequel le matériau déposé par épitaxie est choisi dans le groupe constitué de Si et GaAs.