CLAIMS

1. A method comprising:

forming a trench isolation region in a semiconductor layer of a semiconductor device by using a first dielectric material, said trench isolation region laterally delineating an active region in said semiconductor layer;

forming a cap layer on said first dielectric material by using a second dielectric material, said first and second dielectric materials having different material composition; and

forming a gate electrode structure on said active region and said trench isolation region including said cap layer.

2. The method of claim 1, wherein forming a gate electrode structure comprises forming a gate insulation layer so as to include a high-k dielectric material and forming a metal containing electrode material above said gate insulation layer.

3. The method of claim 2, wherein forming said gate electrode structure further comprises forming a protective liner on sidewalls of said gate insulation layer and said metal containing electrode material.

4. The method of claim 1, wherein forming said cap layer comprises filling an isolation trench at least with said first dielectric material, recessing said first dielectric material and forming said second dielectric material on said recessed first dielectric material.

5. The method of claim 4, wherein recessing said first dielectric material comprises adjusting a height level of said first dielectric material so as to be below a height level of a surface of said semiconductor layer.

6. The method of claim 1, further comprising forming a semiconductor alloy on said active region prior to forming said gate electrode structure.

7. The method of claim 6, wherein forming said semiconductor alloy comprises recessing said active region and selectively depositing said semiconductor alloy in said recess.

8. The method of claim 1, further comprising forming a cavity in said active region in the presence of said gate electrode structure and forming a strain inducing semiconductor material in said cavity.

9. The method of claim 8, wherein said strain inducing semiconductor material comprises at least one of germanium, tin and carbon.

10. A method comprising:

forming a trench isolation region in a semiconductor layer of a semiconductor device by recessing a first dielectric material of said trench isolation region and forming a second dielectric material as a cap layer on said recessed first dielectric material; and

forming a gate electrode structure on said cap layer of said trench isolation region, said gate electrode structure comprising a high-k dielectric material.

11. The method of claim 10, wherein recessing said first dielectric material comprises adjusting a height level of said first dielectric material so as to be below a height level of a surface of said semiconductor layer.

12. The method of claim 10, wherein forming a second dielectric material as a cap layer comprises depositing a silicon and nitrogen containing layer and performing a planarization process.

13. The method of claim 10, further comprising, prior to forming said gate electrode structure, forming a semiconductor alloy on an active region that

is laterally delineated in said semiconductor layer by said trench isolation region.

14. The method of claim 11, wherein forming said gate electrode structure comprises forming a layer stack comprising a gate insulation layer including said high-k dielectric material and a metal containing electrode material above said gate insulation layer, patterning said layer stack and forming a protective liner on sidewalls of said patterned layer stack.

15. The method of claim 14, further comprising forming cavities in an active region that is laterally delineated in said semiconductor layer by said trench isolation region and forming a strain inducing semiconductor alloy in said cavities.

16. The method of claim 10, further comprising forming a first mask layer on said semiconductor layer and forming a second mask layer on said first mask layer and using said first and second mask layers as an etch mask for forming a trench in said semiconductor layer.

17. The method of claim 16, wherein said first mask layer comprises a silicon oxide material and has a thickness of approximately 10 nm (nanometer) or more.

18. A semiconductor device comprising:

a trench isolation region laterally delineating an active region in a semiconductor layer, said trench isolation region comprising a first dielectric material and a second dielectric material formed on said first dielectric material, said first and second dielectric materials differing in material composition; and

a gate electrode structure formed on a channel area of said active region, said gate electrode structure comprising a material system comprising a high-k dielectric material and a metal containing electrode material, said gate electrode structure further comprising a protective liner formed on

sidewalls of said high-k dielectric material and said metal containing electrode material.

19. The semiconductor device of claim 18, wherein said channel region comprises a semiconductor alloy.

20. The semiconductor device of claim 18, wherein said first dielectric material extends to a height level that is less than a height level of an interface formed by a gate insulation layer of said gate electrode structure and said channel region.

What is claimed:

1. A method, comprising: forming a dual layer patterned hard mask layer comprised of a first mask layer formed on a surface of a semiconductor layer and a second mask layer formed on said first mask layer; forming a trench through said dual layer patterned hard mask layer and into said semiconductor layer; forming a trench isolation region in said semiconductor layer of a semiconductor device by using a first dielectric material, said trench isolation region laterally delineating an active region in said semiconductor layer; with said dual layer patterned hard mask in position, including said second mask layer, forming a cap layer on the trench isolation region comprised of said first dielectric material by overfilling said trench with a second dielectric material, said first and second dielectric materials having different material composition; removing said second hard mask layer while leaving said first hard mask layer positioned on said surface of said semiconductor layer; with said first hard mask layer in position, performing a recess etching process on said cap layer comprised of said second dielectric material so as to thereby define a recessed cap layer having an upper surface that is positioned at a level that is below an upper surface of said first hard mask layer; completely removing said first hard mask layer so as to thereby expose said surface of said semiconductor layer; and after completely removing said first hard mask layer, forming a gate electrode structure on said active region and said cap layer.

2. The method of claim 1, wherein forming said gate electrode structure comprises forming a gate insulation layer so as to include a high-k dielectric material and forming a metal-containing electrode material above said gate insulation layer.

3. The method of claim 2, wherein forming said gate electrode structure further comprises forming a protective liner on sidewalls of said gate insulation layer and said metal-containing electrode material.

4. The method of claim 1, wherein, prior to forming said cap layer, the method comprises recessing said first dielectric material and forming said second dielectric material on said recessed first dielectric material.

5. The method of claim 4, wherein recessing said first dielectric material comprises adjusting a height level of said first dielectric material so as to be below a height level of the surface of said semiconductor layer.

6. The method of claim 1, further comprising forming a semiconductor alloy on said active region prior to forming said gate electrode structure.

7. The method of claim 6, wherein forming said semiconductor alloy comprises recessing said active region and selectively depositing said semiconductor alloy in said recess.

8. The method of claim 1, further comprising forming a cavity in said active region in the presence of said gate electrode structure and forming a strain-inducing semiconductor material in said cavity.

9. The method of claim 8, wherein said strain-inducing semiconductor material comprises at least one of

germanium, tin and carbon.

10. A method, comprising: forming a dual layer patterned hard mask layer comprised of a first mask layer formed on a surface of a semiconductor layer and a second mask layer formed on said first mask layer; forming a trench through said dual layer patterned hard mask layer and into said semiconductor layer; forming a trench isolation region comprised of a first dielectric material in said semiconductor layer of a semiconductor device, said trench isolation region having an upper surface that is positioned at a level that is below said surface of said semiconductor layer; forming a second dielectric material as a cap layer on said upper surface of said trench isolation region, wherein said first and second dielectric materials have different material compositions, said cap layer being formed by: overfilling said trench with said second dielectric material; and performing a chemical mechanical polishing process that removes portions of said second dielectric material and said second hard mask layer and stops on said first hard mask layer thereby leaving said first hard mask layer positioned on said surface of said semiconductor layer; and forming a gate electrode structure on said active region and said cap layer, said gate electrode structure comprising a high-k dielectric material.

11. The method of claim 10, wherein forming the trench isolation region comprises overfilling the trench with the first dielectric material, performing a chemical mechanical polishing process on the first dielectric material that stops on the second hard mask layer, and performing a recess etching process on the first dielectric material to recess said first dielectric material such that the upper surface of the trench isolation region is positioned at the level that is below the upper surface of the semiconductor layer.

12. The method of claim 10, wherein the second dielectric material comprises a silicon and nitrogen-containing layer.

13. The method of claim 10, further comprising, prior to forming said gate electrode structure, forming a semiconductor alloy on an active region that is laterally delineated in said semiconductor layer by said trench isolation region.

14. The method of claim 11, wherein forming said gate electrode structure comprises forming a layer stack comprising a gate insulation layer including said high-k dielectric material and a metal-containing electrode material above said gate insulation layer, patterning said layer stack and forming a protective liner on sidewalls of said patterned layer stack.

15. The method of claim 14, further comprising forming cavities in an active region that is laterally delineated in said semiconductor layer by said trench isolation region and forming a strain-inducing semiconductor alloy in said cavities.

16. The method of claim 10, wherein said first mask layer comprises a silicon oxide material and has a thickness of approximately 10 nm or more.

17. The method of claim 1, wherein said first mask layer comprises silicon dioxide and said second mask

layer comprises silicon nitride.

18. The method of claim 10, wherein said first mask layer comprises silicon dioxide and said second mask layer comprises silicon nitride.

19. A method, comprising: forming a dual layer patterned hard mask layer comprised of a first mask layer formed on a surface of a semiconductor layer and a second mask layer formed on said first mask layer; forming a trench through said dual layer patterned hard mask layer and into said semiconductor layer; forming a trench isolation region comprised of a first dielectric material in said semiconductor layer of a semiconductor device, said trench isolation region having an upper surface that is positioned at a level that is below an upper surface of said semiconductor layer; forming a second dielectric material as a cap layer on said upper surface of said trench isolation region, wherein said first and second dielectric materials have different material compositions, said cap layer being formed by: overfilling said trench with said second dielectric material; and performing a chemical mechanical polishing process that removes portions of said second dielectric material and said second hard mask layer and stops on said first hard mask layer thereby leaving said first hard mask layer positioned on said surface of said semiconductor layer; with said first hard mask layer in position on said surface of said semiconductor layer, performing a second dielectric material recess etching process on said cap layer such that, after said second dielectric material recess etching process is completed, an upper surface of the recessed cap layer is positioned at a level that is below an upper surface of said first hard mask layer and above an upper surface of said semiconductor layer; completely removing said first hard mask layer so as to thereby expose said surface of said semiconductor layer, and after completely removing said first hard mask layer, forming a gate electrode structure on said active region and said recessed cap layer.

20. The method of claim 19, wherein said first mask layer comprises silicon dioxide and said second mask layer comprises silicon nitride.

21. The method of claim 19, wherein forming said trench isolation region comprises overfilling said trench with said first dielectric material, performing a chemical mechanical polishing process on said first dielectric material that stops on said second hard mask layer, and performing a first dielectric recess etching process on said first dielectric material.

22. The method of claim 10, further comprising, after performing said chemical mechanical polishing process, and with said first hard mask layer positioned on said surface of said semiconductor layer, performing a recess etching process on said cap layer comprised of said second dielectric material so as to thereby define a recessed cap layer having an upper surface that is positioned at a level that is below an upper surface of said first hard mask layer.

23. A device formed in accordance with the method of any one of the preceding claims.