CLAIMS

1. A memory device comprising a pillar of semiconductor material and at least one memory cell associated with the pillar, wherein each of the at least one memory cells comprises a charge trap and a transistor, wherein, for each of the at least one memory cells:

the charge trap of the memory cell is configured to store a charge and to control a threshold voltage of the transistor of the memory cell by said stored charge; and

the transistor of the memory cell comprises a source, a body, and a drain, wherein the source, body, and drain are respective pillar segments along an axial direction of the pillar, wherein a source pillar segment and a drain pillar segment are separated by a body pillar segment, wherein the transistor is either

- a NPN transistor, wherein the source pillar segment is n-doped, the body pillar segment is p-doped, and the drain pillar segment is n-doped; or

- a PNP transistor, wherein the source pillar segment is p-doped, the body pillar segment is n-doped, and the drain pillar segment is p-doped;

wherein at least one p-doped pillar segment of the transistor comprises a plurality of semiconductor layers stacked in the axial direction of the pillar, wherein layers of the plurality of semiconductor layers are made of AlGaN or GaN, and wherein the plurality of semiconductor layers is configured such that an aluminum content changes between each consecutive layer such that every second layer has a lower aluminum content than the neighboring mutually opposite layers thereof.

2. The memory device according to claim 1, wherein, for each of the at least one memory cells:

the memory cell comprises a control gate arranged at a lateral side of the pillar, the control gate being configured to control a current through the body pillar segment of the transistor by a voltage of the control gate relative to

the threshold voltage of the transistor; and

the charge trap of the memory cell is arranged between the control gate and the body pillar segment of the transistor of the memory cell, the charge trap comprising a first oxide layer, a charge trapping layer, and a second oxide layer, wherein the first oxide layer separates the charge trapping layer from the body pillar segment and the second oxide layer separates the charge trapping layer from the control gate, wherein the charge trapping layer comprises a dielectric layer and/or a conductive layer.

3. The memory device according to claim 2, wherein the first oxide layer, the charge trapping layer, the second oxide layer, and the control gate extend around a circumference of the pillar.

4. The memory device according to claim 2, wherein, for each of the at least one memory cells, the charge trapping layer of the charge trap of the memory cell comprises a high-k dielectric material.

5. The memory device according to claim 4, wherein the high-k dielectric material is selected from Y_2O_3, TiO_2, HfO_2, ZrO_2, and La_2O_3.

6. The memory device according to claim 2, wherein, for each of the at least one memory cells, one or more of: the first oxide layer and the second oxide layer comprises Al_2O_3.

7. The memory device according to claim 1, wherein, for each of the at least one memory cells, the transistor of the memory cell comprises a repetition of a pair of semiconductor layers, wherein each pair of semiconductor layers comprises

a low Al content layer, having an Al content below 10%; and

a high Al content layer, having an Al content above 15%.

8. The memory device according to claim 1, wherein, for each of the at least one memory cells, each layer, of the plurality of semiconductor layers of the at least one p-doped pillar segment of the transistor, has a thickness between 3 nm and 10 nm.

9. The memory device according to claim 1, wherein the memory device comprises a first and a second pillar, each of the first and second pillar having at least one memory cell associated with said pillar, wherein a memory cell of the first pillar and a memory cell of the second pillar share a common control gate, the common control gate being configured to simultaneously control a current through the body pillar segment of the transistor of the memory cell of the first pillar and a current through the body pillar segment of the transistor of the memory cell of the second pillar, by a voltage of the common control gate.

10. Use of the memory device according to claim 1 for analog to digital conversion, wherein conversion rules for the analog to digital conversion are stored in the memory device.

11. A method for producing a memory device, the method comprising

depositing semiconductor layers on a substrate, the semiconductor layers being stacked in a stacking direction, whereby a semiconductor structure is formed out of the deposited semiconductor layers;

etching the semiconductor structure to form a pillar, the pillar having an axial direction in the stacking direction;

forming a transistor in the pillar, the transistor comprising a source, a body, and a drain, wherein the source, body, and drain are respective pillar segments along the axial direction of the pillar, wherein a source pillar segment and a drain pillar segment are separated by a body pillar segment, wherein the transistor is either

- a NPN transistor, wherein the source pillar segment is n-doped, the body pillar segment is p-doped, and the drain pillar segment is n-doped; or

- a PNP transistor, wherein the source pillar segment is p-doped, the

body pillar segment is n-doped, and the drain pillar segment is p-doped;

wherein at least one p-doped pillar segment of the transistor comprises a plurality of semiconductor layers, of the deposited semiconductor layers, stacked in the axial direction of the pillar (40), wherein layers of the plurality of semiconductor layers of the p-doped pillar segment are made of AlGaN or GaN, and wherein the plurality of semiconductor layers of the p-doped pillar segment is configured such that an aluminum content changes between each consecutive layer such that every second layer has a lower aluminum content than the neighboring mutually opposite layers thereof;

forming a charge trap configured to store a charge and to control a threshold voltage of the transistor by said stored charge,

wherein the transistor and the charge trap are parts of a memory cell of the memory device.

12. The method according to claim 11, further comprising

lithographically defining a lateral size and a position of the pillar by imprint lithography.

13. The method according to claim 11, wherein the charge trap is formed by depositing, on a lateral side of the pillar, a first oxide layer, a charge trapping layer, a second oxide layer, and a control gate,

wherein the first oxide layer separates the charge trapping layer from the body pillar segment, and the second oxide layer separates the charge trapping layer from the control gate;

wherein the charge trapping layer comprises a dielectric layer and/or a conductive layer;

wherein the control gate is configured to control a current through the body pillar segment of the transistor, by a voltage of the control gate relative to the threshold voltage of the transistor;

wherein the first oxide layer, the charge trapping layer, the second oxide layer, and the control gate extend around a circumference of the pillar.

14. The method according to claim 13, further comprising:

etching the semiconductor structure to form a first and a second pillar, each of the first and second pillar having at least one memory cell associated with said pillar;

forming a common control gate, the common control gate being shared between a memory cell of the first pillar and a memory cell of the second pillar, the common control gate being configured to simultaneously control a current through the body pillar segment of the transistor of the memory cell of the first pillar and a current through the body pillar segment of the transistor of the memory cell of the second pillar, by a voltage of the common control gate, wherein the common control gate is formed after etching the semiconductor structure to form the first and the second pillar.

15. The method according to claim 13, wherein the first oxide layer, the charge trapping layer, and the second oxide layer are deposited by one or more conformal depositing techniques.

16. The method according to claim 15, wherein the one or more conformal depositing techniques are selected from atomic-layer deposition, chemical vapor deposition, and plasma-enhanced chemical vapor deposition.

17. The method according to claims 13, wherein the control gate is deposited by a directional depositing technique.

18. The method according to claim 17, wherein the directional depositing technique is selected from evaporation and sputtering.