Multiple-Gate Transistors Formed on Bulk Substrates

[0001] This application claims the benefit of U.S. Provisional Application No. 60/495,071, filed on August 13, 2003, entitled "Multiple-Gate Transistors Formed on Bulk Substrates," which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates to semiconductor devices and more particularly to the multiple-gate transistors formed on bulk semiconductor substrates.

BACKGROUND

[0003] The dominant semiconductor technology used for the manufacture of ultra-large scale integrated (ULSI) circuits is the metal-oxide-semiconductor field effect transistor (MOSFET) technology. Reduction in the size of MOSFETs has provided continued improvement in speed performance, circuit density, and cost per unit function over the past few decades. As the gate length of the conventional bulk MOSFET is reduced, however, the source and drain increasingly interact with the channel and gain influence on the channel potential. Consequently, a transistor with a short gate length suffers from problems related to the inability of the gate to substantially control the on and off states of the channel.

[0004] Phenomena such as reduced gate control associated with transistors with short channel lengths are termed short-channel effects. Increased body doping concentration, reduced gate oxide thickness, and ultra-shallow source/drain junctions are ways to suppress short-channel effects. However, for device scaling well into the sub-50 nm regime, the requirements for body-doping concentration, gate oxide thickness, and source/drain (S/D) doping profiles become

increasingly difficult to meet when conventional device structures based on bulk silicon (Si) substrates are employed.

[0005] For device scaling well into the sub-30-nm regime, a promising approach to controlling short-channel effects is to use an alternative transistor structure with more than one gate, i.e. a multiple-gate transistor. Prior art multiple-gate transistors are formed on silicon-on-insulator substrates. A prior art multiple-gate transistor 10 is shown in plan view in Figure 1. The structure includes a silicon fin 12 overlying an insulator layer 14, which overlies a substrate (see element 22 in Figure 2). A gate dielectric (see element 20 in Figure 2) covers a portion of the silicon fin 12, and a gate electrode 16 straddles across the silicon fin 12. The gate dielectric 20 isolates the gate electrode 16 from the silicon fin 12.

[0006] Examples of the multiple-gate transistor include the double-gate transistor, triple-gate transistor, omega field-effect transistor (FET), and the surround-gate or wrap-around gate transistor. A multiple-gate transistor structure is expected to extend the scalability of CMOS technology beyond the limitations of the conventional bulk MOSFET and realize the ultimate limit of silicon MOSFETs. The introduction of additional gates improves the capacitance coupling between the gates and the channel, increases the control of the channel potential by the gate, helps suppress short channel effects, and prolongs the scalability of the MOS transistor.

[0007] The simplest example of a multiple-gate transistor is the double-gate transistor as described in U.S. Patent No. 6,413,802 issued to Hu *et al.* As illustrated in the cross-sectional view of Figure 2a, the double-gate transistor has a gate electrode 16 that straddles across the channel or the fin-like silicon body 12, thus forming a double-gate structure. There are two gates, one on each sidewall 18 of the silicon fin 12. The plan view of the double-gate structure is shown in Figure 1.

[0008] In U.S. Patent No. 6,413,802, the transistor channel comprises a thin silicon fin 12 defined using an etchant mask 24 and formed on an insulator layer 14, e.g. silicon oxide. Gate oxidation is performed, followed by gate deposition and gate patterning to form a double-gate structure overlying the sides of the fin. Both the source-to-drain direction and the gate-to-gate direction are in the plane of the substrate surface.

[0009] Another example of the multiple-gate transistor is the triple-gate transistor. A cross-sectional view of a triple-gate transistor structure is provided in Figure 2b. The plan view of the triple-gate structure is shown in Figure 1. The triple-gate transistor structure has a gate electrode 16 that forms three gates: one gate on the top surface 26 of the silicon body/fin 12, and two gates on the sidewalls 18 of the silicon body/fin 12. The triple-gate transistor achieves better gate control than the double-gate transistor because of it has one more gate on the top of the silicon fin.

[0010] The triple-gate transistor structure may be modified for improved gate control, as illustrated in Figure 2c. Such a structure is also known as the Omega (Ω) field-effect transistor (FET), or simply omega-FET, since the gate electrode 16 has an omega-shape in its cross-sectional view. The encroachment of the gate electrode 16 under the semiconductor fin or body 12 forms an omega-shaped gate structure. It closely resembles the Gate-All-Around (GAA) transistor for excellent scalability, and uses a very manufacturable process similar to that of the double-gate or triple-gate transistor.

[0011] The omega-FET has a top gate (adjacent surface 26), two sidewall gates (adjacent surfaces 18), and special gate extensions or encroachments 28 under the fin-like semiconductor body 12. The omega-FET is therefore a field effect transistor with a gate that almost wraps around the body. In fact, the longer the gate extension, i.e., the greater the extent of the

encroachment E, the more the structure approaches or resembles the gate-all-around structure. The encroachment of the gate electrode 16 under the silicon body helps to shield the channel from electric field lines from the drain and improves gate-to-channel controllability, thus alleviating the drain-induced barrier lowering effect and improving short-channel performance.

SUMMARY OF THE INVENTION

[0012] The preferred embodiment of the present invention provides a multiple-gate transistor that is formed on a bulk substrate. Bulk silicon substrates are cheaper than silicon-on-insulator substrates. Therefore, the availability of a technology that forms multiple-gate transistors on bulk substrates will enable future device scaling at a significantly reduced cost.

[0013] In accordance with a preferred embodiment of the preferred embodiment, a structure and method for the fabrication of multiple-gate transistors on bulk substrates includes depletion-mode bulk multiple-gate transistors and accumulation mode bulk multiple-gate transistors, bulk double-gate transistor, bulk triple-gate transistor, and bulk omega-gate transistor and multiple-gate transistors formed on bulk substrates may be integrated with conventional bulk transistors.

[0014] Prior art multiple-gate transistors such as the double-gate transistor, the triple-gate transistor, and the omega-FET are formed on silicon-on-insulator substrates. This patent teaches a structure and method for forming multiple-gate transistors on bulk substrate. Many of the multiple-gate transistors taught here achieve low cost of manufacture and enable scalability of bulk transistors to significantly reduced feature sizes.

[0015] In one aspect, the present invention teaches a multiple-gate transistor that includes a semiconductor fin formed in a portion of a bulk semiconductor substrate. A gate dielectric overlies a portion of the semiconductor fin and a gate electrode overlies the gate dielectric. A source region and a drain region are formed in the semiconductor fin oppositely adjacent to the gate electrode. In the preferred embodiment, the bottom surface of the gate electrode is lower than either the source-substrate junction or the drain-substrate junction.

[0016] In one method of forming a multiple-gate transistor according to a preferred embodiment, a bulk semiconductor substrate is provided. A semiconductor fin is formed on the bulk semiconductor substrate and isolation regions are provided on sides of the semiconductor fin. A gate dielectric and a gate electrode are formed on a portion of the semiconductor fin. A source region and a drain region are formed in the semiconductor fin. Once again, in the preferred embodiment the source-substrate junction or drain-substrate junction is higher than the bottom surface of the gate electrode.

[0017] In another embodiment of the present invention, portions of a silicon substrate are etched to form at least one semiconductor fin. A gate dielectric layer is formed over the semiconductor fin and a gate electrode layer is formed over the gate dielectric layer. Portions of the gate electrode layer are etched to form a gate electrode so that the gate electrode overlies sidewalls and a top surface of the semiconductor fin. A region of material, e.g., dielectric, is formed adjacent portions of the semiconductor fin not underlying the gate electrode such that a sidewall of the semiconductor fin extends above an upper surface of the region of material. The sidewall of the semiconductor fin above the region of material can then be doped.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0019] Figure 1 is a plan view illustrating the multiple-gate transistor of the present invention;

[0020] Figure 2a is a cross-sectional view of the double-gate transistor of the present invention;

[0021] Figure 2b is a cross-sectional view of the triple-gate transistor of the present invention;

[0022] Figure 2c is a modified structure of the triple-gate transistor shown in Figure 2b;

[0023] Figure 3 is a three-dimensional view of a triple-gate transistor embodiment of the present invention;

[0024] Figures 4a – 4c provide cross-sectional views of the triple-gate transistor of Figure 3;

[0025] Figures 5a – 5e and 6a – 6e illustrate the fabrication of a triple-gate transistor of the present invention;

[0026] Figure 7 is a perspective view of another embodiment triple-gate transistor of the present invention;

[0027] Figure 8 is a perspective view of a double-gate transistor of the present invention; and

[0028] Figure 9 is a perspective view of an omega-gate transistor of the present invention.

DETAILED DESCRIPTION OF illustrative embodiments

[0029] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention; and do not limit the scope of the invention.

[0030] The preferred embodiment relates to the field of semiconductor devices and more particularly to semiconductor devices with multiple gates. Aspects of this invention provide a structure and method for forming multiple-gate transistors on bulk silicon substrates.

[0031] Figure 3 shows a three-dimensional perspective of a triple-gate transistor 130 formed on a bulk substrate 132 according to a first embodiment of this invention. The substrate 132 material can be any semiconductor material. For example, the substrate 132 can be an elemental semiconductor such as silicon or germanium, an alloy semiconductor such as silicon-germanium, or a compound semiconductor such as gallium arsenide. In the preferred embodiment, the substrate 132 comprises monocrystalline silicon.

[0032] The bulk triple-gate transistor 130 includes a semiconductor fin 134 formed on the bulk substrate 132. Isolation regions 136 are formed between semiconductor fins (one fin 134 as shown), or between a semiconductor fin 134 and another active region (not shown). The isolation region 136 may comprise silicon oxide, silicon oxynitride, silicon nitride, or combinations thereof. Mesa isolation can also be used.

[0033] The semiconductor fin 134 includes a doped source region 138 and a doped drain region 140. The source and drain regions 138 and 140 sandwich a channel region 142. A gate

dielectric 144 overlies the channel portion 142 of the semiconductor fin 134, as shown in Figure 3. In fact, the gate dielectric 144 insulates the semiconductor fin 134 from the gate electrode 146.

[0034] The gate electrode 146 straddles across fin-like active region 134. The sidewall surfaces 148 of the semiconductor fin 134 are used for current conduction. In the preferred embodiment, a significant amount of source-to-drain current in the transistor is carried along the sidewall surfaces 148. The semiconductor fin 134 has a predetermined fin width w_f and a drain that has a depth w_d from the top surface of the semiconductor fin. Essentially, the effective device width of the transistor is a function of w_d and w_f. A larger w_d or w_f would result in a larger amount of drive current.

[0035] Cross-sectional views of the triple-gate transistor of Figure 3 in the planes of 4a-4a', 4b-4b', and 4c-4c' are illustrated in Figures 4a, 4b, and 4c, respectively. Figure 4a shows a cross-sectional view in the plane that cuts through the gate electrode 146, the gate dielectric 144, and the channel region 142 of semiconductor fin 134. The gate electrode 146 has a bottom surface 150 that touches the isolation region 136.

[0036] A cross-sectional view in the plane of 4b-4b', which is parallel to plane 4a-4a', is shown in Figure 4b. The view cuts through the drain region 140 of the transistor 130. One feature of the design is that the bottom surface 150 of the gate electrode 146 is below the level of the drain-substrate junction 152 or the level of the source-substrate junction 154.

[0037] Referring now to Figures 4a and 4b, the drain-substrate junction 152 depicted in Figure 4b is at a level that is higher than the level of the bottom surface 150 of the gate electrode 146 depicted in Figure 4a. The difference d in the heights of the drain-substrate junction 152 and

the bottom surface 150 of the gate electrode 146 may be in the range of about 50 angstroms to about 500 angstroms, and preferably about 200 angstroms.

[0038] Figure 4c shows a cross-sectional view in the plane that cuts through the gate electrode 146, the gate dielectric 144, the channel region 142, the source region 138, and the drain region 140. Figure 4c also shows a potential leakage current path 156 between the source and the drain regions 138 and 140. The gate electrode 146 above or below the plane of the page (i.e., plane 4c-4c') is drawn in dashed lines in Figure 4c, showing that the gate electrode 146 is in the vicinity of the potential leakage current path. Therefore, by having the gate electrode 146 extend below the source-substrate junction 154 or the drain-substrate junction 152, and positioning the gate electrode 146 in the vicinity of the potential leakage path 156, this embodiment ensures that the gate electrode 146 exerts considerable influence on the potential leakage path 156 to suppress the leakage.

[0039] In various aspects of this invention, the source and drain regions 138 and 140 may be doped n-type, and the body region 142 may be doped p-type to form an n-channel depletion-mode transistor, or the source and drain regions 138 and 140 may be doped p-type, and the body region 142 doped n-type to form a p-channel depletion-mode transistor. Alternatively, accumulation mode transistors may be formed by having the body regions 142 doped the same type as the source and drain regions 138 and 140. For example, the source 138, drain 140, and body 142 may all be doped n-type to form an n-channel accumulation mode transistor.

[0040] A method of forming the multiple-gate transistor of Figure 3 will now be described with reference to Figures 5a-5e (collectively Figure 5) and Figures 6a-6e (collectively Figure 6). Figures 5 and 6 show the device cross-section in two parallel planes at the various stages of device fabrication. In particular, Figure 5 shows the device 130 in the plane 4a-4a' of Figure 3

and Figure 6 shows the device 130 in the plane 4b-4b' of Figure 3. As before, the planes 4a-4a' and 4b-4b' are parallel to each other. A perspective view of a transistor after additional steps are performed is shown in Figure 7.

[0041] The starting material is a semiconductor substrate 132 that may be an elemental semiconductor, an alloy semiconductor, or a compound semiconductor. The starting material is preferably a silicon substrate, preferably about 300 mm in diameter. At least one semiconductor fin 134 is formed by patterning the semiconductor substrate, as shown in Figures 5a and 6a. The semiconductor fin patterning process may be accomplished by forming a mask (not shown) over the semiconductor 132, followed by the etching of the semiconductor 132 to a predetermined depth d_t. The mask may comprise a commonly used mask material such as photoresist or silicon oxide or silicon nitride, combinations thereof. The trench depth d_t may be in the range of about 200 angstroms to about 6000 angstroms, preferably about 3000 angstroms.

[0042] The trench depth d_t may be the same for all semiconductor fins 134 formed in substrate 132. Alternatively, trenches of different depths can be formed on the same bulk semiconductor substrate 132. This embodiment allows for transistors with different drive currents to be formed on the same chip. This embodiment can be realized by selectively removing portions of the trench mask (not shown) during the etching process so that some trenches are etched for longer.

[0043] The mask may or may not be removed after the etching step. If it is removed, as in the preferred embodiment, a triple-gate transistor will be formed. If it is not removed, a double-gate transistor, as illustrated in Figure 8, can be formed.

[0044] Referring now to Figures 5b and 6b, isolation regions 136 with a depth of d_i are formed in the trench 160. The isolation depth d_i may be in the range of about 20 angstroms to

about 6000 angstroms, preferably about 200 angstroms. In the preferred embodiment, the ratio of d_r:d_f ranges from about 1.2:1 to about 6:1, preferably about 2:1. The semiconductor fin has sidewall surfaces 158 as shown.

[0045] A gate dielectric layer 144 is then formed on the semiconductor fin 134. Due to subsequent processing, the gate dielectric 144 is shown in Figure 5c but not in Figure 6c. The gate dielectric may be formed by thermal oxidation, chemical vapor deposition, sputtering, or any other methods known and used in the art for forming a gate dielectric. Depending on the technique of gate dielectric formation, the gate dielectric 144 thickness on the top of the fin 134 may be different from the gate dielectric thickness on the fin sidewall. In one embodiment, the gate dielectric thickness on the top surface of the fin is less than about 20 angstroms.

[0046] The gate dielectric may be formed from a material such as silicon dioxide or silicon oxynitride with a thickness ranging from about 3 angstroms to about 100 angstroms, preferably about 10 angstroms or less. The gate dielectric may also formed from a high permittivity (high-k) material such as lanthanum oxide (La_2O_3), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), hafnium oxynitride (HfON), or zirconium oxide (ZrO_2), or combinations thereof, with an equivalent oxide thickness of about 3 angstroms to about 100 angstroms.

[0047] Next, the gate electrode 146 material is deposited. The gate electrode material is a conductive material and may be amorphous or polycrystalline silicon (poly-Si), poly-crystalline silicon-germanium (poly-SiGe), a metallic nitride, a metallic silicide, a metallic oxide, or a metal. Examples of metallic nitrides include tungsten nitride, molybdenum nitride, titanium nitride, and tantalum nitride, or their combinations. Examples of metallic silicide include tungsten silicide, titanium silicide, cobalt silicide, nickel silicide, platinum silicide, erbium silicide, or their combinations. Examples of metallic oxides include ruthenium oxide, indium tin

oxide, or their combinations. Examples of metal include tungsten, titanium, aluminum, copper, molybdenum, nickel, platinum, and others.

[0048] The gate electrode 146 material may be deposited by chemical vapor deposition (CVD), by sputter deposition, or by other techniques known and used in the art for depositing conductive materials. The thickness of the gate electrode material may be in the range of about 200 angstroms to about 4000 angstroms, preferably about 1500 angstroms. The top surface of the gate electrode 146 material usually has a non-planar top surface, and may be planarized (e.g., chemical-mechanical polished) prior to patterning of the gate electrode 146 material or gate etch. Ions may or may not be introduced into the gate electrode 146 material at this point. Ions may be introduced, for example, by ion implantation techniques.

[0049] The next step is the definition of the gate electrode 146. A mask material (not shown) is formed on the gate electrode material, and the gate electrode 146 is formed by an etching process, preferably an anisotropic etch (e.g., dry plasma etching process), to give the cross-sections in Figure 5c and 6c. In this example, gate dielectric 144 has also been patterned, although this step is not necessary.

[0050] A dielectric layer 162 is then formed to cover a portion of the sidewall surface 158 of the semiconductor fin 134, not already covered by isolation region 136. Referring now to Figures 5d and 6d, the layer 162 is formed such that a sidewall 158 semiconductor fin 134 extends above the upper surface of layer 162. This dielectric layer 162 allows the formation of the source and drain regions 138 and 140 such that the drain-substrate junction 152 or the source-substrate junction 154 is at a higher level than the bottom surface 150 of the gate electrode 146. In the preferred embodiment, the drain-substrate junction 152 or the source-substrate junction 154 is defined to be the position where the doping concentration in the source or drain region

138 is at the 10^{18} cm^{-3} level. In the preferred embodiment, dielectric layer 162 comprises silicon oxide.

[0051] In the preferred embodiment, the material region 162 is formed to a thickness between about 50 angstroms and about 500 angstroms, preferably about 200 angstroms. The height of the exposed portion of sidewall 158 is typically in the range of about 500 angstroms to about 2000 angstroms, preferably about 1000 angstroms. As a result, the ratio of the thickness of the material region 162 to the height of the exposed portion of the sidewall 158 is preferably between about 1:1 to about 1:20

[0052] The source and drain regions 138 and 140 are formed next as shown in Figures 5e and 6e. The formation of the source and drain regions 138 and 140 may involve several steps. In the preferred embodiment, an ion implantation process is first performed to dope the source and drain regions 138 and 140 immediately adjacent to the channel region 142. The channel region 142 is the portion of the semiconductor fin 134 wrapped around by the gate dielectric 144 and the gate electrode 146.

[0053] Spacers (164 in Figure 7) are then formed on the sidewalls of the gate electrode 146. The spacers 164 may be formed by deposition of a spacer material(s) followed by anisotropic etching of the spacer material(s) to form the spacers 164. The spacer is formed from a dielectric material, preferably silicon nitride (e.g., Si_3N_4). The spacer material may also be formed from a stack of dielectric materials, such as a silicon nitride layer overlying a silicon oxide layer. Figure 7 shows a three-dimensional perspective of the transistor structure with spacers 164 and the dielectric layer 162.

[0054] A selective epitaxy may additionally be performed to increase the width and/or height of the fin 134 in the source and drain regions 138 and 140. The selective epitaxy results

in epitaxial growth in the source and drain regions 138 and 140, and perhaps the gate electrode region 146. The epitaxy can be performed uniformly for all fins 134 on a single substrate 132 or can be performed to different levels (including none) for different fins on a single substrate.

[0055] An optional ion implantation is then performed to dope the source and drain regions 138 and 140. The ion implantation process is performed if the selective epitaxy does not incorporate dopants into the grown regions during epitaxial growth. Conductive materials (not shown) such as silicides may be formed on the source and drain regions (138 and 140) to increase the conductance in these regions.

[0056] Figure 8 shows a structure for a double gate transistor. This device is similar to the triple gate device of Figure 7 but also includes an etch mask 166, as was discussed above. In the preferred embodiment, the etch mask 166 is formed of silicon oxynitride and has a thickness between about 20 angstroms and about 500 angstroms.

[0057] A transistor with an omega-shaped gate electrode, as shown in Figure 9, can also be formed by slightly modifying the fabrication process just described. For example, during the definition of the semiconductor fin in Figures 5a and 6a, a two-step etch may be employed. A first etch step may employ a highly anisotropic plasma etch process with a negligible lateral etch rate. A second etch step may employ a less anisotropic etch so that some lateral etch takes place, resulting in a narrower semiconductor fin at the base. The two-step etch will result in a semiconductor fin with a wider fin width at the top, e.g., source 138 and drain 140, and a narrower fin width at the bottom 168. The remaining fabrication steps follow those as described above. The resulting transistor structure is shown in Figure 9.

[0058] The following references are related to aspects of the preferred embodiment and are hereby incorporated herein by reference:

[1] C. Hu *et al.*, University of California, FinFET transistor structures having a double gate channel extending vertically from a substrate and methods of manufacture, U.S. Patent No. 6,413,802.

[2] K. P. L. Muller *et al.*, International Business Machines Corporation, June 26 2001, Planarized Si fin device, U.S. Patent No. 6,252,284.

[3] K. P. L. Muller *et al.*, International Business Machines Corporation, Aug. 13 2002, Process for making planarized silicon fin device, U.S. Patent No. 6,432,829.

[4] B. Yu, Advanced Micro Devices, Inc., May 21 2002, Double-gate transistor formed in a thermal process, U.S. Patent No. 6,391,695.

[5] B. Yu, Advanced Micro Devices, Inc., May 21 2002, Process for forming multiple active lines and gate-all-around MOSFET, U.S. Patent No. 6,391,782.

[6] B. Yu *et al.*, Advanced Micro Devices, Inc., Sep. 17 2002, CMOS inverter configured from double gate MOSFET and method of fabricating same, U.S. Patent No. 6,451,656.

[7] M. Ieong *et al.*, International Business Machines Corporation, Dec. 10, 2002, Variable threshold voltage double gated transistors and method of fabrication, U.S. Patent No. 6,492,212.

[8] X. Huang *et al.*, "Sub-50 nm p-channel finFET," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 880-886, May 2001.

[9] F.-L. Yang *et al.*, "35 nm CMOS FinFETs," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 109-110, June 2002.

[10] H.-S. P. Wong, "Beyond the conventional transistor," *IBM J. Research and Development*, vol. 46, no. 2/3, pp. 133-168, March/May 2002.

[11] R. Chau *et al.*, "Advanced depleted-substrate transistors: single-gate, double-gate, and tri-gate", 2002 International Conference on Solid State Devices and Materials, Nagoya, Japan, pp. 68-69, Sep. 2002.

[12] F.-L. Yang *et al.*, "25 nm CMOS Omega-FETs," *International Electron Device Meeting*, Dig. Technical Papers, Dec. 2002.

[13] J. P. Colinge *et al.*, "Silicon-on-insulator gate-all-around device," *International Electron Device Meeting*, Dig. Technical Papers, pp. 595-598, Dec. 1990.

[14] E. Leobandung *et al.*, "Wire-channel and wrap-around-gate metal-oxide-semiconductor field-effect transistors with a significant reduction of short channel effects," *J. Vacuum Science and Technology B*, vol. 15, no. 6, pp. 2791-2794, 1997.

[0059] While several embodiments of the invention, together with modifications thereof, have been described in detail herein and illustrated in the accompanying drawings, it will be evident that various modifications are possible without departing from the scope of the preferred embodiment. The examples given are intended to be illustrative rather than exclusive. The drawings may not necessarily be to scale and features may be shown in a schematic form.

WHAT IS CLAIMED IS:

1. A multiple-gate transistor comprising:

a semiconductor fin formed in a portion of a bulk semiconductor substrate;

a gate dielectric overlying a portion of the semiconductor fin;

a gate electrode overlying the gate dielectric, the gate electrode having a bottom surface; and

a source region and a drain region formed in the semiconductor fin oppositely adjacent to the gate electrode, the source region having a source-substrate junction, and the drain region having a drain-substrate junction;

wherein the bottom surface of the gate electrode is lower than the source-substrate junction or the drain-substrate junction.

2. The structure of claim 1 wherein the gate electrode comprises polycrystalline or amorphous silicon.

3. The structure of claim 1 and further comprising a silicide region formed over the gate electrode.

4. The structure of claim 1 wherein the gate electrode is formed from a polycrystalline semiconductor.

5. The structure of claim 1 wherein the gate electrode is formed from a metallic nitride.

6. The structure of claim 1 wherein the gate electrode is formed from a metallic silicide.

7. The structure of claim 1 wherein the gate electrode is formed from a metal.

8. The structure of claim 1 wherein the gate electrode has a substantially planar top surface.

9. The structure of claim 1 and further comprising spacers on sides of the gate electrode.

10. The structure of claim 1 wherein the semiconductor fin comprises silicon.

11. The structure of claim 1 wherein the semiconductor fin comprises silicon and germanium.

12. The structure of claim 1 wherein the semiconductor structure further comprises an etchant mask overlying the semiconductor fin.

13. The structure of claim 1 wherein the semiconductor fin has a fin width that is larger at the top of the semiconductor fin than at the bottom of the semiconductor fin.

14. The structure of claim 1 wherein the gate dielectric comprises silicon oxide.

15. The structure of claim 1 wherein the gate dielectric comprises silicon oxynitride.

16. The structure of claim 1 wherein the gate dielectric comprises a high permittivity material.

17. The structure of claim 1 wherein the gate dielectric comprises a material selected from the group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, and zirconium oxide, and combinations thereof.

18. The structure of claim 1 wherein the gate dielectric comprises a material with a relative permittivity greater than about 5.

19. The structure of claim 1 wherein the gate dielectric has a thickness of between about 3 and about 100 angstroms.

20. The structure of claim 1 wherein the multiple-gate transistor is a triple-gate transistor.

21. The structure of claim 1 wherein the multiple-gate transistor is a double-gate transistor.

22. The structure of claim 1 wherein the multiple-gate transistor is an omega-gate transistor.

23. The structure of claim 1 wherein the bottom surface of the gate electrode is lower than the source-substrate junction and the drain-substrate junction by at least about 50 angstroms.

24. A method of forming a multiple-gate transistor, the method comprising:

providing a bulk semiconductor substrate;

forming a semiconductor fin in the bulk semiconductor substrate;

forming isolation regions on sides of the semiconductor fin;

forming a gate dielectric and a gate electrode on a portion of the semiconductor fin, the gate electrode having a bottom surface; and

forming a source region and a drain region in the semiconductor fin, the source region having a source-substrate junction and the drain region having a drain-substrate junction, the source-substrate junction or drain-substrate junction being higher than the bottom surface of the gate electrode.

25. The method of claim 24 wherein the source-substrate junction and the drain-substrate junction is higher than the bottom surface of the gate electrode by at least 50 angstroms.

26. The method of claim 24 wherein forming a semiconductor fin comprises:

forming a mask over the bulk semiconductor substrate; and

etching exposed regions of the semiconductor substrate to form the semiconductor fin.

27. The method of claim 26 further comprising removing the mask.

28. The method of claim 27 wherein the mask comprises a photoresist.

29. The method of claim 27 wherein the mask comprises a material selected from the group consisting of silicon oxide, silicon oxynitride, silicon nitride, and combinations thereof.

30. The method of claim 24 and further comprising strapping the source and drain regions with a conductive material.

31. The method of claim 24 and further comprising forming spacers on sides of the gate electrode.

32. The method of claim 24 and further comprising performing selective epitaxy on the source and drain regions.

33. The method of claim 24 wherein the semiconductor fin comprises silicon.

34. The method of claim 24 wherein the semiconductor fin comprises silicon and germanium.

35. The method of claim 24 wherein the gate dielectric comprises silicon oxide or silicon oxynitride or silicon nitride.

36. The method of claim 24 wherein the gate dielectric comprises a high permittivity material.

37. The method of claim 24 wherein the gate dielectric comprises a material selected from the group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, and zirconium oxide, and combinations thereof.

38. The method of claim 24 wherein the gate dielectric comprises a material with a relative permittivity greater than about 5.

39. The method of claim 24 wherein the gate dielectric has a thickness of between about 3 and about 100 angstroms.

40. The method of claim 24 wherein the gate electrode comprises polycrystalline or amorphous silicon.

41. The method of claim 24 wherein the gate electrode comprises poly-SiGe.

42. The method of claim 24 wherein the gate electrode comprises a metallic nitride.

43. The method of claim 24 wherein the gate electrode comprises a metallic silicide.

44. The method of claim 24 wherein the gate electrode comprises a metal.

45. The method of claim 24 wherein the multiple-gate transistor is a triple-gate transistor.

46. The method of claim 24 wherein the multiple-gate transistor is a double-gate transistor.

47. The method of claim 24 wherein the multiple-gate transistor is an omega-gate transistor.

48. A method of forming a semiconductor device, the method comprising:

providing a silicon substrate;

etching portions of the silicon substrate to form at least one semiconductor fin;

forming a gate dielectric layer over the semiconductor fin;

forming a gate electrode layer over the gate dielectric layer;

etching portions of the gate electrode layer to form a gate electrode, the gate electrode overlying sidewalls and a top surface of the semiconductor fin;

forming a region of material adjacent portions of the semiconductor fin not underlying the gate electrode such that a sidewall of the semiconductor fin extends above an upper surface of the region of material; and

doping the sidewall of the semiconductor fin above the region of material.

49. The method of claim 48 wherein forming an isolation region comprises depositing an oxide material.

50. The method of claim 48 and further comprising forming a masking material over the silicon substrate and wherein the step of etching portions of the silicon substrate is performed in alignment with the masking material.

51. The method of claim 50 and further comprising removing the masking material after the semiconductor fin is formed.

52. The method of claim 50 wherein the gate dielectric layer and the gate electrode layer are formed over the masking material.

53. The method of claim 48 wherein forming a region of material comprises depositing a dielectric layer.

54. The method of claim 48 wherein forming a gate dielectric layer comprises forming a layer of a material with a relative permittivity greater than about 5.

55. The method of claim 48 and further comprising forming an isolation region adjacent the semiconductor fin.

56. The method of claim 48 and further comprising removing the region of material after doping the sidewall.