CLAIMS

[Claim 1]

A lead frame, comprising:

a plurality of lead portions, wherein

at least a part of an upper surface of the lead portion and a sidewall surface of the lead portion is a rough surface having been subjected to roughening treatment, and

a value of a* in a CIELab color space of the rough surface is within a range from 12 to 19, and a value of b* is within a range from 12 to 17.

[Claim 2]

A lead frame, comprising:

a plurality of lead portions, wherein

at least a part of an upper surface of the lead portion and a sidewall surface of the lead portion is a rough surface having been subjected to roughening treatment, and

an arithmetic mean peak curvature Spc of peaks of the rough surface is 700 mm^{-1} or greater.

[Claim 3]

The lead frame according to claim 2, wherein

an arithmetic mean height Sa of the rough surface is 0.12 μm or greater.

[Claim 4]

The lead frame according to claim 1 or 2, wherein

a part of the upper surface of the lead portion and the sidewall surface of the lead portion is the rough surface, and

a metal plating layer is provided on, of the upper surface of the lead portion, a part that is not the rough surface.

[Claim 5]

The lead frame according to claim 4, wherein

the metal plating layer includes at least one of an Ag plating layer, an Ni plating layer, a Pd plating layer, or an Au plating layer.

[Claim 6]

The lead frame according to claim 1 or 2, wherein

the lead portion includes an inner lead portion thinned from a lower surface side of the lead portion, and

a lower surface of the inner lead portion is the rough surface.

[Claim 7]

The lead frame according to claim 1 or 2, further comprising:

a die pad portion on which a semiconductor element is mountable, wherein

the plurality of lead portions is disposed around the die pad portion, and

an upper surface of the die pad portion and a sidewall surface of the die pad portion is the rough surface.

[Claim 8]

The lead frame according to claim 1 or 2 to be used for manufacturing a semiconductor device that includes a molding portion that seals at least the plurality of lead portions, wherein

an upper surface of the lead portion in contact with the molding portion and a sidewall surface of the lead portion in contact with the molding portion is a rough surface having been subjected to roughening treatment.

[Claim 9]

A method of manufacturing a lead frame, comprising:

a metal substrate preparation step of preparing a metal substrate that has a first surface and a second surface that is an opposite of the first surface;

a metal substrate processing step of forming a plurality of lead portions by processing the metal substrate; and

a rough surface forming step of forming a rough surface by roughening at least a part of an upper surface of the lead portion and a sidewall surface of the lead portion, wherein

in the rough surface forming step, the roughening is performed such that a value of a* in a CIELab color space of the rough surface is within a range from 12 to 19, and a value of b* is within a range from 12 to 17.

[Claim 10]

A method of manufacturing a lead frame, comprising:

a metal substrate preparation step of preparing a metal substrate that has a first surface and a second surface that is an opposite of the first surface;

a metal substrate processing step of forming a plurality of lead portions by processing the metal substrate; and

a rough surface forming step of forming a rough surface by roughening at least a part of an upper surface of the lead portion and a sidewall surface of the lead portion, wherein

in the rough surface forming step, the roughening is performed such that an arithmetic mean peak curvature Spc of peaks of the rough surface is 700 mm^{-1} or greater.

[Claim 11]

The method of manufacturing the lead frame according to claim 10,

wherein

in the rough surface forming step, the roughening is performed such that an arithmetic mean

height Sa of the rough surface is 0.12 μm or greater.

[Claim 12]

The method of manufacturing the lead frame according to claim 9 or10,

wherein

alkaline treatment is applied to the lead portion after the rough surface forming step.

[Claim 13]

The method of manufacturing the lead frame according to claim 9 or10,

wherein

a metal plating layer is provided on a part of the upper surface of the lead portion, and,

in the rough surface forming step, a part of the upper surface of the lead portion where the metal plating layer is not provided and the sidewall surface thereof are roughened.

[Claim 14]

The method of manufacturing the lead frame according to claim 13,

wherein

the metal plating layer includes at least one of an Ag plating layer, an Ni plating layer, a Pd plating layer, or an Au

plating layer.

[Claim 15]

The method of manufacturing the lead frame according to claim 9 or10,

wherein,

in the metal substrate processing step, the lead portion that includes an inner lead portion thinned from a lower surface side of the lead portion is formed, and, in the rough surface forming step, the rough surface is formed at a lower surface of the inner lead portion.

[Claim 16]

The method of manufacturing the lead frame according to claim 9 or10,

wherein,

in the metal substrate processing step, a die pad portion on which a semiconductor element is mountable is formed such that the plurality of lead portions is disposed around the die pad portion, and

in the rough surface forming step, the rough surface is formed by roughening an upper surface of the

die pad portion and a sidewall surface of the die pad portion and at least a part of an upper surface of the lead portion and a sidewall surface of the lead portion.

[Claim 17]

A lead frame, comprising:a die pad on which a semiconductor element is mountable;and a lead portion located around the die pad, wherein

a first rough surface is formed at, at least, a part of a front surface of the die pad,

a second rough surface is formed at, at least, a part of a front surface of the lead portion,

the second rough surface of the lead portion is rougher than the first rough surface of the die pad, and

the front surface of the die pad and the front surface of the lead portion are surfaces located on sides on which the semiconductor element is mountable, respectively.

[Claim 18]

The lead frame according to claim 17, wherein

a third rough surface is formed at a side surface of the die pad, and

the third rough surface of the die pad is rougher than the first rough surface of the die pad.

[Claim 19]

The lead frame according to claim 17, wherein

the lead portion includes an inner lead thinned from a back surface side, an inner lead back surface is formed at a back surface side of the inner lead, a fourth rough surface is formed at the inner lead back surface, and

the fourth rough surface of the lead portion is rougher than the first rough surface of the die pad.

[Claim 20]

The lead frame according to claim 17, wherein

the lead portion includes an inner lead thinned from a back surface side, an inner lead tip surface is formed at, of the inner lead, a surface oriented

toward the die pad,

a fifth rough surface is formed at the inner lead tip surface, and

the fifth rough surface of the lead portion is rougher than the first rough surface of the die pad.

[Claim 21]

The lead frame according to claim 17, wherein

an area of a smooth surface is formed in the front surface of the leadportion.

[Claim 22]

The lead frame according to claim 21, wherein

a metal layer is formed on the area of the smooth surface.

[Claim 23]

The lead frame according to claim 21, wherein the area of the

smooth surface is exposed to outside.

[Claim 24]

The lead frame according to claim 17, wherein

an S ratio of the first rough surface is 1.10 or higher but lower than 1.30, and an S ratio of the second rough surface is 1.30 or higher and 2.30 or lower.

[Claim 25]

A method of manufacturing a lead frame, comprising:

a step of preparing a metal substrate;

a step of forming a die pad on which a semiconductor element is mountable and a lead portion located around the die pad by etching the metal substrate;

a step of forming a coating layer on the die pad and the lead portion;

a step of removing the coating layer existing on at least a part of a front surface of the die pad;

a step of forming a first rough surface at, of the die pad, a part that is not covered by the coating

layer;

a step of removing the coating layer existing on at least a part of a front surface of the lead portion; and

a step of forming a second rough surface at, of the lead portion, a part that is not covered by the coating layer, wherein

the second rough surface of the lead portion is rougher than the first rough surface of the die pad, and

the front surface of the die pad and the front surface of the lead portion are surfaces located on sides on which the semiconductor element is mountable, respectively.