

METHOD AND APPARATUS UTILIZING DIRECT DIGITAL SYNTHESIZER AND SPREAD SPECTRUM TECHNIQUES FOR REDUCING EMI IN DIGITAL DISPLAY DEVICES

5

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The invention relates to liquid crystal displays (LCDs). More specifically, the
10 invention describes a method and apparatus for reducing electromagnetic interference
in a liquid crystal display.

2. DISCUSSION OF RELATED ART

Electromagnetic interference (EMI) is a measure of the amount of interference
15 that an electronic device (the unintentional transmitter) disturbs an intentional
receiver. Not surprisingly, EMI is a major concern in design of devices, such as PCs,
flat panel monitors, etc, that rely on high speed components, because it determines
whether a system, PC motherboard, graphics controller, etc gets approved for sale by
the US Department of Commerce. This situation is especially true in designs that
20 feature high speed (e.g., Pentium-class) processors, high-speed buses, and several
clock outputs. Typically, EMI testing occurs late in the design process, so failing the
test can mean expensive redesign and increased time to market. In addition to
material costs, using shielding as a way to reduce EMI significantly increases
production complications, further driving up system cost.

25 There are, however, various techniques to reduce and/or eliminate EMI. One
such technique is referred to as pulse shaping which requires control of the output

waveshape in order to control higher frequency harmonics. However, pulse shaping does not control the spectral energy of the fundamental but only changes the shape of the rising edge by rounding off the corners and reducing some of the higher frequency components and their energy. Therefore, pulse shaping works if one can control the
5 portion of the waveform near the switching threshold.

An additional problem with pulse shaping is that the balancing act between too much rounding and not enough rounding to achieve the desired EMI reduction is made even more complex since temperature and voltage variations disrupt the balance. This balancing act is further complicated by the fact that techniques used for
10 optimum rounding may not give consistent results from run to run in manufacturing. For example, carefully set capacitive or resistive shaping values change from production lot to production lot requiring overdesign of the system to ensure that process variations leave sufficient EMI control and rise time.

Yet another approach to reducing EMI referred to as slew-rate control
15 manages the rising-edge slope by maintaining an output drive that doesn't overcharge load capacitance. Slew-rate control achieves this maintenance by creating a current-controlled output that avoids having a fast, high current and should theoretically be effective. However, as with pulse shaping, a major issue is maintaining control on a manufacturing lot-to-lot basis and across various voltage and temperature ranges.
20 The design must account for the worst-case process and for both high and low temperatures and voltages. These potential variations are both critical and unpredictable. As a result, slew-rate control is difficult to implement and unreliable.

Finally, the most popular approach to reducing EMI, referred to as spread spectrum technology (SST), spreads the energy of a fundamental frequency to

minimize any peaking of energy at specific frequencies. This technique reduces both the fundamental-frequency EMI and the higher frequency harmonic components, significantly reducing overall system EMI radiation without compromising clock-edge rise and fall times (see Figs. 1A-1B). With lower spectrum-peak amplitudes, a system meets and has more margin for EMI. Spread spectrum is the simplest, most efficient technique and offers the most immunity to manufacturing-process variations. Accordingly, the use of SST has pervaded the motherboard market to the point where it is being used in virtually all designs using chipsets that support a 100 MHz front side bus (FSB) as well as for PCI, CPU, and memory buses. All motherboard chipset vendors are designing their parts to work with spread-spectrum timing signals.

A useful component in the frequency conversion of discrete signals is a direct digital synthesizer (DDS), shown by way of example in FIG. 1C. The DDS usually performs a frequency step-down function. Summation unit 402 adds the n-bit value SF stored in SF register 404 to the n-bit value from the output of phase accumulator 406. The sum is synchronously updated upon each rising edge of SCLK. Phase accumulator 406 feeds the n-bit DDS frequency F_{DDS} to the output module, and feeds back F_{DDS} to summation unit 402, thereby generating, over some number of SCLK cycles, a staircase periodic signal 408 with a frequency given by the formula in Equation (2) below:

$$F_{DDS} = \frac{SF}{2^n} F_{SCLK} \quad (2)$$

where F_{SCLK} is the frequency value of SCLK. Output module 410 converts the DDS frequency signal F_{DDS} to a destination clock DCLK. Output module 410 could, for example, convert the staircase waveform into a binary clock signal with frequency F_{DDS} . It should be noted that the jitter in the period of staircase periodic signal 408 is

equal to the SCLK period. If the SCLK period varies over a wide range (i.e., has high jitter), then it may be difficult (or impossible) to design the output module to reduce the jitter effectively.

Therefore what is desired is an efficient method and apparatus for reducing
5 EMI using spread spectrum technology by providing a selectable frequency modulated clock signal.

SUMMARY OF THE INVENTION

According to the present invention, methods, apparatus, and systems are disclosed for reducing EMI using spread spectrum technology by providing a
10 selectable frequency modulated clock signal are disclosed.

In one embodiment, a clock synthesizer circuit arranged to provide a selectable spread spectrum based output clock signal that includes a phase accumulator circuit, a reference clock source coupled to the phase accumulator circuit arranged to provide a reference clock signal, a frequency shifter unit coupled to the
15 phase accumulator, a nominal phase source coupled to the phase accumulator, coupled to the frequency shifter unit arranged to provide a nominal phase signal, and a modulated phase source coupled to the frequency shifter unit arranged to provide a modulation signal. The frequency shifter unit combines the nominal phase signal and the modulation signal to form a frequency shift signal as input to the phase
20 accumulator which uses the frequency shift signal to sample the reference clock signal so as to produce the output clock signal having a central frequency and a frequency spread based upon the modulation signal.

In another embodiment, a method of providing a selectable spread spectrum based output clock signal is described. The method includes operations for providing
25 a phase accumulator circuit, coupling a reference clock source to the phase

accumulator circuit arranged to provide a reference clock signal, and coupling a
frequency shifter unit to the phase accumulator. The method further includes
coupling a nominal phase source to the phase accumulator coupled to the frequency
shifter unit arranged to provide a nominal phase signal and coupling a modulated
5 phase source to the frequency shifter unit arranged to provide a modulation signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the following
description taken in conjunction with the accompanying drawings.

10

Fig. 1A shows a representative clock signal and associated harmonic based
EMI.

Fig. 1B illustrates a spread spectrum processing of the representative clock
signal of Fig. 1A and a resulting reduction in harmonic EMI levels.

15

Fig. 2 shows a system for providing a selectable modulated system clock in
accordance with an embodiment of the invention.

Fig. 3 shows a representative bipolar signal in accordance with an
embodiment of the invention.

20

Figs. 4A-4C shows representative output signals in accordance with an
embodiment of the invention.

Fig. 5 shows the clock modulator circuit that takes the form of a direct digital
synthesizer circuit (DDS) in a particular embodiment of the invention.

Fig. 6 shows a particular implementation of a phase accumulator circuit in
accordance with an embodiment of the invention.

Fig. 7 shows a flowchart detailing a process for providing a spread spectrum based modified clock in accordance with an embodiment of the invention.

Fig. 8 illustrates a computer system 800 employed to implement the invention.

5 DETAILED DESCRIPTION OF SELECTED EMBODIMENTS

Reference will now be made in detail to a preferred embodiment of the invention. An example of the preferred embodiment is illustrated in the accompanying drawings. While the invention will be described in conjunction with a preferred embodiment, it will be understood that it is not intended to limit the
10 invention to one preferred embodiment. To the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

In one embodiment, a direct digital synthesizer circuit (DDS) arranged to provide a selectable spread spectrum based output clock signal is described. The
15 synthesizer includes a phase accumulator circuit, a reference clock source coupled to the phase accumulator circuit arranged to provide a reference clock signal, a frequency shifter unit coupled to the phase accumulator, a nominal phase source coupled to the phase accumulator coupled to the frequency shifter unit arranged to provide a nominal phase signal, and a modulated phase source coupled to the
20 frequency shifter unit arranged to provide a modulation signal. The frequency shifter unit combines the nominal phase signal and the modulation signal to form a frequency shift signal as input to the phase accumulator that produces the output clock signal having a central frequency and a frequency spread based upon the modulation signal.

The invention will now be described in terms of a spread spectrum system and methods of use thereof capable of being incorporated in an integrated semiconductor device well known to those skilled in the art used to provide a modulated clock signal to an LCD. It should be noted, however, that the described embodiments are for
5 illustrative purposes only and should not be construed as limiting either the scope or intent of the invention.

Accordingly, Fig. 2 shows a spread spectrum system 200 in accordance with an embodiment of the invention. The system 200 includes a DDS circuit 202 arranged to modify a reference clock signal CLK_{ref} received from a reference clock
10 signal source 204 based upon a clock modulation signal CLK_{mod} provided by a clock modulation signal generator 206 and a nominal signal CLK_{nom} provided by a nominal signal generator 208. Each of the clock modulation signal generator 206 and the nominal signal generator 208 is coupled to an adder unit 210 having an output coupled to a phase accumulator 212. It should be noted that the clock modulation
15 signal CLK_{mod} is a periodic bipolar signal (i.e., has symmetric positive and negative-going waveform) having an average value of substantially zero. One such signal is illustrated in Fig. 3 showing both a clock modulation signal waveform 302 and an associated clock modulation signal CLK_{mod} that in this case takes the form of a series of hexadecimal waveform values 304. In this way, even though an output clock
20 CLK_{out} signal is frequency modulated by the variation of the clock modulation signal CLK_{mod} , yet its central frequency remains unchanged.

In the described embodiment, an output circuit 214 included in the clock modulation circuit 202 is used to provide in some cases, an analog modulated clock signal using an digital to analog converter (DAC) 216 coupled to a phase locked loop
25 (PLL) circuit 218 well known to those skilled in the art.

During operation, the adder unit 210 adds the clock modulation signal CLK_{mod} to the nominal signal CLK_{nom} thereby generating a modulated signal 220 provided as input to the phase accumulator 212. The phase accumulator 212 responds by sampling the reference clock signal CLK_{ref} based upon the received modulated signal 220 thereby producing an accumulator output signal 222 shown in Fig. 4A. In accordance with an embodiment of the invention, the accumulator output signal 222 provides a frequency spread Δf around a central reference frequency f_{ref} directly related to the clock modulation signal CLK_{mod} . Figs 4B and 4C illustrate at least one advantage of the invention in that although the output clock CLK_{out} signal is frequency modulated by the clock modulation signal CLK_{mod} , the central frequency f_{ref} remains unchanged.

In one embodiment shown in Fig. 5, the clock modulation circuit 202 takes the form of a direct digital synthesizer circuit (DDS) 500. The generation of the output clock CLK_{out} signal from the reference clock signal CLK_{ref} and the clock modulation signal CLK_{mod} is performed by a phase accumulator circuit 502. In some embodiments, the phase accumulator circuit 502 is coupled to a ROM lookup table of sinusoidal magnitude values 506. In this embodiment, the sampled output of the phase accumulator 502 is then used to address the ROM lookup table of sinusoidal magnitude values 506. It should be noted that in this situation, the conversion of the sampled phase to a sinusoidal magnitude is analogous to the projection of the real or imaginary component in time. Since the number of bits used by the phase accumulator 502 determines the granularity of the frequency adjustment steps of the output clock CLK_{out} signal, a typical phase accumulator size is 24 to 32 bits. Since the use the DDS 500 requires that the nominal value of the output clock CLK_{out} signal

cannot be greater than approximately $\frac{1}{2}$ of the reference clock signal CLK_{ref} , the output clock CLK_{out} signal depends upon the phase locked loop (PLL) circuit 218.

In one implementation shown in Fig. 6, during operation, the phase accumulator circuit 502 is loaded synchronous to the reference clock signal CLK_{ref} with an N bit frequency word F (where N is typically 24) based upon the clock modulation signal CLK_{mod} . This frequency word F is continuously accumulated with the last sampled phase value by an N bit adder 602. The output of the adder 602 is sampled at the reference clock signal CLK_{ref} coupled to the N bit adder 602. When the accumulator circuit 502 reaches the N bit maximum value (modified by the clock modulation signal CLK_{mod}) the accumulator circuit 502 rolls over and continues.

Fig. 7 shows a flowchart detailing a process 700 for providing a spread spectrum based modified clock in accordance with an embodiment of the invention. The process begins at 702 by selecting a desired frequency spread Δf . Once a particular frequency spread Δf has been selected, a bipolar counter signal is selected based upon the selected frequency spread Δf at 704. It should be noted that the bipolar counter signal is a periodic signal having an average value of substantially zero. The selected bipolar counter signal is then combined with a nominal phase signal at 706 to form a modified phase signal which, in turn, is provided to a phase accumulator circuit at 708. The phase accumulator circuit then samples a reference clock signal based upon the modified phase signal at 710. The sampled reference clock signal as output of the phase accumulator is then provided to an output circuit suitably arranged to provide a modified output clock signal at 712 having a substantially unchanged central frequency and the selected frequency spread Δf .

Fig. 8 illustrates a computer system 800 employed to implement the invention. Computer system 800 is only an example of a graphics system in which the present

invention can be implemented. Computer system 800 includes central processing unit (CPU) 810, random access memory (RAM) 820, read only memory (ROM) 825, one or more peripherals 830, graphics controller 860, primary storage devices 840 and 850, and digital display unit 870. CPUs 810 are also coupled to one or more

5 input/output devices 890 that may include, but are not limited to, devices such as, track balls, mice, keyboards, microphones, touch-sensitive displays, transducer card readers, magnetic or paper tape readers, tablets, styluses, voice or handwriting recognizers, or other well-known input devices such as, of course, other computers. Graphics controller 860 generates analog image data and a corresponding reference

10 signal, and provides both to digital display unit 870. The analog image data can be generated, for example, based on pixel data received from CPU 810 or from an external encode (not shown). In one embodiment, the analog image data is provided in RGB format and the reference signal includes the VSYNC and HSYNC signals well known in the art. However, it should be understood that the present invention

15 can be implemented with analog image, data and/or reference signals in other formats. For example, analog image data can include video signal data also with a corresponding time reference signal.

Although only a few embodiments of the present invention have been described, it should be understood that the present invention may be embodied in

20 many other specific forms without departing from the spirit or the scope of the present invention. The present examples are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope of the appended claims along with their full scope of equivalents.

While this invention has been described in terms of a preferred embodiment, there are alterations, permutations, and equivalents that fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing both the process and apparatus of the present invention. It is therefore
5 intended that the invention be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

What is claimed is:

10

In the claims.

1. A clock synthesizer circuit arranged to provide a selectable spread spectrum based output clock signal, comprising:
 - 5 a phase accumulator circuit;
 - a reference clock source coupled to the phase accumulator circuit arranged to provide a reference clock signal;
 - a frequency shifter unit coupled to the phase accumulator;
 - a nominal phase source coupled to the phase accumulator coupled to the
 - 10 frequency shifter unit arranged to provide a nominal phase signal;
 - a modulated phase source coupled to the frequency shifter unit arranged to provide a modulation signal.
2. A circuit as recited in claim 1, wherein the frequency shifter unit
- 15 combines the nominal phase signal and the modulation signal to form a frequency shift signal.
3. A circuit as recited in claim 2, wherein the frequency shift signal is an
- input to the phase accumulator.
- 20
4. A circuit as recited in claim 3, wherein the phase accumulator uses the frequency shift signal to sample the reference clock signal so as to produce the output clock signal.

5. A circuit as recited in claim 4, wherein the output clock signal has a central frequency and a frequency spread based upon the modulation signal.

6. A circuit as recited in claim 1, wherein the phase accumulator circuit is
5 coupled to a read only memory (ROM) look up table.

7. A circuit as recited in claim 6, wherein the ROM look up table includes sinusoidal magnitude values.

10 8. A circuit as recited in claim 7, wherein a sampled output of the phase accumulator provides an input signal to the ROM look up table in order to convert the sampled output signal to a sinusoidal magnitude signal.

9. A method of providing a selectable spread spectrum based output
15 clock signal, comprising:
providing a phase accumulator circuit;
coupling a reference clock source to the phase accumulator circuit arranged to provide a reference clock signal;
coupling a frequency shifter unit to the phase accumulator;
20 coupling a nominal phase source to the phase accumulator coupled to the frequency shifter unit arranged to provide a nominal phase signal;
coupling a modulated phase source to the frequency shifter unit arranged to provide a modulation signal.

25 10. A method as recited in claim 9 further comprising:

combining the nominal phase signal and the modulation signal to form a frequency shift signal by the frequency shifter unit.

11. A method as recited in claim 10 further comprising:
5 inputting the frequency shift signal to the phase accumulator.
12. A method as recited in claim 11, comprising:
producing the output clock signal by the phase accumulator by.
- 10 13. A method as recited in claim 12, further comprising:
sampling the reference clock signal by the frequency shift signal.
14. A method as recited in claim 12, wherein the output clock signal has a central frequency and a frequency spread based upon the modulation signal.
- 15 15. A method as recited in claim 1, further comprising
coupling the phase accumulator circuit to a read only memory (ROM) look up table.
- 20 16. A method as recited in claim 15, wherein the ROM look up table includes sinusoidal magnitude values.
17. A method as recited in claim 16, comprising:
converting the sampled output signal to a sinusoidal magnitude signal based upon the
25 sinusoidal magnitude values included in the ROM lookup table.