

METHOD AND APPRATUS FOR INTERFACING A PROCESSOR TO A COPROCESSOR

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Abstract of the Disclosure

A processor (12) to coprocessor (14) interface supporting multiple coprocessors (14, 16) utilizes compiler generatable software type function call and return, instruction execute, and variable load and store interface
10 instructions. Data is moved between the processor (12) and coprocessor (14) on a bi-directional shared bus (28) either implicitly through register snooping and broadcast, or explicitly through function call and return and variable load and store interface instructions. The load and store interface instructions allow selective memory address preincrementation. The bi-directional bus
15 (28) is potentially driven both ways on each clock cycle. The interface separates interface instruction decode and execution. Pipelined operation is provided by indicating decoded instruction discard by negating a decode signal before an execute signal is asserted.

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FIG. 1 accompanies this abstract.