CLAIMS

What is claimed is:

1. A system comprising:

a memory device;

a volatile memory comprising buffers; and

a processing device coupled to the memory device and the volatile memory, wherein a command generation processor of the processing device is to:

receive, from a host system, a read request comprising a first logical block address (LBA) of an LBA address space for the memory device;

create a first logical transfer unit (LTU) to include the first LBA, the first LTU to be mapped to a first physical address of the memory device;

read, from the volatile memory, a flag to determine that the first LTU is associated with a zone of the LBA address space, wherein the zone comprises a plurality of sequential LBAs that are sequentially mapped to a plurality of sequential physical addresses; and

generate a set of command tags that are to direct a command execution processor of the processing device to retrieve data from the memory device and store the data in a set of the buffers, wherein the set of command tags comprises a first command tag associated with the first physical address and a second command tag associated with a second physical address that sequentially follows the first physical address.

2. The system of claim 1, wherein each command tag of the set of command tags comprises:

an LTU number identifying an LTU that is mapped to a physical address of a physical address space of the memory device; and

a buffer address of a location within the set of the buffers.

3. The system of claim 1, wherein the set of command tags further comprises additional command tags associated with subsequent physical addresses that are sequentially numbered following the second physical address, and wherein each subsequent physical address is incremented by page number until reaching an end of a read window size from the first physical address.

4. The system of claim 1, wherein the command generation processor of the processing device is further to:

retrieve, from the volatile memory, the first physical address; and

return, to the host system, a first subset of the data retrieved from the first physical address and that is stored in a first buffer of the set of the buffers.

5. The system of claim 4, wherein, in response to a second read request, the command generation processor is to:

determine that a second LBA of the second read request corresponds to the second physical address;

retrieve a second subset of the data from a second buffer of the set of the buffers, the second buffer having a buffer address associated with the second command tag; and

transmit the second subset of the data to the host system.

6. The system of claim 1, wherein a translation processor of the processing device is to set the flag in the volatile memory based on the data being sequentially written to the memory device.

7. The system of claim 1, wherein the command generation processor is further to transmit, to the command execution processor of the processing device, a group of commands respectively comprising one of the set of command tags, and in response to receipt of the set of command tags, the command execution processor is to retrieve the data from the memory device and store the data in the set of the buffers according to respective buffer addresses of the set of command tags.

8. The system of claim 1, wherein the command generation processor is further to:

interlink the set of command tags into a command chain; and

transmit the command chain in a single command message to the command execution processor.

9. The system of claim 1, wherein the command generation processor is further to allocate and track the buffers within the volatile memory using one of:

a two-three tree algorithm in which the buffers are sorted by LTU number; or

an N-way cache that employs a hash algorithm.

10. A method comprising:

receiving, by a command generation processor of a processing device, a read request comprising a first logical block address (LBA) of an LBA address space for a memory device;

creating, by the command generation processor, a first logical transfer unit (LTU) to include the first LBA, the first LTU to be mapped to a first physical address of the memory device;

reading, by the command generation processor from a volatile memory, a bit value of a bit map to determine that the first LTU is associated with a zone of the LBA address space, wherein the zone comprises a plurality of sequential LBAs that are sequentially mapped to a plurality of sequential physical addresses;

allocating, by the command generation processor, a set of buffers in the volatile memory, wherein a capacity of the set of buffers matches an amount of data stored at the first physical address and at subsequent physical addresses that are sequentially numbered within a read window size that starts at the first physical address; and

generating, by the command generation processor, a set of command tags that are to direct a command execution processor of the processing device to retrieve the data from the memory device and store the data in the set of buffers, wherein the set of command tags comprise at least a first command tag associated with the first physical address and a second command tag associated with a second physical address, of the subsequent physical addresses, that sequentially follows the first physical address.

11. The method of claim 10, further comprising, by the command generation processor:

retrieving, from the volatile memory, the first physical address;

determining that a die available flag, associated with the first physical address, is set; and

returning, to a requesting agent, a first subset of the data retrieved from the first physical address and that is cached in a first buffer of the set of buffers.

12. The method of claim 11, further comprising:

receiving a second read request;

determining that a second LBA of the second read request corresponds to the second physical address within the read window size from the first physical address;

retrieving a second subset of the data from a second buffer of the set of buffers, the second buffer having a buffer address associated with the second command tag; and

transmitting the second subset of the data to the requesting agent.

13. The method of claim 10, further comprising tracking usage of the set of buffers via use of one of a flag or a counter for each buffer, wherein the tracking enables use of the set of buffers by multiple host applications corresponding to multiple zones.

14. The method of claim 10, wherein the set of command tags further comprise additional command tags associated with the subsequent physical addresses, to include the second command tag, the method further comprising determining the subsequent physical addresses by incrementing the first physical address by page number until reaching an end of the read window size from the first physical address.

15. The method of claim 10, wherein generating the set of command tags further comprises updating, within a command buffer of the volatile memory:

the first command tag with a first LTU number of the first LTU and a first buffer address of the set of buffers; and

the second command tag with a second LTU number of second LTU, corresponding to a second LBA, and a second buffer address of the set of buffers.

16. The method of claim 10, further comprising, by a translation processor of the processing device:

determining that the first LBA is associated with the zone; and

setting the bit value, associated with the first physical address, in the volatile memory based on the data being sequentially written to the memory device.

17. The method of claim 10, wherein the set of command tags further comprise additional command tags associated with the subsequent physical addresses, to include the second command tag, the method further comprising:

transmitting, by the command generation processor to the command execution processor, a group of commands respectively comprising the set of command tags;

retrieving, by the command execution processor, the data from the first physical address and from the subsequent physical addresses of the memory device; and

storing the data in the set of buffers according to respective buffer addresses of the set of command tags.

18. The method of claim 10, further comprising:

interlinking the set of command tags into a command chain; and

transmitting the command chain in a single command message to the command execution processor.

19. The method of claim 10, further comprising tracking allocation of the set of buffers within the volatile memory via one of:

a two-three tree algorithm in which the set of buffers are sorted by LTU; or

an N-way cache that employs a hash algorithm.

20. A non-transitory computer-readable medium storing instructions, which when executed by a command generation processor of a processing device of a sub-system memory controller, cause the processing device to perform a plurality of operations comprising:

receiving a read request comprising a first logical block address (LBA) of an LBA address space for a memory device;

creating, by the command generation processor, a first logical transfer unit (LTU) to include the first LBA, the first LTU to be mapped to a first physical address of the memory device;

reading, from a volatile memory, a flag to determine that the first LTU is associated with a zone of the LBA address space, wherein the zone comprises a plurality of sequential LBAs that are sequentially mapped to a plurality of sequential physical addresses;

allocating a set of buffers in the volatile memory, wherein a capacity of the set of buffers matches an amount of data stored at the first physical address and at subsequent physical addresses that are sequentially numbered within a read window size that starts at the first physical address; and

generating a set of command tags that are to direct a command execution processor of the processing device to retrieve the data from the memory device and store the data in the set of buffers, wherein the set of command tags comprise at least a first command tag associated with the first physical address and a second command tag associated with a second physical address, of the subsequent physical addresses, that sequentially follows the first physical address.