CLAIMS

1. A pulse width testing circuit, comprising:

a first sampling module, configured to receive a to-be-tested pulse signal, and sample an inverted signal of the to-be-tested pulse signal to generate a first sampled signal; and

a second sampling module, configured to receive the to-be-tested pulse signal, and sample the to-be-tested pulse signal to generate a second sampled signal,

wherein the second sampled signal and the first sampled signal have a phase difference, the phase difference being equal to a pulse width of the to-be-tested pulse signal;

wherein the first sampling module comprises:

a first temporary storage unit, configured to sample a first feedback signal in response to the to-be-tested pulse signal so as to generate a first temporary storage signal, wherein a triggering type of the first temporary storage unit is edge triggering, and an edge of the first temporary storage signal corresponds to a first edge of the to-be-tested pulse signal and corresponds to an edge of the first sampled signal;

a first inverter, wherein the first inverter forms a first feedback loop together with the first temporary storage unit, the first feedback loop is configured to respond to the to-be-tested pulse signal and generate the first feedback signal, and an edge of the first feedback signal corresponds to the first edge of the to-be-tested pulse signal;

wherein the second sampling module comprises:

a second temporary storage unit, configured to sample a second feedback signal in response to the to-be-tested pulse signal so as to generate a second temporary storage signal, wherein a triggering type of the second temporary storage unit is edge triggering, and an edge of the second temporary storage signal corresponds to a second edge of the to-be-tested pulse signal and corresponds to an edge of the second sampled signal;

a fourth inverter, wherein the fourth inverter forms a second feedback loop together with the second temporary storage unit, the second feedback loop is configured to respond to the to-

be-tested pulse signal and generate the second feedback signal, and an edge of the second feedback signal corresponds to the second edge of the to-be-tested pulse signal.

2. The pulse width testing circuit of claim 1, wherein the first sampling module is configured to generate the first sampled signal in response to a falling edge of the to-be-tested pulse signal, and the second sampling module is configured to generate the second sampled signal in response to a rising edge of the to-be-tested pulse signal.

3. The pulse width testing circuit of claim 1, wherein a first delay time of the first sampling module on a first transmission path is equal to a second delay time of the second sampling module on a second data transmission path.

4. The pulse width testing circuit of claim 1, wherein the first temporary storage unit comprises one or more of a trigger, a latch or a register.

5. The pulse width testing circuit of claim 1, wherein an input terminal of the first inverter is connected to an output terminal of the first temporary storage unit, an output terminal of the first inverter is connected to an input terminal of the first temporary storage unit, and the first inverter is configured to invert the first temporary storage signal so as to generate the first feedback signal.

6. The pulse width testing circuit of claim 5, wherein the first sampling module further comprises:

a second inverter, wherein an input terminal of the second inverter is connected to the output terminal of the first inverter, and the second inverter is configured to receive the first feedback signal, invert the first feedback signal and output the inverted first feedback signal as the first sampled signal.

7. The pulse width testing circuit of claim 1, wherein the first sampling module further comprises:

a third inverter, wherein an input terminal of the third inverter is connected to the to-be-tested pulse signal, an output terminal of the third inverter is connected to a drive terminal of the first temporary storage unit, and the third inverter is configured to receive the to-be-tested pulse signal and output an inverted to-be-tested pulse signal to the first temporary storage unit.

8. The pulse width testing circuit of claim 7, wherein the second sampling module further comprises a transmission gate, and a fifth inverter,

wherein an input terminal of the transmission gate is connected to the to-be-tested pulse signal, an output terminal of the transmission gate is connected to a drive terminal of the second temporary storage unit, and the transmission gate is configured to transmit the to-be-tested pulse signal to the second temporary storage unit; and

an input terminal of the fifth inverter is connected to an output terminal of the fourth inverter, and the fifth inverter is configured to receive the second feedback signal, invert the second feedback signal and output the inverted second feedback signal as the second sampled signal.

9. The pulse width testing circuit of claim 1, wherein the first sampled signal and the second sampled signal are square wave signals, and have a same signal amplitude, frequency and duty cycle.

10. The pulse width testing circuit of claim 8, wherein the first temporary storage unit and the second temporary storage unit both respond to a rising edge.

11. A testing device, comprising:

the pulse width testing circuit of any of claims 1 to 10; and

an analysis module, connected to the pulse width testing circuit, and configured to obtain a width of a to-be-tested pulse signal according to a phase difference between the first sampled signal and the second sampled signal, wherein the phase difference is equal to a pulse width of the to-be-tested pulse signal.

12. A pulse width testing method, performed by the testing device of claim 11, the method comprising:

receiving, by the first sampling module and the second sampling module, a to-be-tested pulse signal;

generating, by the first sampling module and the second sampling module, a first sampled signal and a second sampled signal according to the to-be-tested pulse signal respectively; and

obtaining, by the analysis module, the first sampled signal and the second sampled signal, and obtaining a width of the to-be-tested pulse signal according to a phase difference between the first sampled signal and the second sampled signal,

wherein the phase difference is equal to a pulse width of the to-be-tested pulse signal.

13. The pulse width testing method of claim 12, wherein generating, by the first sampling module and the second sampling module, the first sampled signal and the second sampled signal according to the to-be-tested pulse signal respectively comprises:

generating, by the first sampling module, the first sampled signal in response to a falling edge of the to-be-tested pulse signal, and

generating, by the second sampling module, the second sampled signal in response to a rising edge of the to-be-tested pulse signal.

14. The pulse width testing method of claim 12, wherein generating, by the first sampling module, the first sampled signal comprises:

sampling, by a first temporary storage unit of the first sampling module, a first to-be-sampled signal in response to the to-be-tested pulse signal to generate a first temporary storage signal, wherein a triggering type of the first temporary storage unit is edge triggering, and an edge of the first temporary storage signal corresponds to a first edge of the to-be-tested pulse signal; and

outputting, by the first temporary storage unit, the first temporary storage signal as the first sampled signal.

15. The pulse width testing method of claim 14, further comprising:

providing a first inverter; wherein the first inverter and the first temporary storage unit form a first feedback loop; and

generating, by the first feedback loop responding to the to-be-tested pulse signal, a first feedback signal; wherein an edge of the first feedback signal corresponds to the first edge of the to-be-tested pulse signal.

16. The pulse width testing method of claim 15, further comprising:

providing a second inverter; wherein an input terminal of the second inverter is connected to the output terminal of the first inverter; and

receiving, by the second inverter, the first feedback signal, and generating the first sampled signal according to the first feedback signal.

17. The pulse width testing method of claim 14, further comprising:

providing a third inverter; wherein an input terminal of the third inverter is connected to the to-be-tested pulse signal, an output terminal of the third inverter is connected to a drive terminal of the first temporary storage unit; and

receiving, by the third inverter, the to-be-tested pulse signal and outputting an

inverted to-be-tested pulse signal to the first temporary storage unit.